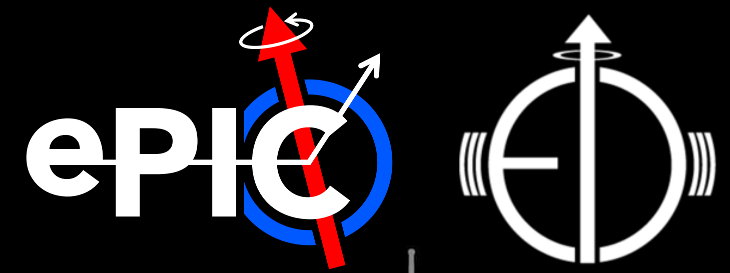


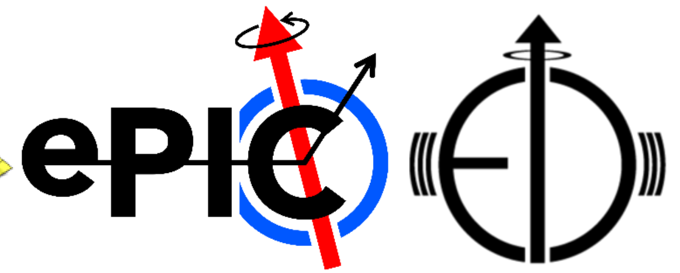
ePIC SVT Module Bonding

James Glover & Eve Tse

EIC-UK WP1 (MAPS)
Face-to-Face meeting @ Oxford

Thu, 3rd October 2024

SVT OB Module



Outer Barrel (Layer3, Layer4)

- Double-sided staves
- Using EIC-LAS (6 RSUs, 5 RSUs)
- 2 EIC-LAS wide (1 module)
- 4 or 8 modules long
- 2 or 4 groups of 4 EIC-LAS (8, 16 total)

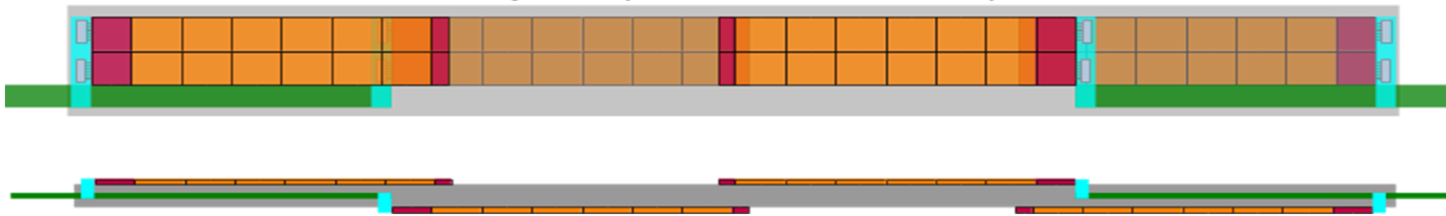
Ancillary ASIC

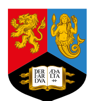
Bridge FPC

EIC LAS

Kapton support sheet

OB L3 (EIC-LAS with 6 RSUs)

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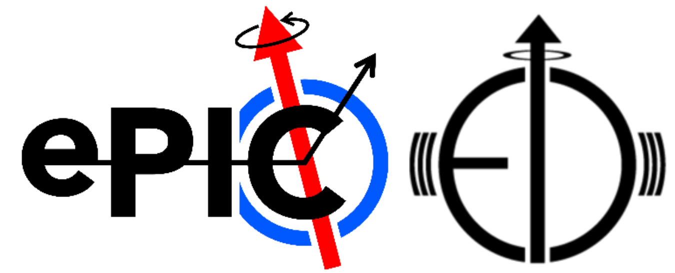
Connections needed



- The AncASIC is needed for the powering and slow controls.
- Data can be readout from EIC-LAS directly.

Element	Power	Data	Slow Controls
EIC-LAS	✓	✓	✓
AncASIC	✓	✗ *	✓
FPC	✓	✓	✓

* Adding data connections to the AncASIC would just be a passthrough (EIC-LAS to AncASIC to FPC). Why add the extra connection point (point of failure)? However, it is only 1 channel (2 pads/traces).

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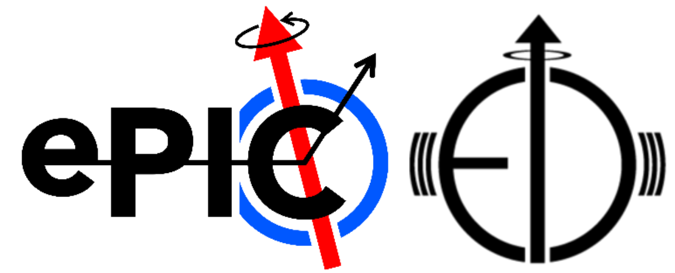
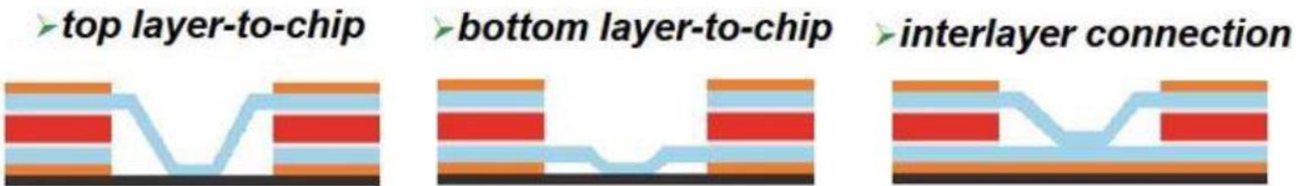
spTAB vs wire bonding



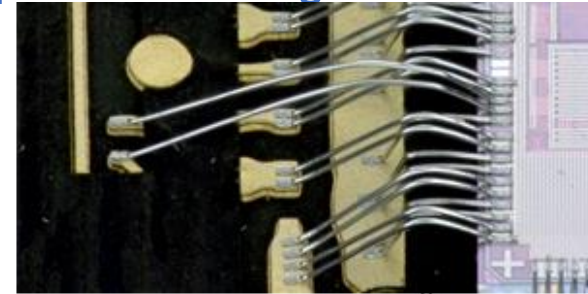
spTAB

- FPC traces have opening in support at bond locations.
- Aluminium trace (of FPC) is directly welded to a pad on the chip*.
- Foil width: ~70 μm.
- Best when FPC is above the chip*.
- Recommended by LTU.
  - Wire bonding to FPC is possible.



Wire bonding

- Wire connection between pads on 2 separate substrates (chip* or FPC).
- Wire width: ~25 μm
- Best when FPC is below the chip*.
- The current base-line for the ITS3 MOSAIX chip.
  - spTAB is being considered.



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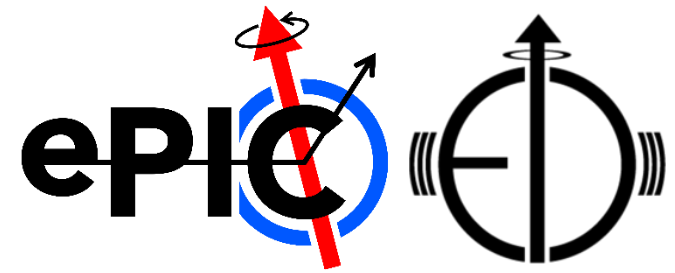
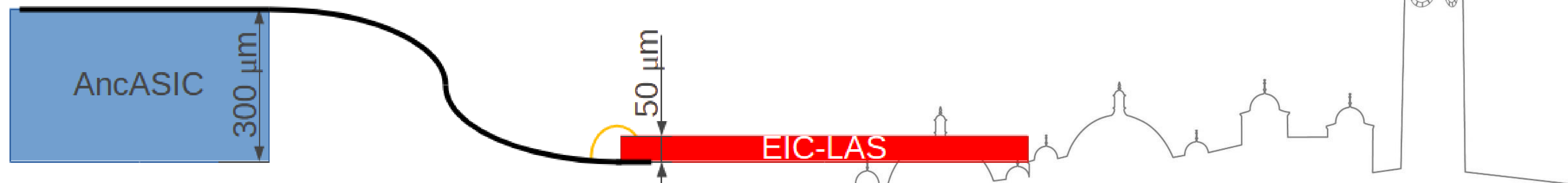
* (EIC-LAS or AncASIC).

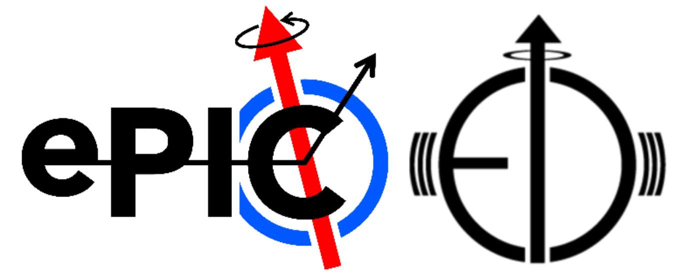
AncASIC vs EIC-LAS



- We are designing the AncASIC – we can dictate pad size, shape, pitch, location, and surface finish.
- EIC-LAS (based on MOSAIX) will have a pad design dictated by ITS3.
  - If they finalise a pitch too small for spTAB, we will have to wire bond!
- Mixed bonding is possible (spTAB for AncASIC and wire bonds for EIC-LAS), but the FPC would have to bend from top of AncASIC to bottom of EIC-LAS (300 µm height difference).
- The FPC has a min bend radius of 5 mm, this dictates a 2.5 mm (larger) gap between chips to account for the curve!

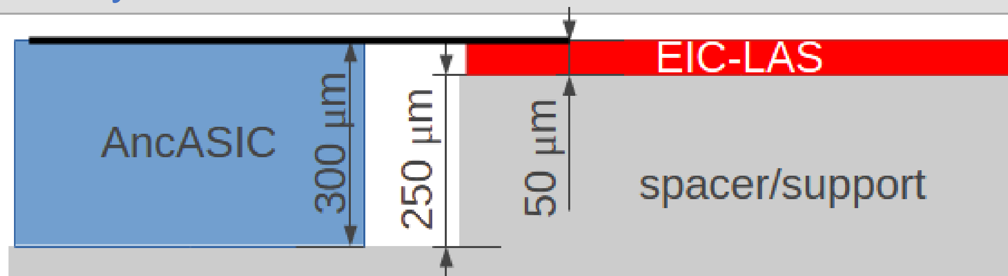


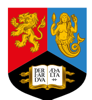
All spTAB



- One bond process would make the production easier.
- To avoid the spacing implication of different surface heights, top of EIC-LAS and AncASIC need to be level.
  - Requires tooling to account for different chip thicknesses.
- Sites (currently) have more expertise with wire bonding.
  - Time needed to change wedge tools in bond machines.
  - Machines (currently) shared with other projects that require wire bonds.
  - A lot of tool changes to accommodate the many projects*.

* May be less of an issue if/when a dedicated bonder is available.





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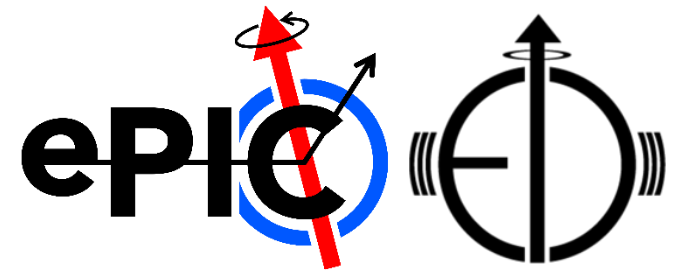
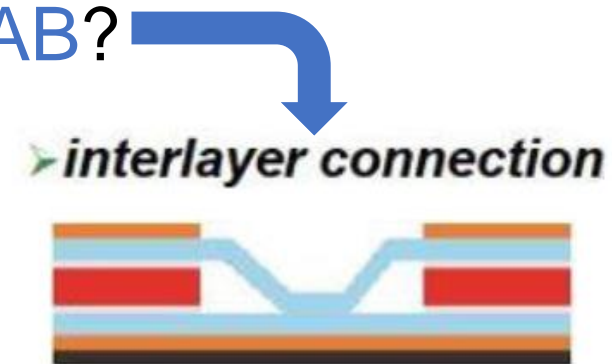
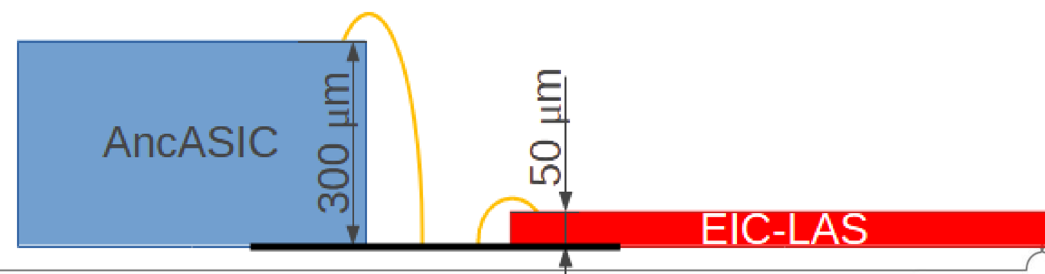
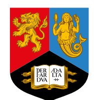
All wire bonds



- One bond process would make the production easier.
- Sites (currently) have more expertise with wire bonding.
    - No time lost due to changing wedge tools in bond machines.
    - Easier to share machines across projects.
- No special tooling required to get surfaces level.
- Do FPC interlayer connections still need spTAB?
    - Therefore, maybe it isn't one bond process?



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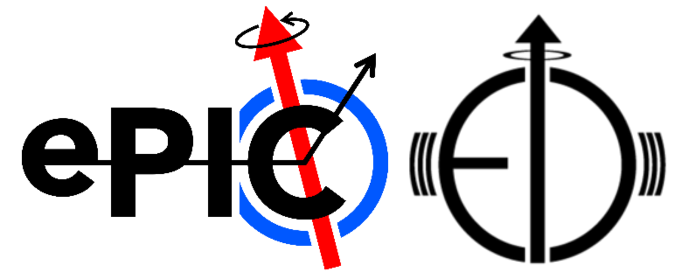
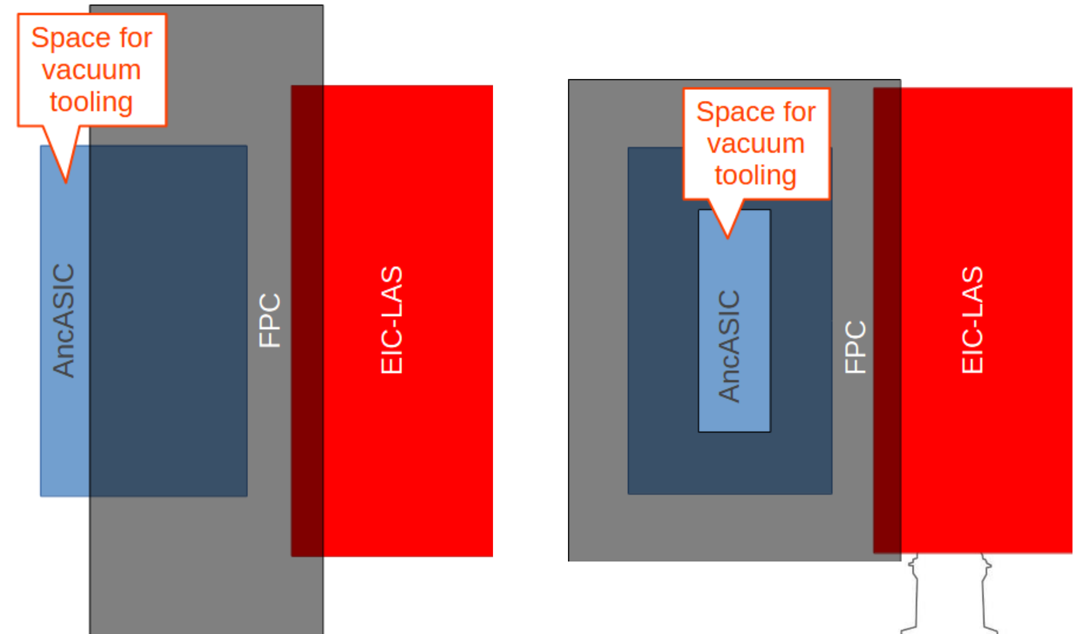
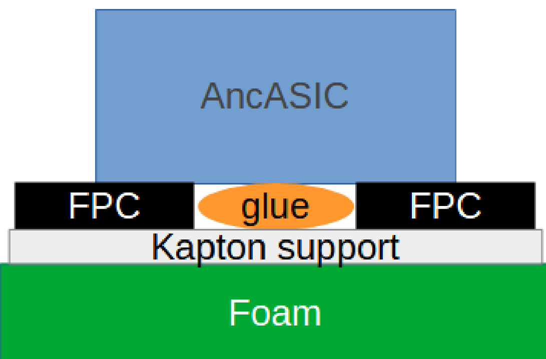
FPC design to fit assembly



Regardless of whether the FPC is above or below the AncASIC, there are still complications.

- FPC above (spTAB) – we need space for vacuum tooling to pick up the AncASIC (opening in FPC or uncovered edge).
  - Relying on bonds to hold AncASIC!





- FPC below (wire bond) – we want good thermal path to carbon foam (conductive glue within opening on FPC).
  - Relying on glues to hold FPC and Kapton!

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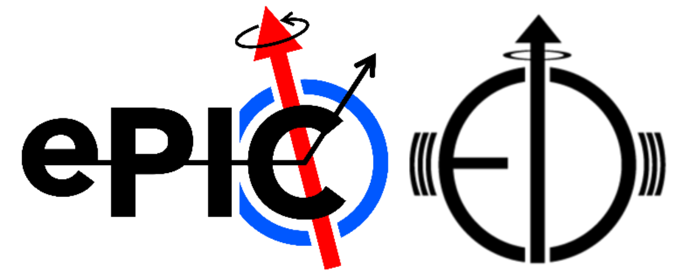
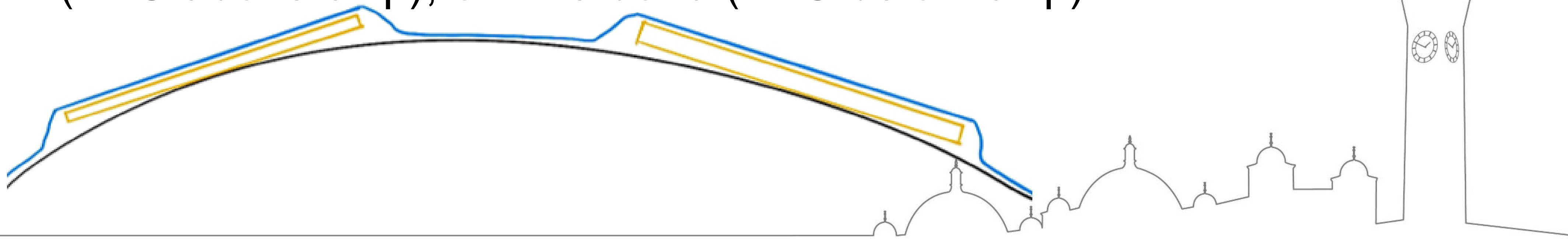
Mixing flat and curved silicon



- Mixing a flat AncASIC on a curved stave adds complexity.
- To build modules flat, there needs to enough tolerance in Kapton support layer and FPC to still follow curvature of stave.
- Can not bond a flat surface to a curved surface.
- We become very dependant to finding the right glues.
  - For structural support, while enabling curvature and a thermal path.
- Assembly sequence is dictated by bond choice.
  - spTAB (FPC above chip), or wire bond (FPC below chip).



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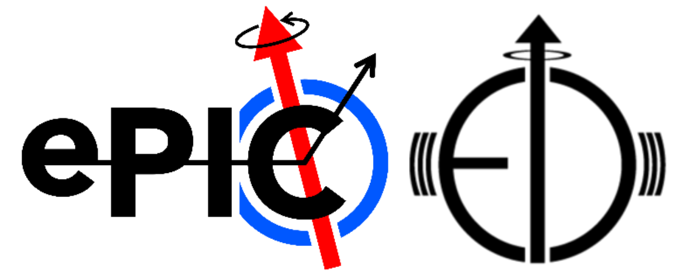
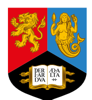
Summary



- A lot of variables to consider.
- Preference would be to minimise the number of bond processes.
  - FPC interlayer connection might dictate spTAB.
  - ITS3's final design could dictate wire bonding.
- spTAB is a challenge to set-up, with shared machines and down-time for tooling changes – a short-term problem.
- Tooling and thermal path considerations also to be considered.
- Keeping a flat AncASIC, while the rest of the module bends adds complications.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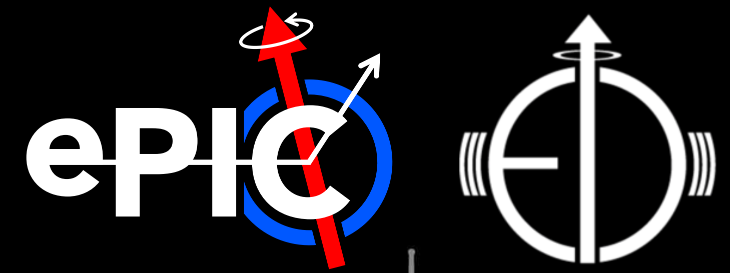

Thank you very much!

Any questions?

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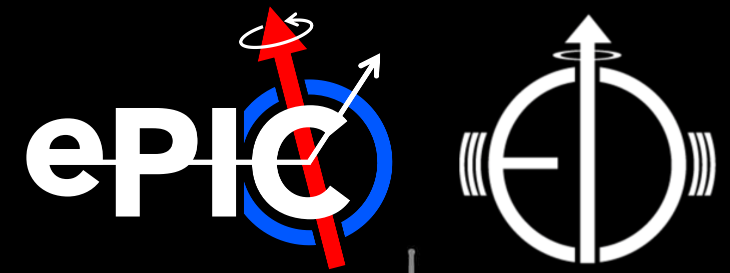
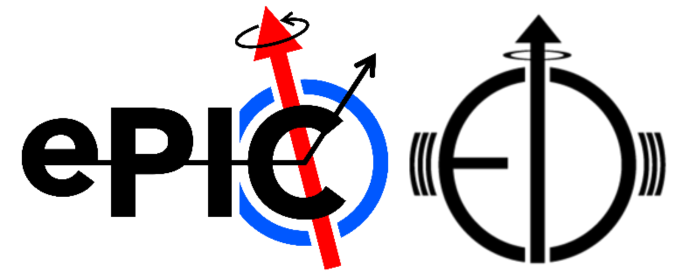
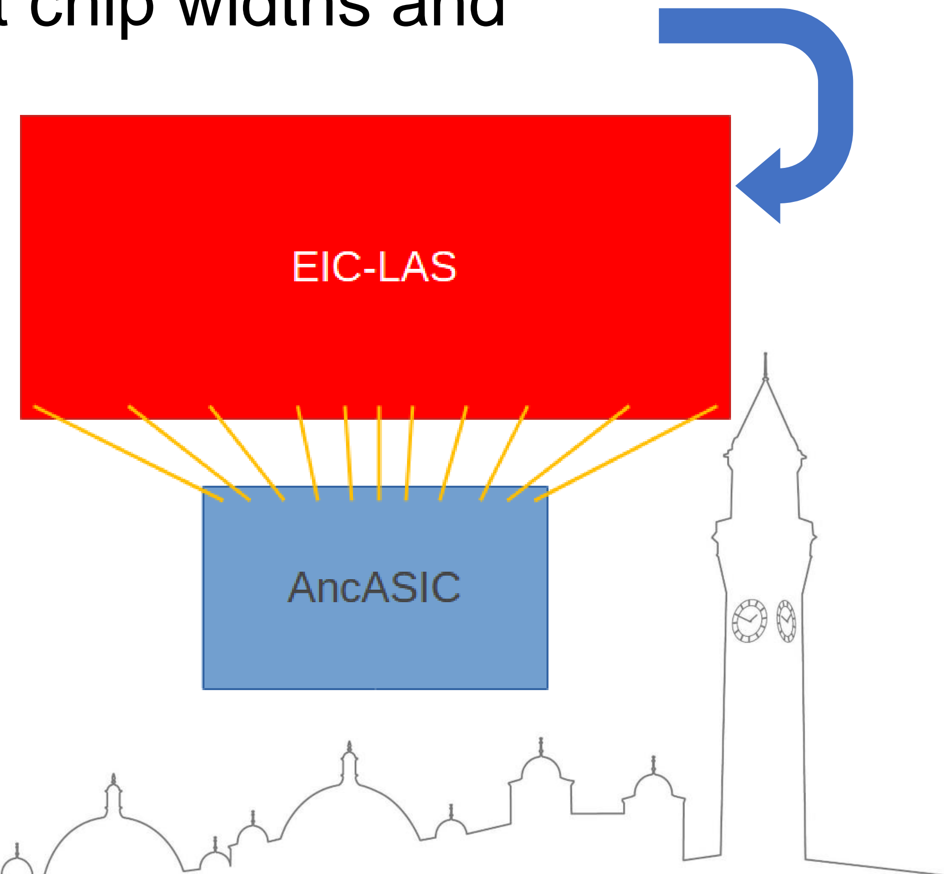


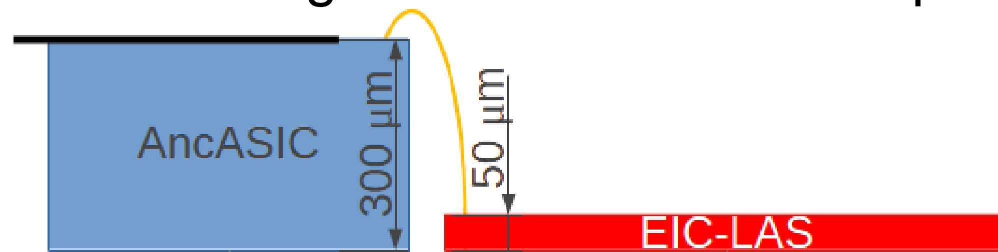
Additional (support) slides

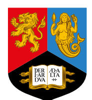
Should we add data to AncASIC?



- If the data channel is added to AncASIC, we could bond directly between AncASIC and EIC-LAS (without interconnects through the FPC) – assuming bond angles fit with different chip widths and predominately on 1 chip edge.
- Then FPC only interfaces with AncASIC.
  - Only one chip height to think about, minimises interconnections.
- Requires use of both bonding techniques.
  - Slows production to switch tooling/machine.
  - Dedicated tab bonding machine can be cheaper.



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