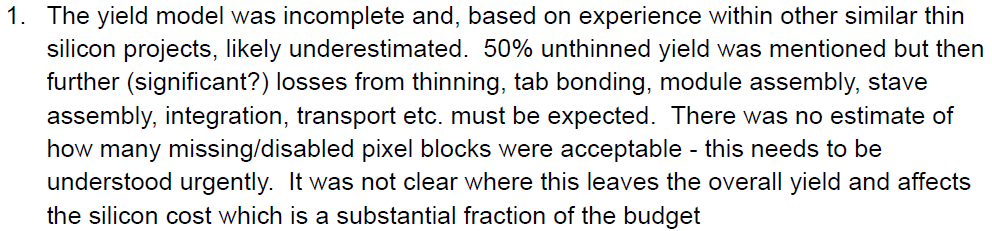
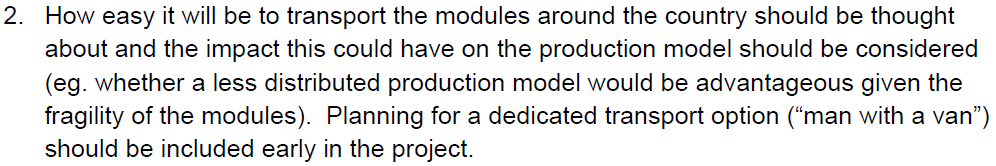
# Response to review comments

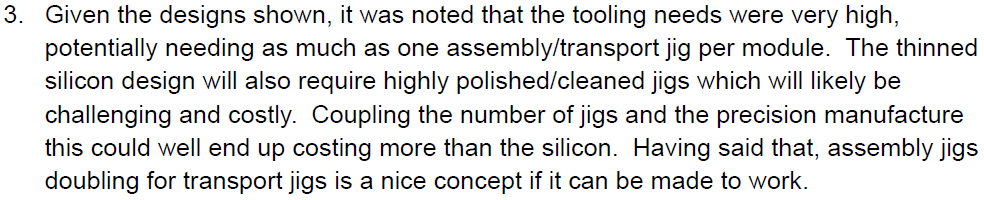


We cannot answer this question. It requires the effect of missing blocks to be included in the overall ePIC simulations. ITS3 have started to publish some data that discuss how the power supply is arranged (https://indico.cern.ch/event/1381495/contributions/5988496/) and “yield” (https://indico.cern.ch/event/1381495/contributions/5988500/) but this is only really good for showing the rough size of a failed area. We need to know from physics simulations how many of these are tolerable. 50% yield on the silicon assuming some tolerance of these failed blocks is probably reasonable, but we do not know about the rest.



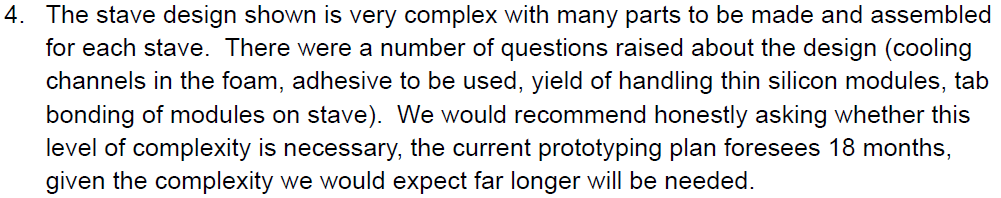
The construction of the OB components in the UK is a joint project of several UK institutions, which all have an important role to play in this. The distributed manufacture is motivated by limits on effort and equipment, and matches activities to expertise available at the different sites.

The current anticipated rate of production for modules is 10 per week at two assembly sites (Birmingham and Daresbury Lab). Even if these require a backing jig, the volume required is not likely to exceed 500×500×150 mm, which can easily fit into a Peli case or similar. We will study transport of modules once we have accrued experience in handling the modules. At this point we are confident that we will not require dedicated transport. However, we are aware that such arrangements are in place for the components for the ATLAS strip and pixel systems, and if there is overlap, we will investigate the possibility to join this arrangement.



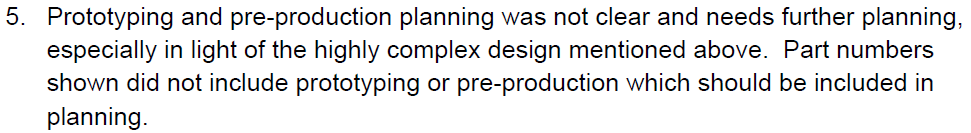
The number of possible jigs and their cost is a valid concern. We are just at the beginning of the optimisation of the jigs for this project, but we keep an eye on costs of jig components needed for protection during transport and storage in our development.

In any case, it is unlikely that we will need one assembly/transport jig per module, as we intend to load staves in parallel with production of modules, so that we only need to provide enough storage capacity to buffer fluctuations in module or stave production. If we assume that these fluctuations can be equivalent to four weeks, this would mean storage capacity for 80 modules. For the staves it is more likely that we will need one transport/storage jig per stave, as we will have less control over the timing of the integration at BNL, but the total number of staves including spares will be less than 150.

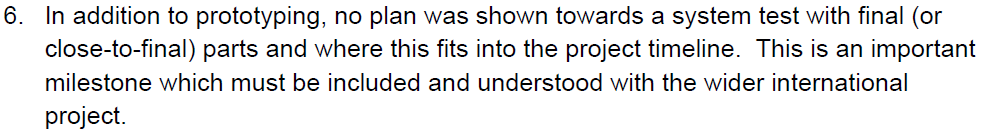


We actually think that the stave design is not that complex, and the number of parts in a stave is not that large (facesheets, central I-beam spur, FPCs, K9 cross-ribs, modules). We cannot see how this could be simplified, while still maintain the concepts of internal air flow and modules that can be tested separately, concepts that we think are central to our approach.

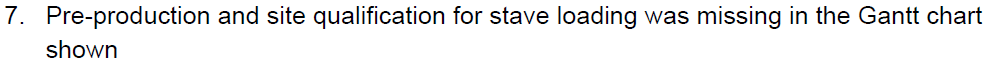
Arguably the biggest complication is the curved shapes of the facesheets, and we are currently evaluating benefits and drawbacks of this design feature. For the first round we will proceed with prototyping the curved surface as this is the more challenging design geometry.



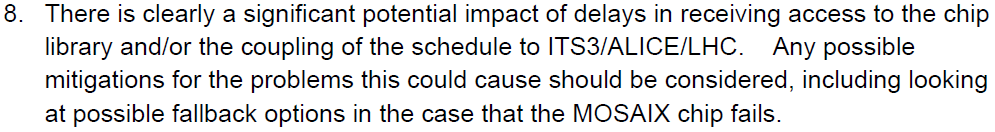
Peter:



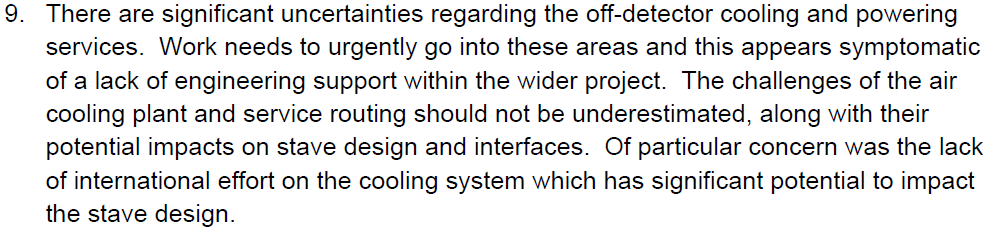
This is something which needs to be organised by the international project and we will raise this there.



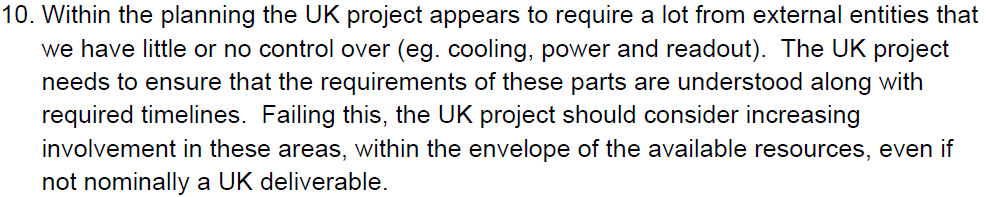
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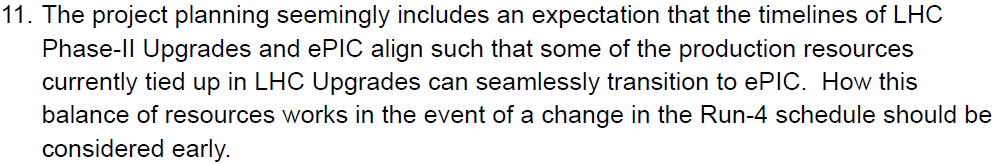
The current ePIC fallback plan is to use ALPIDE/ITS2 sensors if we cannot use MOSAIX. However, given the promising tests coming from the MOSS sensor, it would be hard to imagine MOSAIX failing completely (delays are more likely to be the problem).



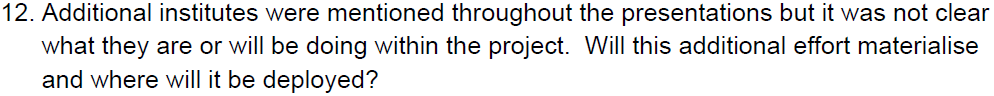
We share these concerns, but these are not responsibilities of the UK groups. We will raise these concerns (again) with our international collaborators.



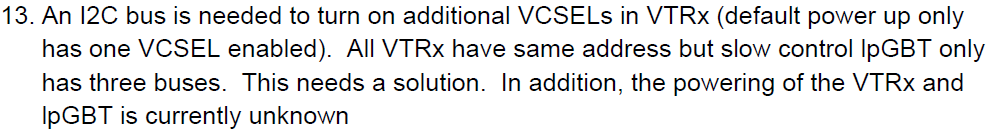
The funds we have requested from and have been awarded by UKRI have been determined based on the plan that our contribution to the SVT will be the manufacture of the OB staves. We believe that this contribution matches our strengths and expertise. We believe that taking over the suggested additional responsibilities would require a significant extension of both our resources and expertise, which we think cannot be achieved within the constraints of the awarded funding. It should also be noted that the ePIC experiment is primarily a US venture, and central responsibilities for the experiment do belong to US institutions.



There is indeed an overlap in construction responsibilities of several groups involved in ePIC with ATLAS. Current planning foresees that UK construction activities for ATLAS should ramp down significantly before the main activities for ePIC. There is obviously a risk that ATLAS construction will be delayed and that this will impact our ePIC activities. However, there is not much that we can do about this, other than monitoring the ATLAS schedule, and explore mitigations in case that significant delays emerge.

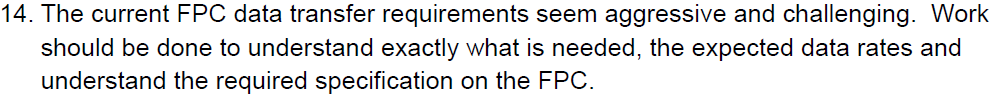


Peter:

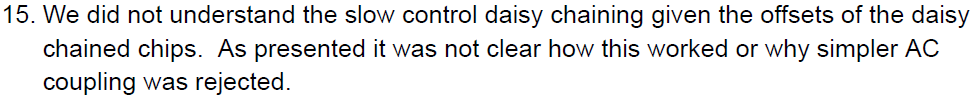


We thank the reviewers for bringing this to our attention. We have raised the point with one of your US readout specialists (Jo Schambach, ORNL), his response:

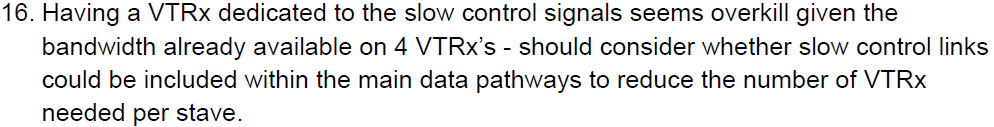
“This means many more lpGBT ASICs. For our case, I am thinking along the lines of adding a “I2C multiplexer” behind the lpGBTs on the control boards (e.g. TCA9544A) which will provide either 4 or 8 additional I2C busses for each lpGBT I2C master. Since these are only used during power up to configure the VTRx+, I think radiation will not be an issue, hopefully they will only see SEEs during operation which shouldn’t matter, since we likely will not use them during beam operation.”



Marcello, Todd:



We have raised the point with the BNL designers of this system. We are awaiting a response. (More details have been shown in the chip designer’s meetings, but not publicly. As far as we know, the design works in theory/simulations, but has never been tested with the required foundry fabrication method/technology).



This can be considered, however it would require much more complex interconnection between boards at different locations in the detector, SC boards are likely to be further from the IP as they talk to up to 16 sets of (up to 4) EIC-LAS, while the RO boards will be as close to the FPC edge as we can, so 1 per set of (up to 4) EIC-LAS. A comparison of complexity and total service material for both configurations can be considered.