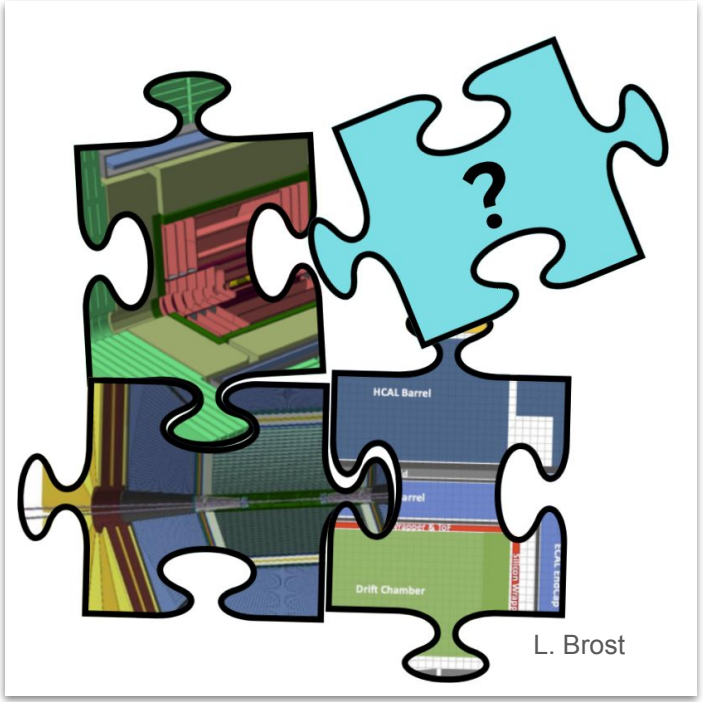
# US HFCC: **A**I, **I**ntegrated Detector Concepts, & **M**icroelectronics

L2 : Julia Gonski, Jim Hirschauer
L3 : Tim Andeen, Liza Brost, Jennet Dickinson, Loukas Gouskos


L2 Session, Strategic Joint Meeting of US HFCC
9 November 2024

# AIM Overview

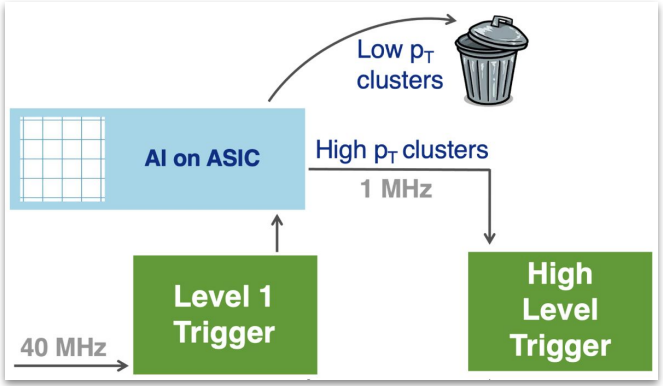
- Focus on **cross-cutting** topics: AI/ML, Integrated Detector Concepts, & Microelectronics
  - Critical to maintain strong connections with HFCC Subdetector L2 Areas, HFCC Software/Computing, HFCC TDAQ, and International efforts
- AIM group evolved from cross-cutting **“Readout/ASICs”** group in P5 costing exercise *[2306.13567]*
  - Enhanced with addition of other cross-cutting topics :
    - AI/ML
    - Integrated Detector Concepts
- HFCC AIM Community Kickoff 6 Nov

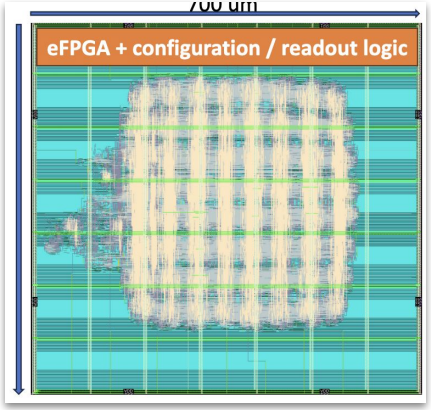


L. Brost

# Scope: AI/ML

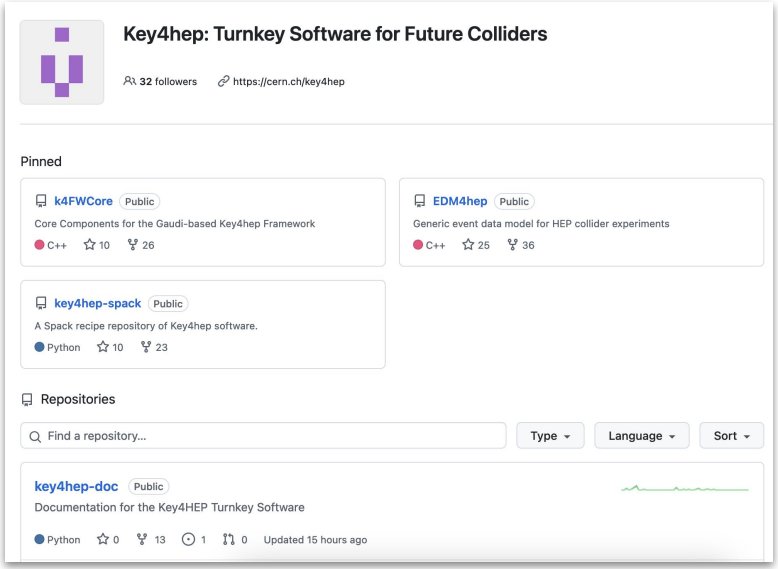
- ***L3: Jennet Dickinson (Cornell)***
- **Potential Work Packages:**
  - AI/ML in on-detector hardware – coordinate with AIM Microelectronics
  - AI/ML in off-detector hardware
  - Algorithm development and optimization: data compression, feature extraction, classification, anomaly detection, etc.
  - AI/ML for detector optimization – coordinate with AIM Integrated Detector Concepts
- **Existing Work/ US Expertise**
  - AI-ASIC development (UT Austin, Cornell, UChicago, UIC, JHU, FNAL, LBNL, SLAC, ANL, BNL, ORNL)
  - Differentiable programming-based ML detector optimization (SLAC)
  - Embedded FPGAs (SLAC, LBNL)



# Scope: Integrated Detector Concepts

- ***L3s: Liza Brost (BNL), Loukas Gouskos (Brown)***
- Critical to coordinate with partners – especially HFCC Software/Computing and International efforts.
- **Potential Work Packages:**
  - Physics studies: strategy, develop/streamline existing SW frameworks, execution
  - Design and optimization of whole-detector concepts – coordinate with AIM AI/ML
  - Integration of subsystem capabilities (e.g. fast timing)
  - Whole-detector data simulation (e.g. for TDAQ bandwidth studies)
- **Existing Work/ US Expertise**
  - Leadership of FCC PED studies for physics benchmarks (BNL, Brown, Maryland, MIT, SLAC, etc)
  - Key4HEP software development (Princeton)



# Scope: Microelectronics

- ***L3: Tim Andeen (UTexas Austin)***
- **Community-driven Work Packages (tentative):**

| **Research Area** | **Ongoing and future effort** |
|---|---|
| AI/ML in ASICs, intelligence on detector | UTAustin, UChicago, Cornell, UIC, UIUC, JHU, Kansas, ANL, LBNL, BNL, FNAL, SLAC, ORNL |
| Common IP for future MOSFET process nodes (28 nm e.g.) | LBNL, BNL, FNAL |
| 3D / hybrid integration | USSC, LBNL, BNL, FNAL |
| Silicon photonics | ANL, LBNL, FNAL |
| High data density (including fast optical links | UPenn, ANL, LBNL, FNAL |
| Novel materials / devices | LBNL, FNAL |
| Novel design tools : open source, automated, AI/ML enhanced | UPenn, LBNL, BNL, FNAL, HEPIC |
| MAPS, 4D/5D sensor + ASICs, electronics for precision timing (now covered in Tracker L2 area) | UMichigan, ND, Oregon, UCSC, ANL, LBNL, BNL, FNAL, SLAC, ORNL |

# Short Term Needs : Item 1

**Physics studies for Integrated Detector Concepts – US-coordinated Community Detector Design/Optimization "Challenge"**

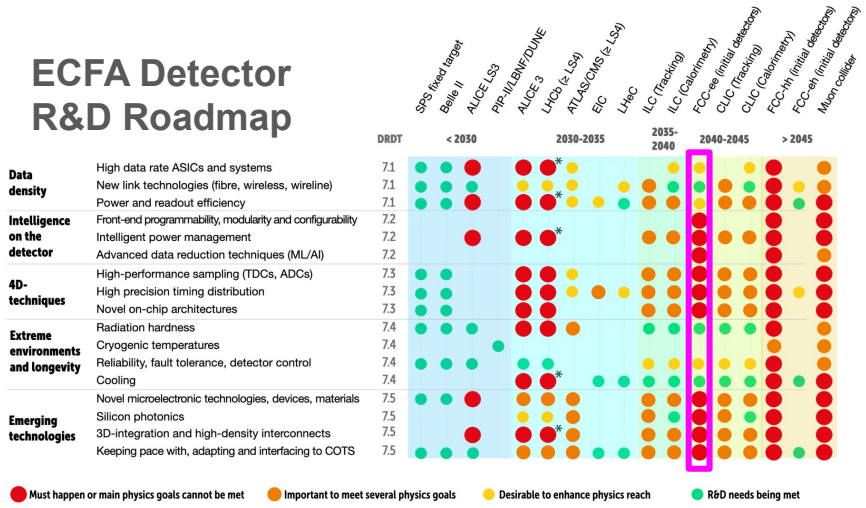
- **Motivation:**
  - Lower the barrier to entry and inspire the US community to enhance contribution to **international efforts** for Integrated Detector physics studies
  - Inspire new optimization and design ideas, both of which are key deliverables for AIM and HFCC.
  - HFCC Charge Item 1
- **Description:** Physicist effort to streamline benchmarks, samples, and code frameworks towards US-coordinated Community Detector Design/Optimization "Challenge" for FY25
  - Synergistic with HFCC Software & Computing, FY24 funding (Key4HEP @ Princeton), FCC Det Concepts planning
- **Short term criticality :** International FCC Det Concepts group is targeting Integrated Detector Concept physics studies for FY25
- **Resources:** $140k

| **Funding** | **Resource** | **Activity** |
|---|---|---|
| $40k | 0.4 FTE post doc | Develop **streamlined** + **user-friendly** software/simulation/documentation - based on existing SW |
| $80k | 0.8 FTE grad student | Assist in code development and training in key detector R&D software |
| $20k | Travel | Sharing results with community (Int'l FCC / HF) and in-person challenge workshops. |

# Short Term Needs : Item 2

## Advanced AI-in-ASIC microelectronics technology for FCC

- **Motivation:**
  - **DOE HEP Det R&D BRN, ECFA Roadmap, Snowmass Reports, and FCC P5 costing report** : microelectronics critical for achieving HF / FCC-ee physics potential
  - **HEPAP International Benchmarking Report** stresses need to maintain US leadership in microelectronics
- **Description:** Adapt recent AI-in-ASIC developments for FCC latency, power, detector occupancy, and radiation requirements
- **Short term criticality :** leverage and maintain recent US momentum and expertise for AI-in-ASIC R&D and direct for FCC use case
- **Resources: $130k**




| Funding | Resource | Activity |
|---|---|---|
| $60k | 0.15 FTE engineer | AI-in-ASIC hardware codesign based on FCC specifications |
| $60k | 0.6 FTE post doc | FCC specification development and testing of FCC AI-in-ASIC demonstrator |
| $10k | Travel | Sharing results with the community (Int'l FCC/HF, ECFA DRDs, CPAD RDCs) and engineer + physicist collaboration |

# AIM plans for SLAC HFCC Workshop : Dec 19-20

- **Preparing input to ESPP:** Invited talk from each L3 area summarizing (and seeking community input on) **priority R&D directions** for Higgs Factories
- **Organize US-coordinated Detector Design/Optimization "Challenge":**
  - Work with stakeholders to define objectives, benchmark physics processes, simulation datasets, software, and logistics/timeline
    - Reminder on goal of challenge : Lower the barrier to entry and inspire the US community to enhance contribution to **international efforts** for Integrated Detector physics studies
- **Roundtable** with all HFCC L2 areas focused on **cross-cutting issues**, e.g.:
    - Physics studies for Integrated Detector Concepts – especially Software/Computing L2
    - AI/ML in detector systems – especially TDAQ L2
    - Digitization/data simulation for integrated-detector bandwidth – especially TDAQ L2
    - Microelectronics / Integrated Circuit needs sub-detectors – especially Tracker/Calo/Muon L2s

→ Ongoing call for community input: thoughts on funding priorities and/or any other feedback in community Google Doc

# Backup

# HFCC Charge

1. **Physics and technical feasibility studies**, including any associated design and R&D efforts, to **advance various experiment detector concepts** at a future Higgs factory;
2. **Prioritization and stewardship** of the national R&D efforts should funds be identified by DOE and/or NSF;
3. **Development of the pre-project detector R&D scope** that will be required prior to DOE and/or NSF initiating any detector project at a future e+e- collider;
4. Conceptualization of the **software and computing framework** that will be needed to advance physics studies and R&D efforts; and to collect, store, and analyze the large volumes of physics data at future collider experiments;
5. In consultation with DOE and NSF program managers, **develop various funding models** that will be required to support the R&D efforts described in items (3) and (4) above; and
6. **Ensure collaborations** by the U.S. with our partners are cost-effectively carried out to advance the future Higgs factory initiatives. (CPAD, ECFA, DRD, others).

- Prepare the groundwork to respond to the P5 Recommendation 6a: "[Convene a targeted panel to review] the level and nature of US contribution in a specific Higgs factory including an evaluation of the associated schedule, budget, and risks once crucial information becomes available"

AIM "Integrated Detector Concepts" L3 area closely coordinated with

- HFCC Software/Computing
- HFCC Detector Groups
- ongoing work by HFCC partners

# Summary from P5 Costing Exercise

*"HFCC AIM" group has evolved from "Readout/ASICs" in P5 Higgs factory costing exercise [2306.13567]*

- Community survey responses from 4 main labs and 6-10 universities
  a. ~20 scientists, ~50 engineers, ~20 postdocs, ~10 students
- Topics:
  a. AI/ML in ASICs
  b. Monolithic sensor ASICs
  c. High performance ASICs for 4D/5D detectors
  d. IP blocks for 28 nm technology
  e. 3D / hybrid integration
  f. Silicon photonics
  g. Increased data density
  h. Emerging tech including open source design/fab, wireless ctrl/monitoring, automated design/verification
  i. Extreme environments & longevity, such as reliability & fault tolerance, radiation hardness, or cryogenic temperatures

*Historical perspective & US leadership in AIM activities:* ASIC design for HEP experiments

- Microelectronics R&D
- R&D for AI in hardware (GPU, FPGA, ASIC, etc)
- HEP experiment design and construction
- Physics studies for optimization of HEP detector concepts