Fermilab U.S. DEPARTMENT OF ENERGY Office of Science

The FCFD ASIC for Detectors with AC-LGAD Strips

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EIC PDR for Electronics & DAQ

Charge Questions Addressed

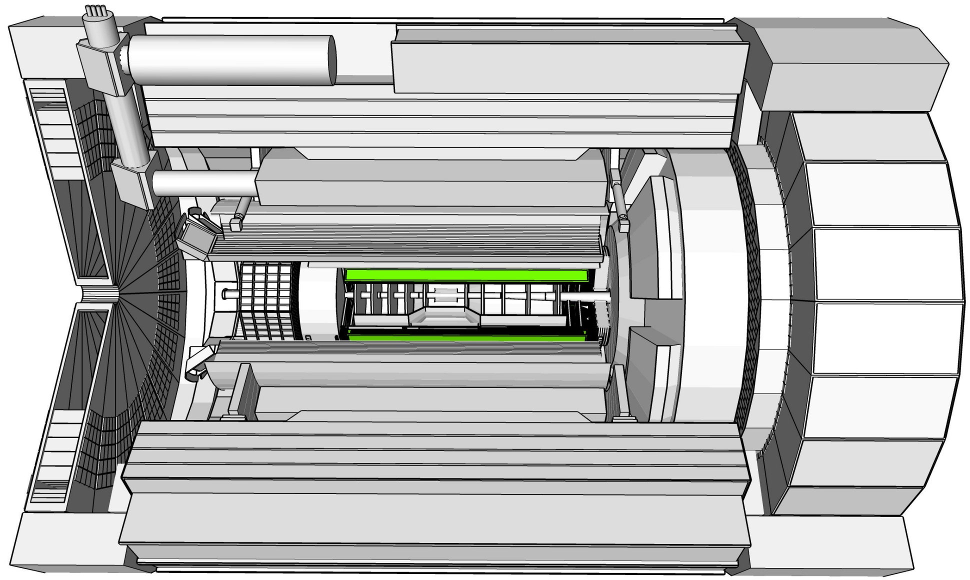
1. Are the technical performance requirements appropriately defined and complete for this stage of the project?
2. Are the plans for the various detector electronics and data acquisition systems appropriately documented and complete for this stage of the project?
3. Are the current plans from front-end electronics to data acquisition for the detector likely to achieve the technical performance requirements, with a low risk for cost increases, schedule delays, and technical problems?
4. Are the schedule assumptions for the fabrication of the various electronics and data acquisition systems and assembly plans reasonable and consistent with the overall detector schedule?
5. Have ESH&Q and QA considerations been adequately incorporated into the plans at their present stage?

Outline

- Documentation status
- Technology for FCFD approach for AC-LGAD time-stamping
- FCFD development history
  - FCFDv0 testing results
  - FCFDv1 development and early results
  - Plans for the next versions
- Summary

Timing for barrel Time-of-Flight detector

Charge #1

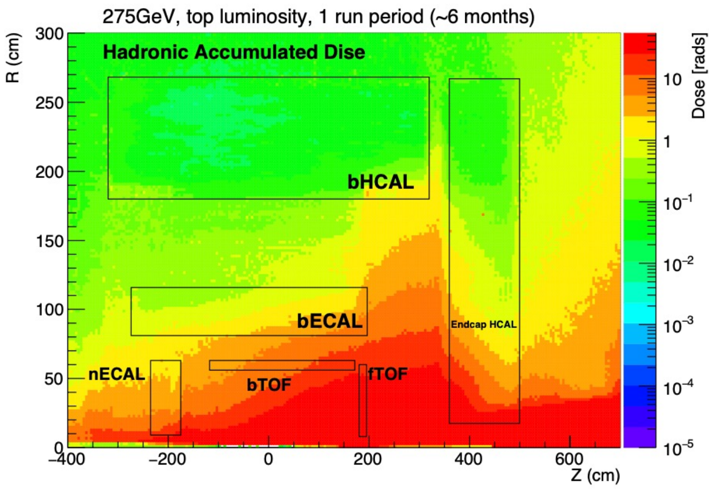


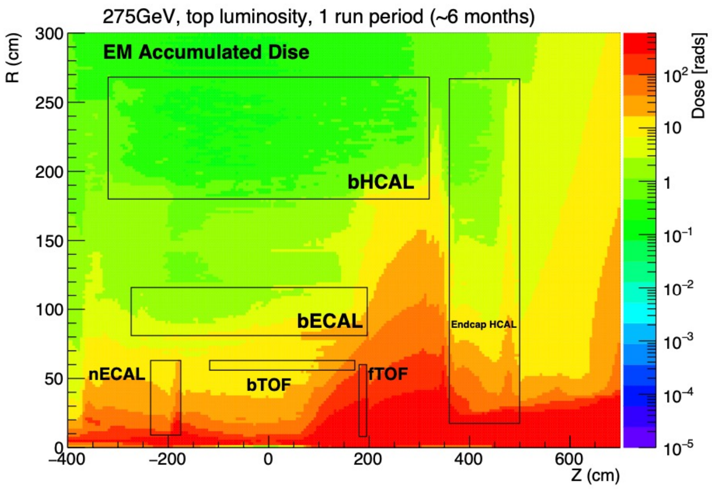
- Focus of this talk is on the development of the readout ASIC for the barrel section of the TOF

Detector	Area	Channel size	Channel number	Time resolution	Spatial resolution	Material budget
Barrel TOF	~10 m^2	0.5mm x 10mm	~2.2 M	35 ps	30 µm in r·φ	0.01 X0
Forward TOF	~1.4 m^2	0.5mm x 0.5mm	~5.6 M	25 ps	30 µm in x and y	0.05 X0

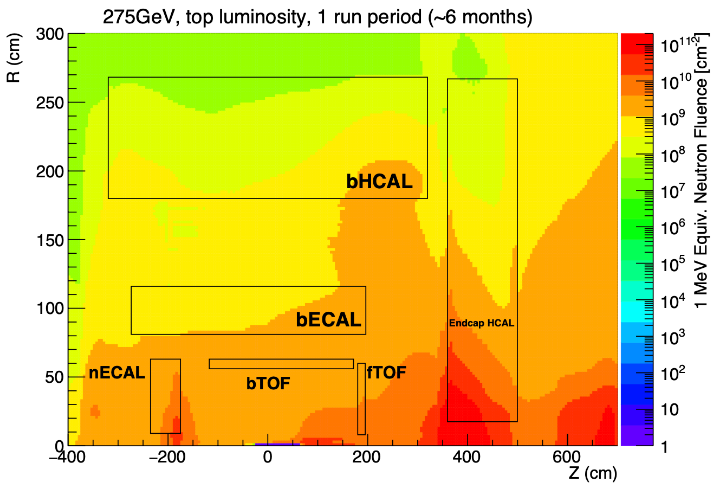
Radiation environment

Charge #1





- Radiation environment after 10 years of running (*plots show the sum of collision and beam + gas*)
  - TID: 1 krad
  - 1 MeV neutron: $3\text{x}10^{10}$ n_{eq}/cm^2



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Documentation status

Charge #2

- Design and results of FCFDv0 summarized in a paper
  - "Design and performance of the Fermilab Constant Fraction Discriminator ASIC", **NIM A** (1056) 2023, p168655
  - Regular presentation at the *"eRD109 Progress Reports - Electronics & DAQ WG"* meetings
- Project Requirements Document
- Project Interfaces Document
- **Under construction**
  - Specifications of AC-LGAD sensors documentation
  - Specifications of the bTOF modules
  - Interfaces with RDO according to specifications documents

Constant Fraction Discriminator ASIC (FCFD)

Charge #3

- A robust fast-timing measurement technique for LGADs
- Achieves the needed performance, especially for low S/N systems, such as LGADs **(NIM A 940 (2019), pp 119-124)**
  - CFD offers significant reduction in noise, as demonstrated in TOFHIR ASIC for CMS barrel timing detector
    - Improvement in the time resolution by x3.5 in TOFHIR
  - CFD-based readout is simple in operation and maintenance
    - No need to maintain the calibration and monitoring system, computing workflows, database maintenance, payloads, etc…
- Power consumption for FCFDv1
  - About 2 mW per channel for the pre-amp and discriminator
  - Estimates for the TDC, SRAM, supporting circuitry to be evaluated

FCFD development history

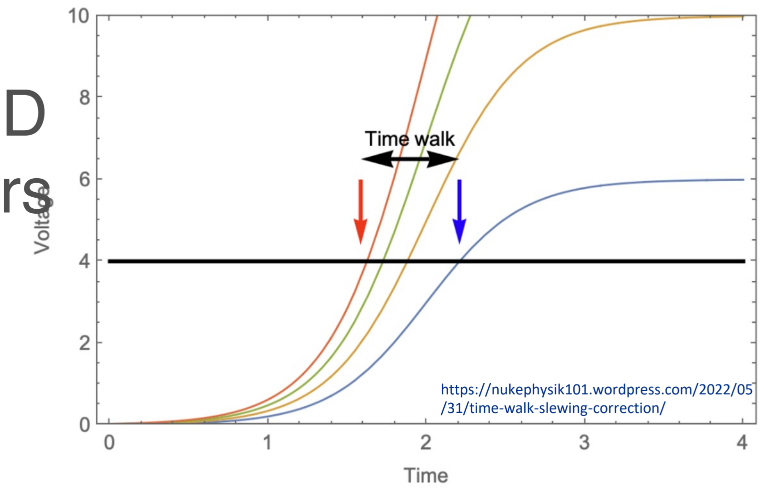
Charge #3

- The first (FCFDv0) version was designed, produced and tested with DC-LGAD sensors
  - Developed in TSMC 65 nm technology node
  - Radiation-hard and extensively characterized technology, widely used in LHC and HL-LHC experiments
  - Excellent performance demonstrated with charge injection, laser and beta source
- The next version (FCFDv1) was optimized with EIC sensor specifications
  - In close collaboration with the EIC detector experts and AC-LGAD developers
  - Specifications for sensors: 1 cm long AC-LGAD, 500 um pitch, 50 um thickness. Estimated capacitance ~5-10 pF

FCFD Readout for Timing Detectors

Charge #3

- Time-walk effect is well known & must be corrected for best performance
- Conventionally addressed with online or offline corrections via some type of LUT
- A hardware-enabled correction via CFD built into the readout ASIC design offers much simpler solution



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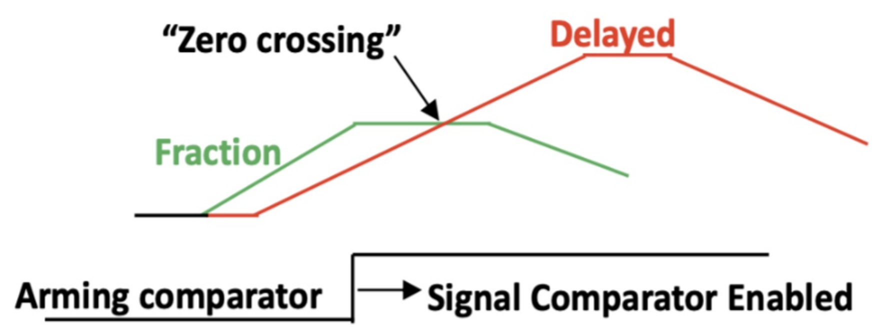
Fermilab CFD Chip Design

Charge #3

- Primary application is (AC-)LGAD sensors for MIP signals
- But can be used for many types of precision timing detectors
- Main features of the CFD are:
  - Integrator & Follower to create the “fraction” signal
  - Comparator for “arming” and timestamping



A. Apresyan et. al, **NIM A 1056, 2023, p168655**
https://doi.org/10.1016/j.nima.2023.168655

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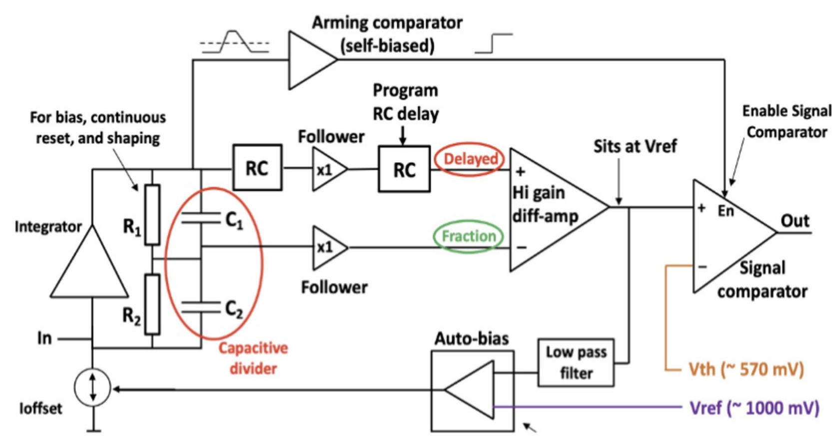

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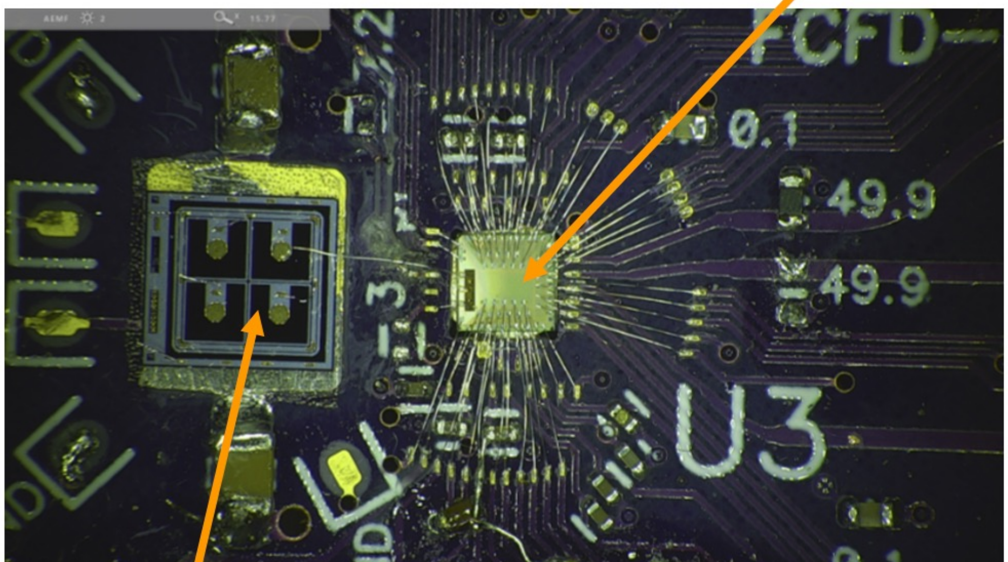
FCFD Chip Prototype v0

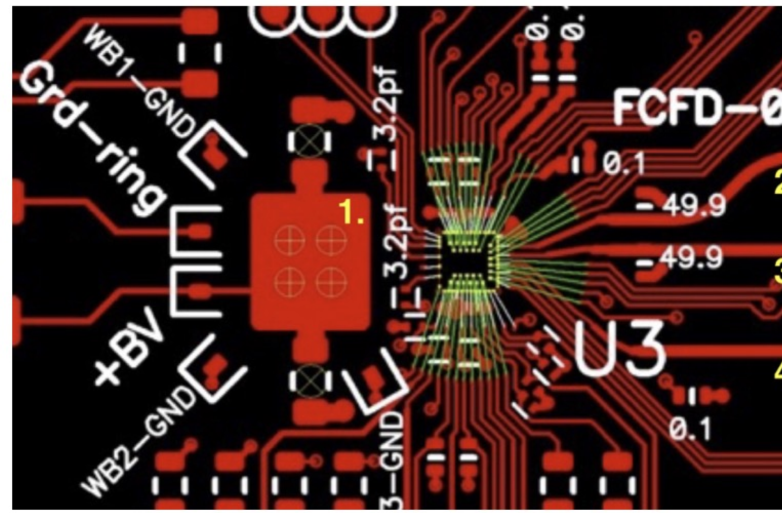
- First prototype designed and fabricated in 2021 & tested in 2022

FCFDv0 ASIC



LGAD Sensor

Schematic Diagram



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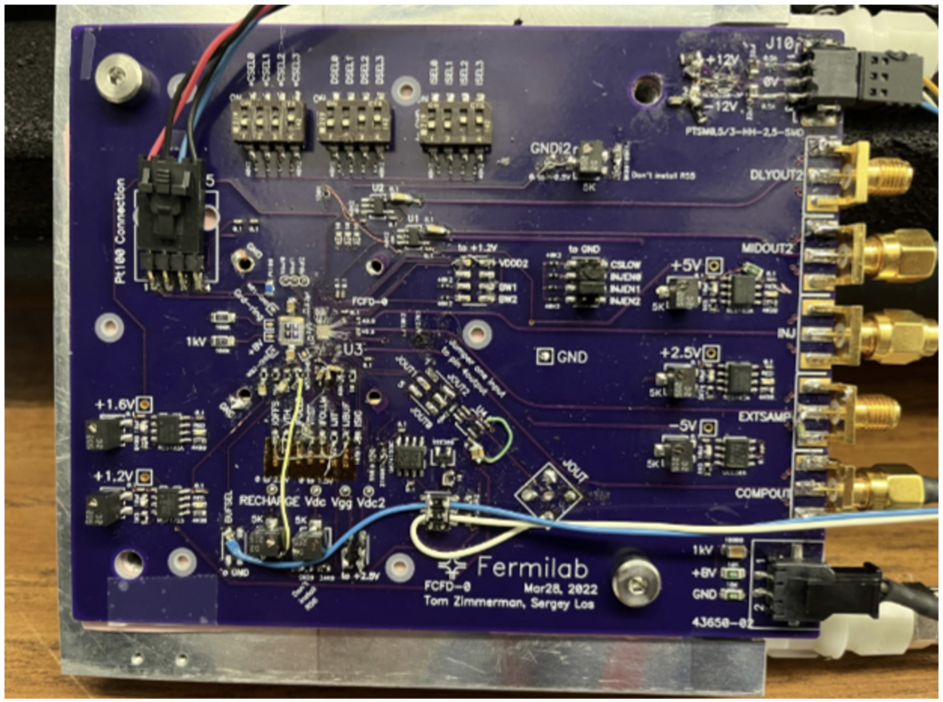


- Full test-board
- Key testing features:
  - Internal charge injection with 3-26 fC dynamic range
- Switch to enable spy on analog signal

Multi-Source Signal Testing Setup

Charge #3

- FCFD v0 performance evaluated using multiple types of signals:
  - Charge-injected signal
  - Picosecond Laser signal
  - Radioactive Source signal
  - Proton Beam signal

Charge Injection

Charge #3

- Inject range of signal sizes from 3-26 fC using built-in mechanism
- Time reference is clock signal used to trigger internal charge injection
- Injected waveforms are based on LGAD signals from simulation (confirmed by past measurements)
- Output waveforms look like this:
  - Spy waveform is small fractional copy of original signal
  - Discriminator waveform is CFD output and used for time-stamping

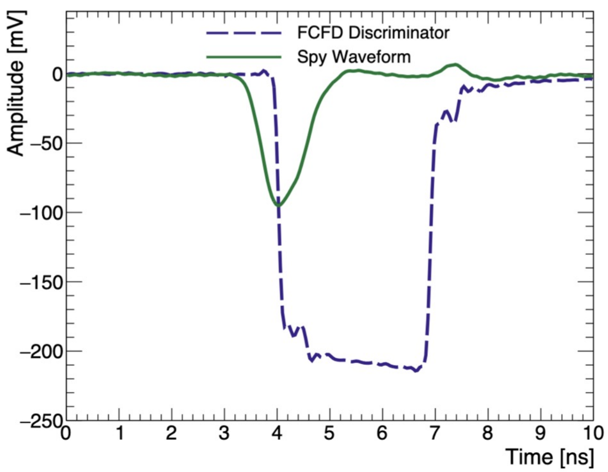
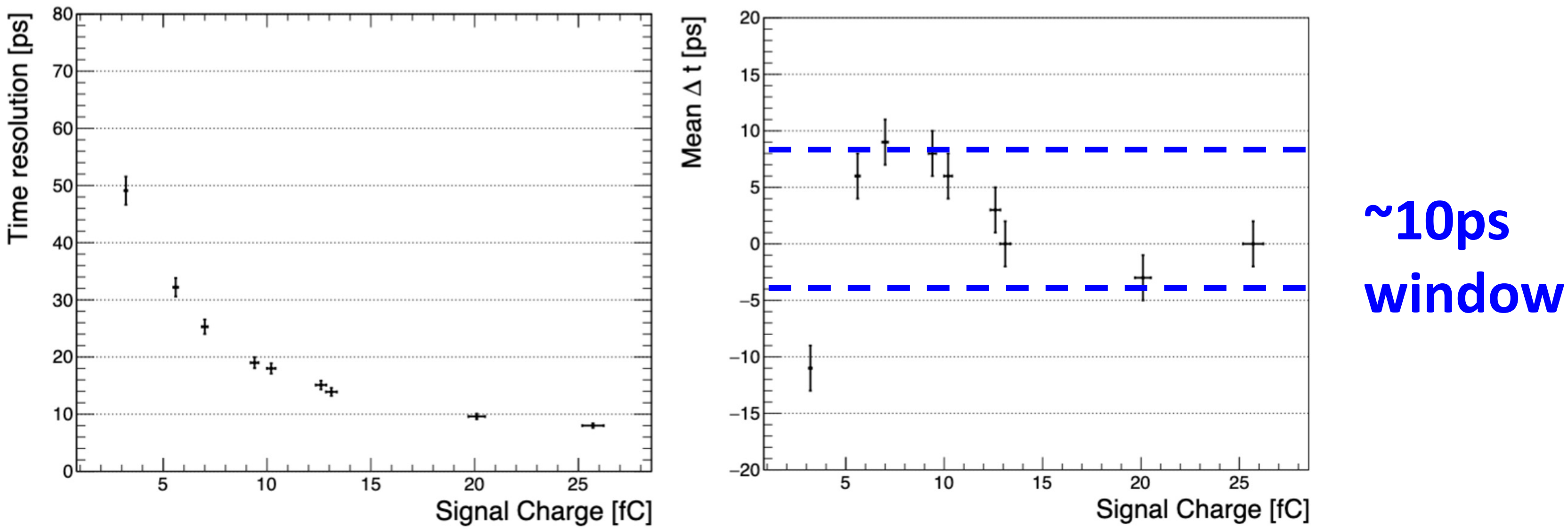


Figure 9: Candidate waveforms of the FCFDv0 discriminator output (blue) and the FCFDv0 input signal spy (green).

Charge Injection

Charge #3

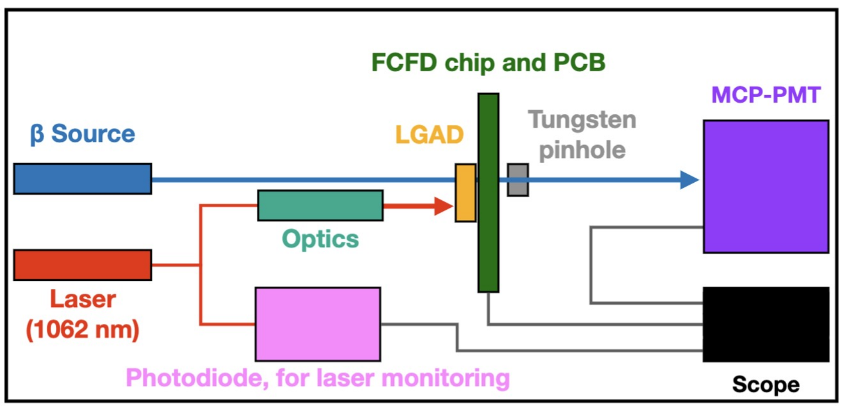
- Time resolution performance as expected
- For largest signal (before saturation) get ~8ps time resolution
- Time walk effect is reduced from 100s of ps to a ~10ps window

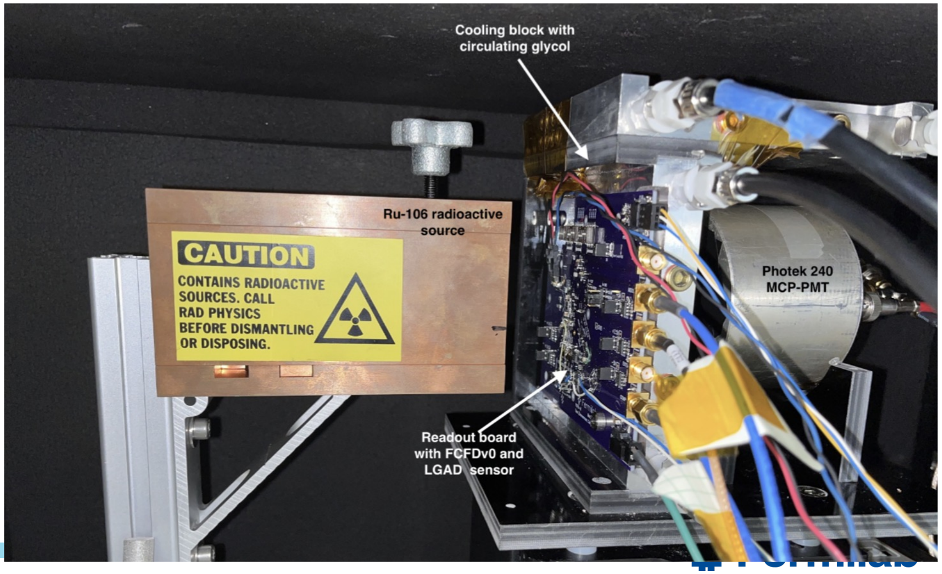


Picosecond Laser & Beta Source Setup

Charge #3

- Dark box with motorized stages, enabling laser injection and beta source
- Picosecond Laser trigger signal serves as time reference
- Collimator and MCP time reference detector ensures straight trajectories: get beta rates of about 2-3Hz at best alignment
- Temperature maintained at 20C by chiller and cooling block

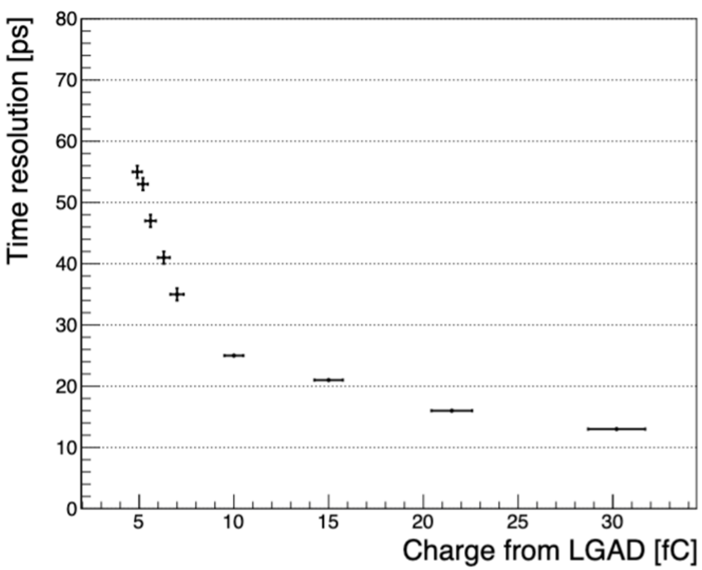




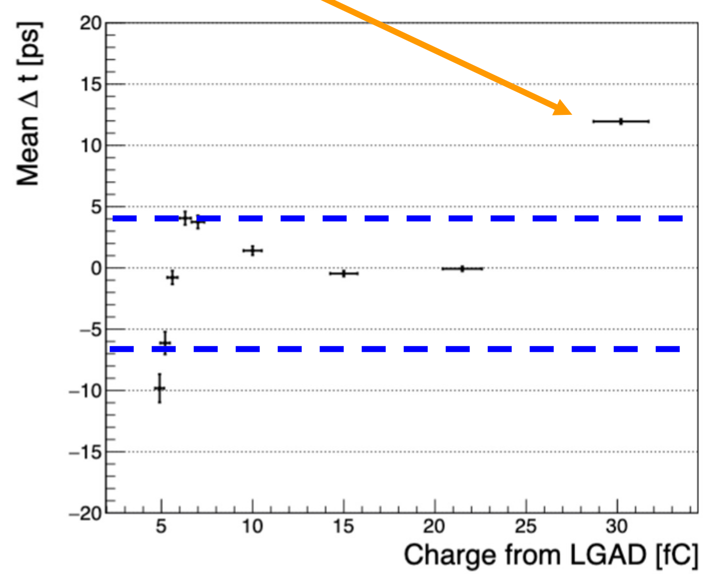
Picosecond Laser Measurements

Charge #3

- Laser measurements confirm similar performance as charge injection



Signal here starts to saturate FCFD v0
Larger dynamic range addressed in next v1 chip



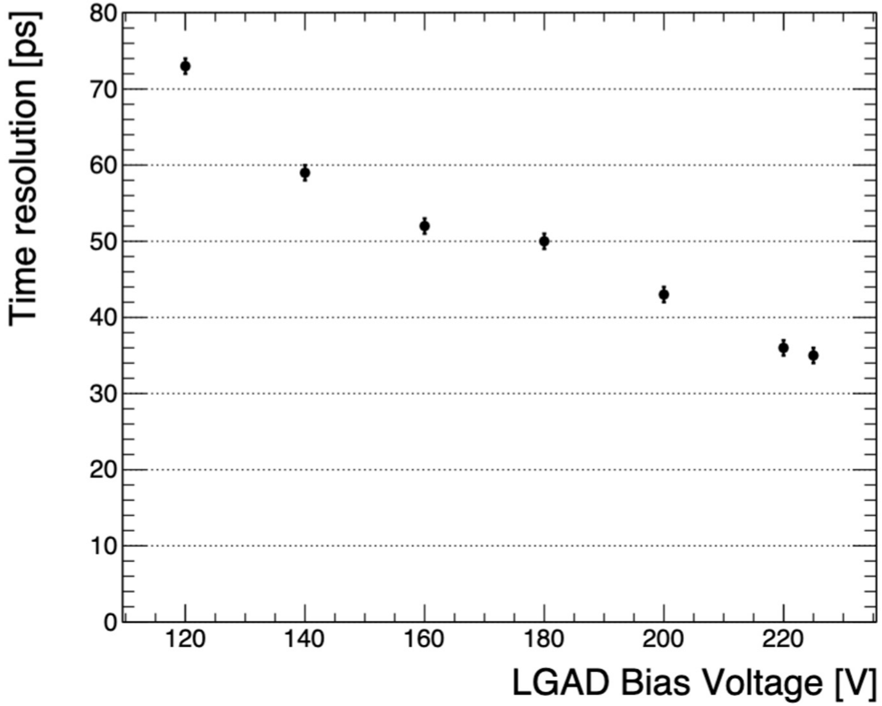
~10ps window

Beta Source Measurements

Charge #3

- Similar performance is also confirmed with beta source

- The measured time resolution is consistent with a 8-10 ps contribution from the CFD chip, accounting for time jitter of LGAD sensor itself and imperfect collimator,

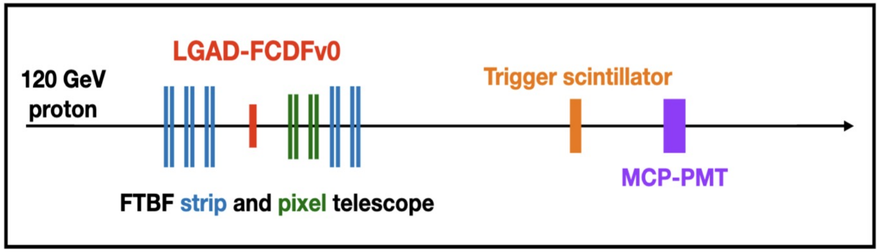


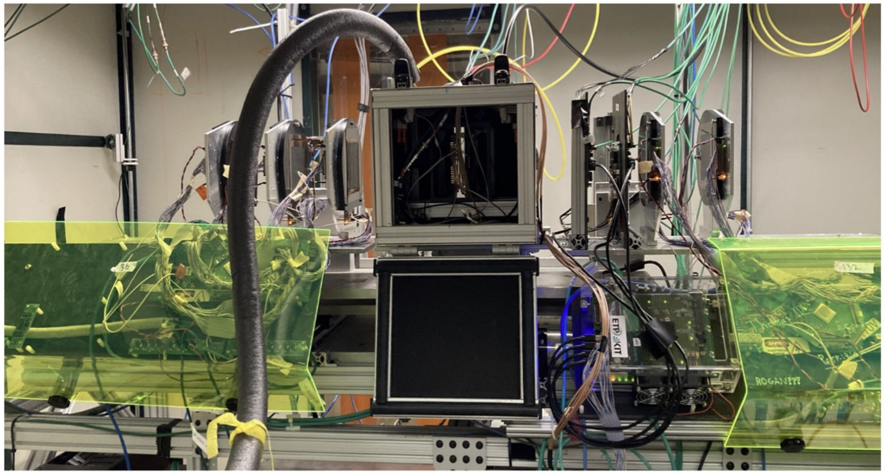
Proton Beam Measurements

Charge #3

- Use Fermilab Testbeam Facility to test CFD chip with 120 GeV protons

- MCP-PMT used as time reference detector
- Temperature maintained at 20C
- Tracking telescope used to measure hit positions and efficiency

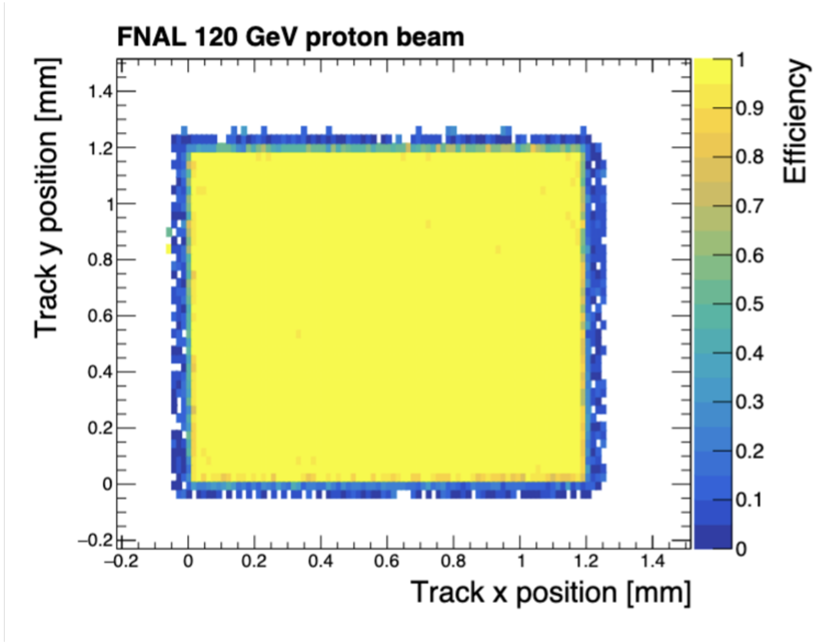




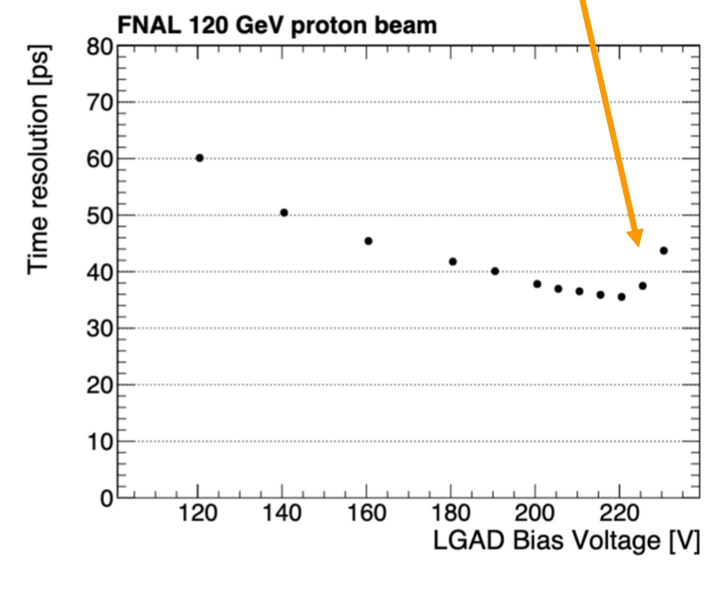
Proton Beam Measurements

Charge #3

- 100% Efficiency is maintained over full LGAD pixel sensor area
- Time resolution performance consistent with Beta Source measurement



Saturation here again
Addressed with v1 chip



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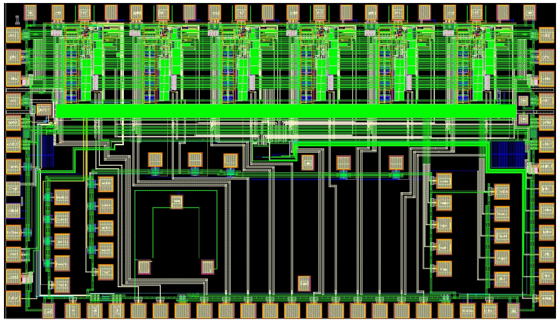
FCFDv1 status

Charge #3

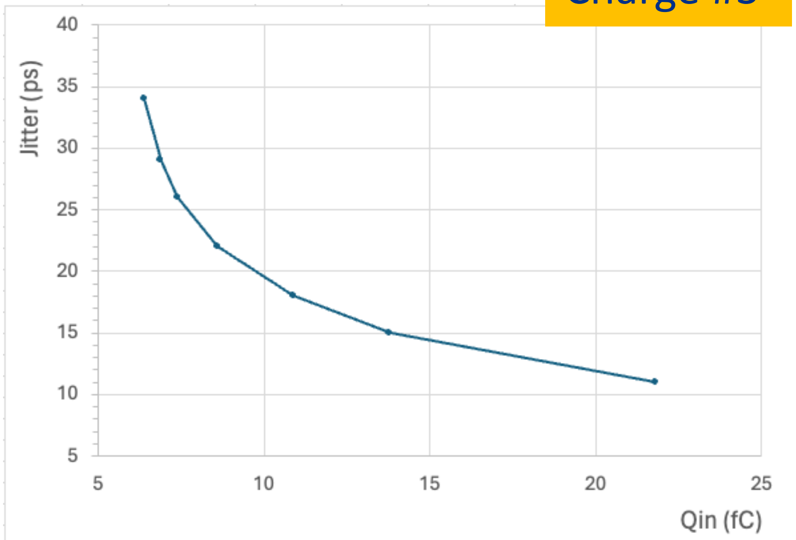
- Six-channel FCFDv1 submitted Sep. 2023
  - Wider dynamic range,
  - Sensitivity to smaller signals
  - Includes signal amplitude measurement for position measurement
- Received the chip back from TSMC in Jan 2024
  - Testing on bench started immediately
  - Preparations for test beam in Spring 2024



Status and Next plans

Charge #3

- FCFDv1 chip is now being tested
  - Measurements with internal charge injections performed with an LGAD-like signal being injected.
  - With input capacitance ~3.5 pF we achieve around 11 ps time resolution
  - The analog output works linearly over the range of input charge from 7 fC to 60 fC, the discriminator flip time output stays constant within around 10 pS



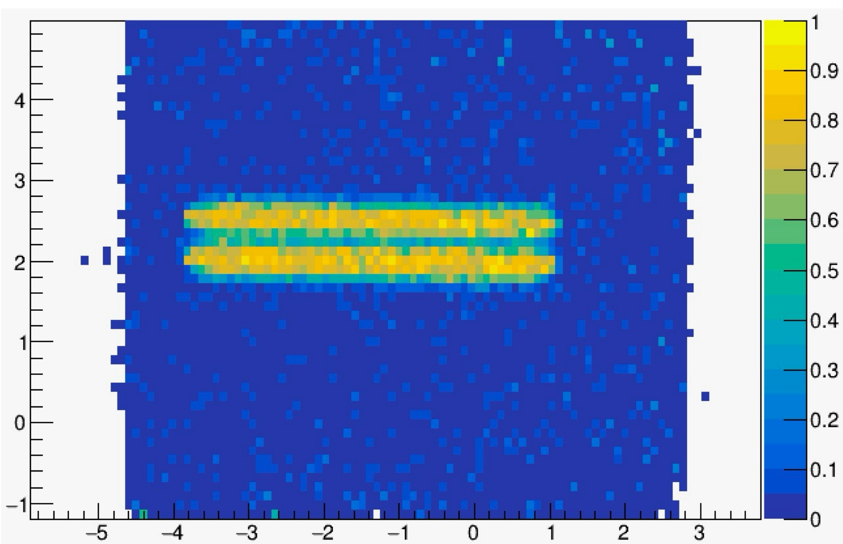
Jitter measurements with 3.5 pf input capacitance and charge injection

- Our measurements of the AC-LGAD strip sensors showed the complex CR-network which complicates operation of the ASIC
  - Additionally, the capacitance for some of the sensors is a lot larger than we originally specified
  - Hamamatsu 5 mm E-type strip sensors behave the best so far, and we have adapted the readout board for this sensor

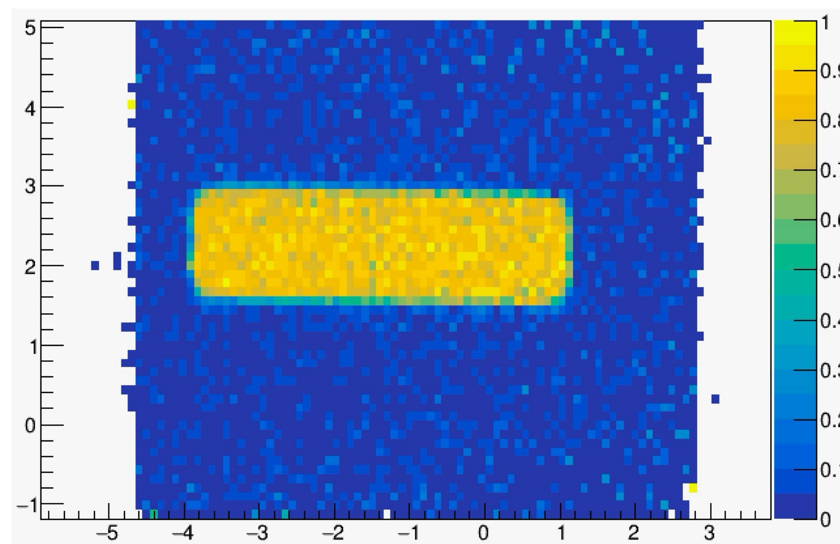
FCFDv1 test beam results

Charge #3

- Testing in the Fermilab beam this week
  - Connected to a 5 mm strip AC-LGAD sensor, 500 µm pitch, 50 µm thickness
  - Main goals to measure timing and position resolution with particles
- Optimizing the readout board grounding, power supplies, noise
  - Two-strip efficiency demonstrated to be 100%
  - Continuing the characterization of the ASIC and timing performance, results soon



Efficiency with 2-strip



Two-strip efficiency

Development plans in 2024 and 2025

Charge #4

- Complete the testing of FCFDv1
  - Characterize the system performance for timing and position measurements using AC-LGAD strip-sensors
  - Early tests showed new features of AC-LGAD sensors that impact performance
  - Would like to re-optimize the chip with the final-spec AC-LGAD parameters as tested with FCFDv1 version, for a minor revision FCFDv1.1
- Next focus on the full chip: full-size FCFD v2 end of 2025
  - Finalize the geometry and sensor key parameters (strip length, sheet resistance and thickness)
  - Complete ASIC with readout that would interface with the EIC experimental DAQ
  - Implement the interfaces with RDO
- The final ASIC (v3) to be produced in FY26

QA/QC plans

Charge #5

- Prior to the production of the final version, several prototype rounds are planned to validate the design
  - The chip will be tested standalone to verify performance
  - Testing with prototype modules connected to the RDO to validate the system design
- During production chips will be tested on-wafer to produce verified good dies, which will be then passed to module assembly teams
  - The procedure for module assembly and quality control will be developed during this period.
  - Module components will need to be tested prior to the final assembly.
  - These criteria will include tests to verify that the ASICs, sensors, hybrids are all functional before assembling the module

Summary

- Described the specifications of the barrel TOF AC-LGAD readout system
  - First prototype ASICs have been fabricated and tested
- A reference plan for the FCFD ASIC has been developed
  - The resource loaded schedule will be refined in the coming months