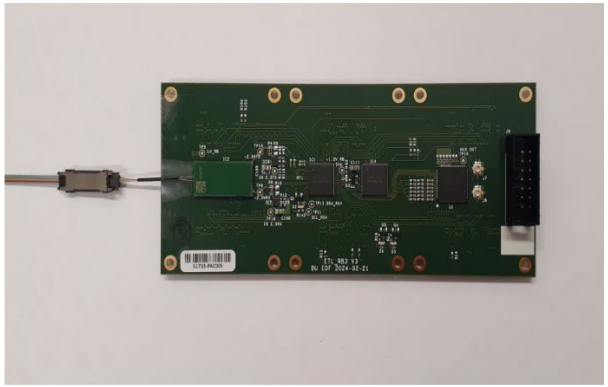
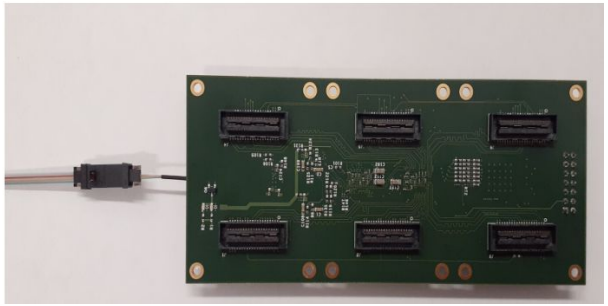
Change to lpGBT (thoughts)

- Conceptual RDO design very similar to CMS ETL RB ⇒
  - a major advantage, IMHO!
  - already very advanced, almost finished!
- FTOF: 1 lpGBT & 1 VTRX+
  - 1 downlink @ 2.56 Gbs
  - 1 uplink @ 5Gbs
  - up to 28 ASICs
- BTOF: 3 lpGBTs & 1 VTRX+
  - 1 lpGBT is in Transceiver Mode (“Master”)
    - 1 downlink @ 2.56 Gbs
    - 1 uplink @ 5 Gbs
  - 2 lpGBTs in Transmission Mode (TX-only) (“Slaves”)
    - 1 uplink @ 5 Gbs each
    - controlled via Master’s I2C
  - ~22 ASICs per lpGBT (need 64)
- FF Detectors (B0, Roman Pots, others?)
  - I assume 1 lpGBT is going to be enough so similar to FTOF

RB v3 (with the MUX64 ASIC instead of SCA ASIC), April 2024





CMS ETL Design Shown with 2 lpGBTs (1 Master, 1 Slave) & 1 VTRX+

Caveats

- Tha “40 MHz” clock issue
  - this is under discussion in the Electronics & DAQ Group but it seems it will be OK (William, Jeff, TL)
    - NOTE: most of our ASICs work off a 40 MHz clock internally anyway
- Clock Jitter
  - some preliminary measurements (Jo) have shown <5ps but I want to repeat them because I am not sure where the clock was measured (BNL?)
  - phase stability → also needs verification (William, BNL?)
  - we might still need a clock cleaner!?
- Streaming?
  - this needs more understanding of the lpGBT but I don’t see a show-stopper right now
  - needs verification! (TL?)
- Fiber data formats from the DAM (and DAQ) now need to be lpGBT’s ⇒ we have no freedom
  - doesn’t seem to be a showstopper but needs deeper, more careful thought (TL, Jeff, …)
    - and experience with an actual lpGBT
- 3x increase in DAM inputs for BTOF is a $ problem
  - however, we could address this with a simple/cheap fiber aggregator board which will be housed outside of the radiation area (SFP, FPGA)
    - to be designed (TL, Jeff, Mike?, Tim?, others??…)
    - e.g. 8 fibers from lpGBT to 1 fiber to DAM
  - can also act as a fiber protocol translator from DAM to lpGBT?
  - can also be a “normal RDO” for other detectors by replacing SFP receivers with copper connectors ⇒ all-in-one board
  - TBD

Proposal (near term)

- send 1 ETL RB with 1 ETROC module to Zagreb (me) soon
  - develop DAM-like receiver FW in Zagreb which connects to the ETL RB over fiber and controls/talks to lpGBT and “a few” ETROCs
  - Why?
    - familiarize us (well, me :-)) with lpGBT protocols
    - configure lpGBT, both Master & Slave (important)
    - configure ETROC via lpGBT
    - prepare FW for jitter measurements
    - develop FW for streaming compatible with the EPIC DAQ Requirements
    - use it to verify all what we need: jitter measurement, streaming, data format issues
- send 2nd pair to BNL for jitter (and other?) measurements once basic FW in place
  - replicate the Zg setup
  - BTW, Zg setup would use the usual STAR Receiver Board (“TEF”) which is a PCIe based fiber board acting as a DAM (FELIX)
- BTW, “Zagreb” and “me” can be someone else → let’s discuss

ppRDO?

- it becomes a resource drag on us if we won't use FPGA based readout
- I propose we wrap up the basic jitter measurements to complete that part in eRDO109 and drop it
- Or, we can continue using it as prototype for the Fiber Aggregator Board?
- Or, we can continue using it as an RDO for other detectors (e.g. Forward ECAL)?
- Thoughts??