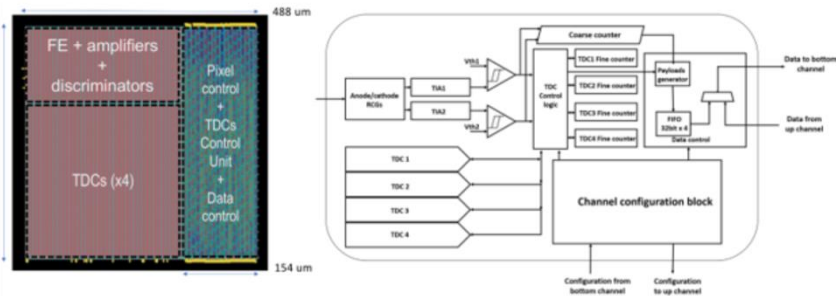


## Meeting with Project on Friday 27<sup>th</sup>

Envelope: flange before and after dRICH  
action: minimize the flange outfit

increase aerogel radius to create an overlap with hpDIRC  
action: check services

**ALCOR** The ALCOR ASIC is currently under development specifically for the readout of the dRICH detector with SiPMs due to its single photo-electron sensitivity requirement. The ALCOR design includes trans-impedance amplification (TIA) with regulated common gate (RCG) bias for low noise, inhibit or shutter operation to limit contribution from dark-rate SiPM noise and TDCs to allow for single-photon tagging or time and charge digitization. The shutter function is a critical aspect of this ASIC and it is programmable for width and latency. The ALCOR Die and block diagram are shown in figure 8.164 and its specifications are summarized in figure 8.165.



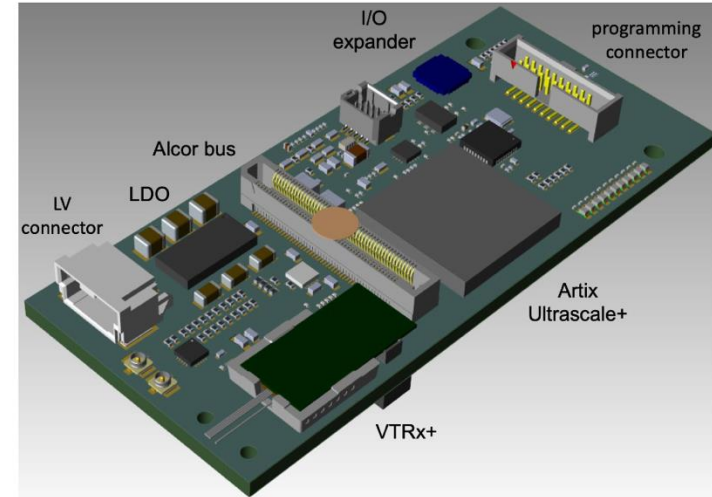
**Figure 8.164:** ALCOR Si Die (left) and block diagram

Function	Digitization from SiPMs with 1 p.e. sensitivity
Mode	Single-photon tagging or time and charge
Tech Node	110 nm CMOS
Channels	64 (8x8), dual polarity
C <sub>in</sub>	<1 nF
Digitization	25 ps TDCs, TOA + TOT; Timing <100 ps
Shutter	Width: 1 – 2 ns, programmable latency
Input Rate	<5 MHz
Clock	39.4 MHz operation from BX 98.5 MHz
Links	640 Mbps LVDS, SPI configuration
Power	12 mW/ch
Package	BGA
Rad Tolerance	Radiation hard

**Figure 8.165:** ALCOR Key Specifications

**dRICH RDO** The dRICH RDO is part of the dRICH Photo Detector Unit PDU (see section ??, 1248 PDUs will serve the dRICH). It provides read-out of four 64-channel ALCOR ASIC, installed each on a separate FEB. The space constraints are particularly demanding: the total RDO area is  $40 \times 90 \text{ mm}^2$  - quite similar to a credit card - requiring a devoted design, given the high integration of data buses and services within the PDU. The FPGA providing readout of the ALCOR is an AMD Artix Ultrascale+ AU15P-SBVB484, complemented by a PolarFire FLASH-based FPGA MPF050T-

FC5G325. The latter will support remote programming and continuous scrubbing of configuration bits of the SRAM-based AMD FPGA, to protect against SEU. Given the space constraints and the need to curb power consumption (total RDO power is expected  $\approx 4 \text{ W}$ ) the CERN-developed VTRX+ optical transceiver has been selected, directly connected to the AMD FPGA SERDES. The maximum throughput per link (reached at maximum radiation damage before annealing) is foreseen not exceeding 2 Gbps, safely within VTRX+ specifications. The ALCOR will be read out at 394 MHz, with a clock multiplier and jitter-attenuator (Skyworks Si5326) deriving this clock from the reconstructed EIC clock. A Microchip microcontroller provides power management and acts as watchdog against SEL. The first prototype of this card is under production and will be intensively tested during 2025, including irradiation tests. A 3D-rendering of the card is shown in Fig. 8.168.



**Figure 8.168:** 3D model of dRICH RDO

**Firmware Trigger** One example of the operation of the protocol is in the firmware trigger to be implemented to reduce dRICH noise. It's important to note that the the firmware trigger under discussion is not (or not necessarily) a global trigger that would remove full events from the readout of the ePIC detector. Instead, this trigger is expected to affect only the data from particular detectors with unusually high data volumes. In this example, the dRICH.

The path of the commands sent is show in figure 8.171. Data arrives at DAM boards with 10us from digitization. It is stored in the DAM boards. After 10us FPGA based algorithms provide a

description of the data (for example number of hits above a specified threshold) from each fHCAL DAM board. This information is encoded into 64 bits and sent to the GTU which aggregates data from fHCAL DAM boards and sends the keep/drop bunch bit to the dRICH DAM boards. The dRICH DAM boards drop or transmit data based upon this message. The decision comes after a fixed latency of about 11us which is very small compared to the buffering available on the DAM board.

Note that a similar approach can be implemented with a hardware signal into the GTU. In this case a fixed delay is applied to the hardware signal, but the decision mechanism uses the same data path.

**dRICH data algorithms** There are also additional schemes for implementing dRICH data reduction using only dRICH data or aggregated data from different sub-detectors. This is currently under investigation by the dRICH groups at INFN. One possibility would be to perform such reduction on the network of interconnected dRICH DAMS using the APEIRON framework [59] which implements a multi FPGA ML algorithm with deterministic time. The results of this calculation are transmitted to the GTU in the same manner as in the previous firmware trigger. The DAM buffering capacity is exploited in this scheme. Another possibility is to use instead, Online Data Filter algorithms in the servers receiving the aggregated data (see Fig. 8.150), exploiting xPU resources. Given the noise rate in the dRICH will increase with the radiation damage (see section ??), this will provide an opportunity to develop and test carefully such systems

