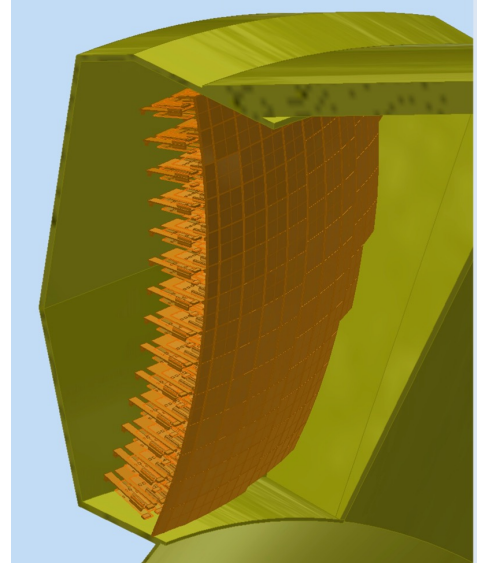


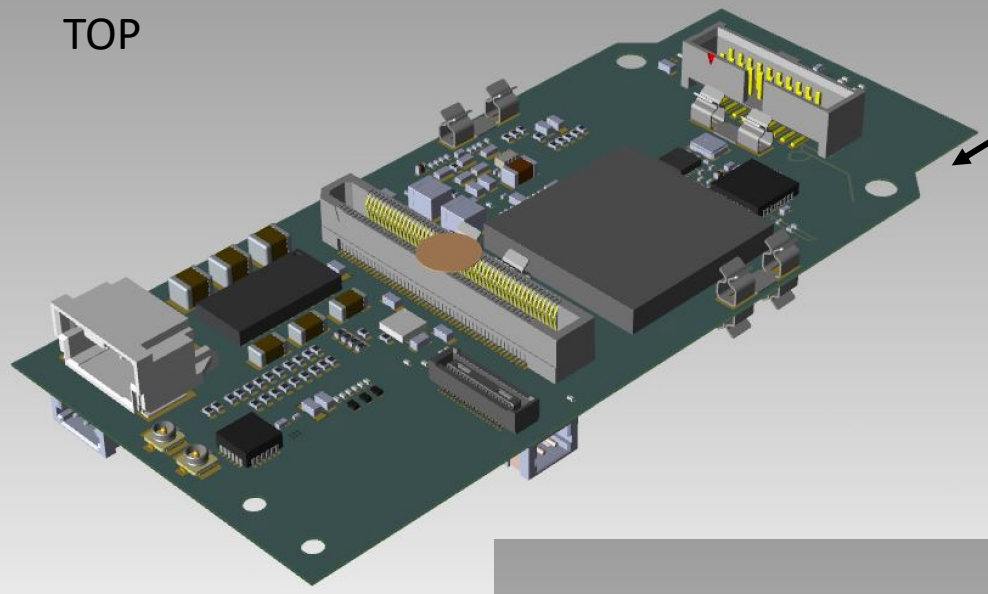
Status of dRICH RDO

INFN Bologna team
P. Antonioli, D. Falchieri, S. Geminiani, L. Rignanese,G. Torromeo

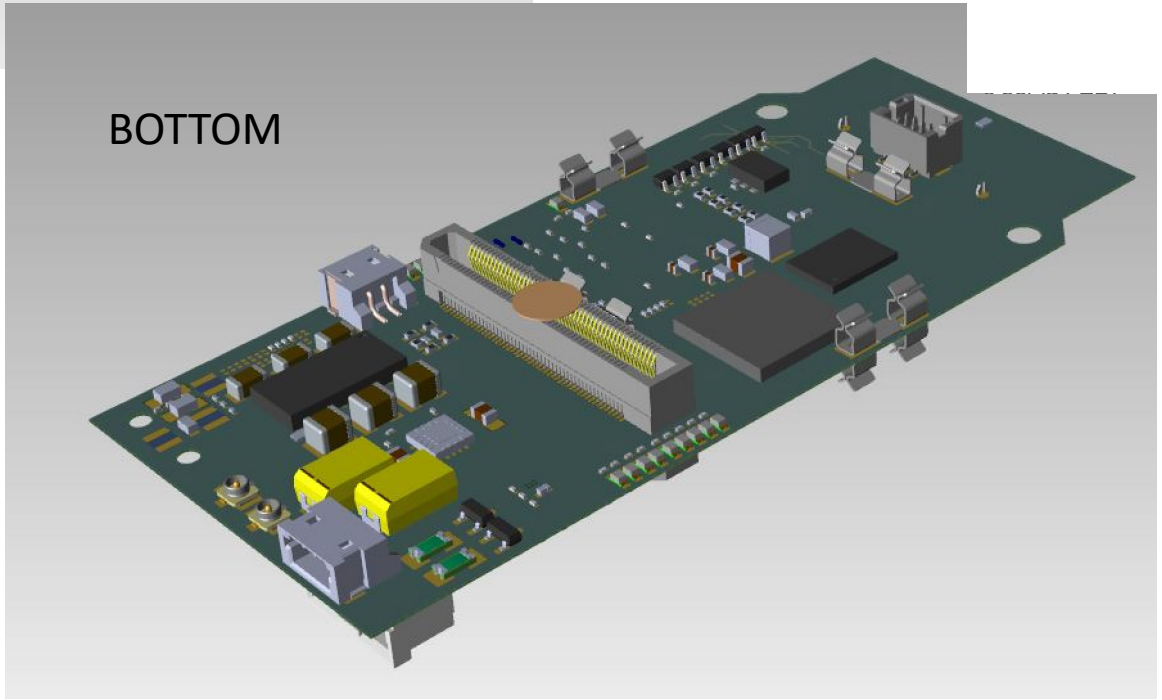
October 3rd, 2024

- extensive presentation given at ePIC/EICUG meeting this Summer by D. Falchieri
- news:
  - finalization of placement and many details (here some reported)
  - procurement on-going
  - planning irradiation tests of key components

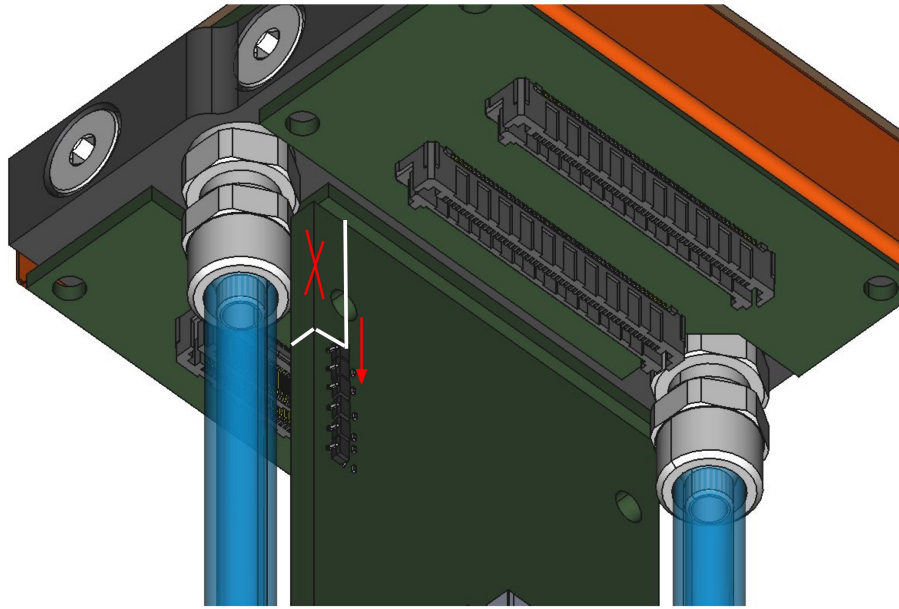
TOP

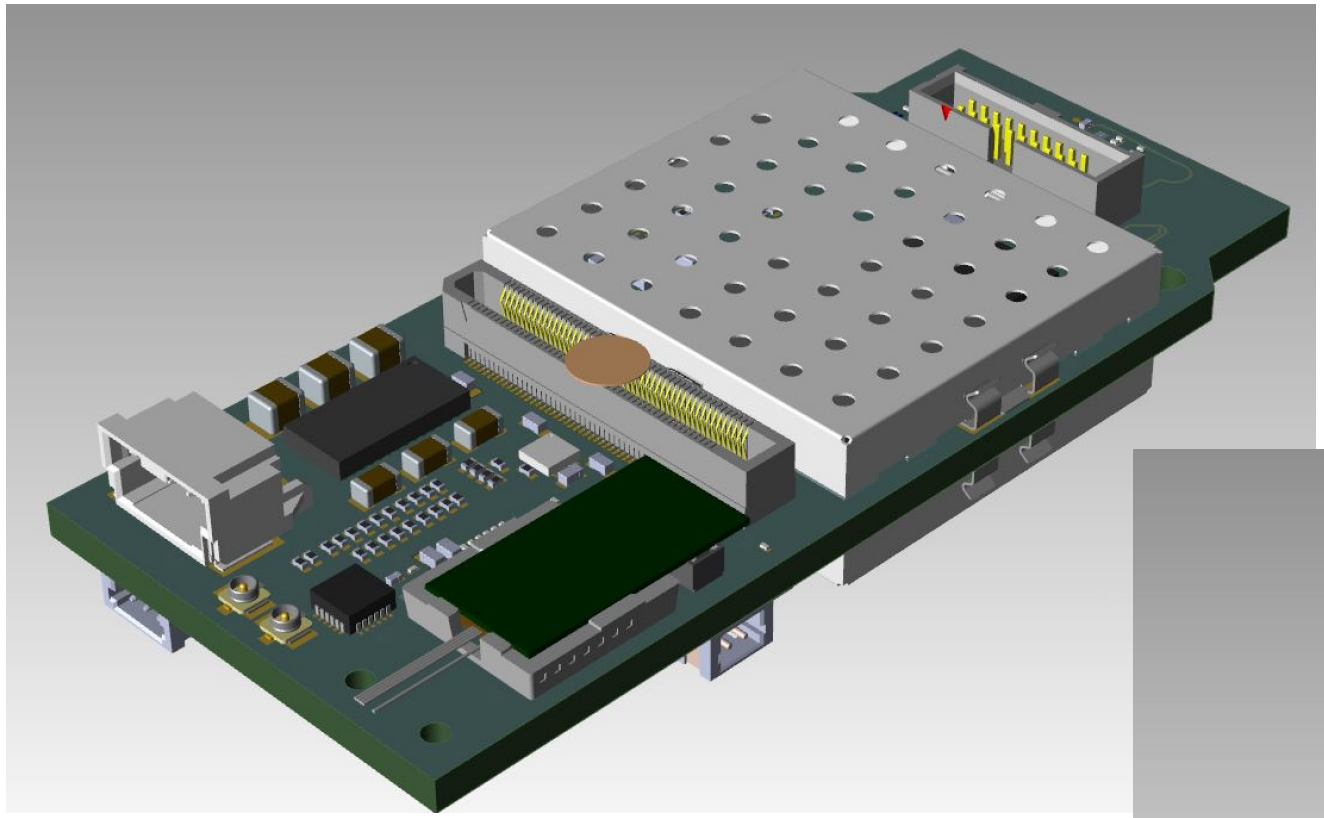


BOTTOM

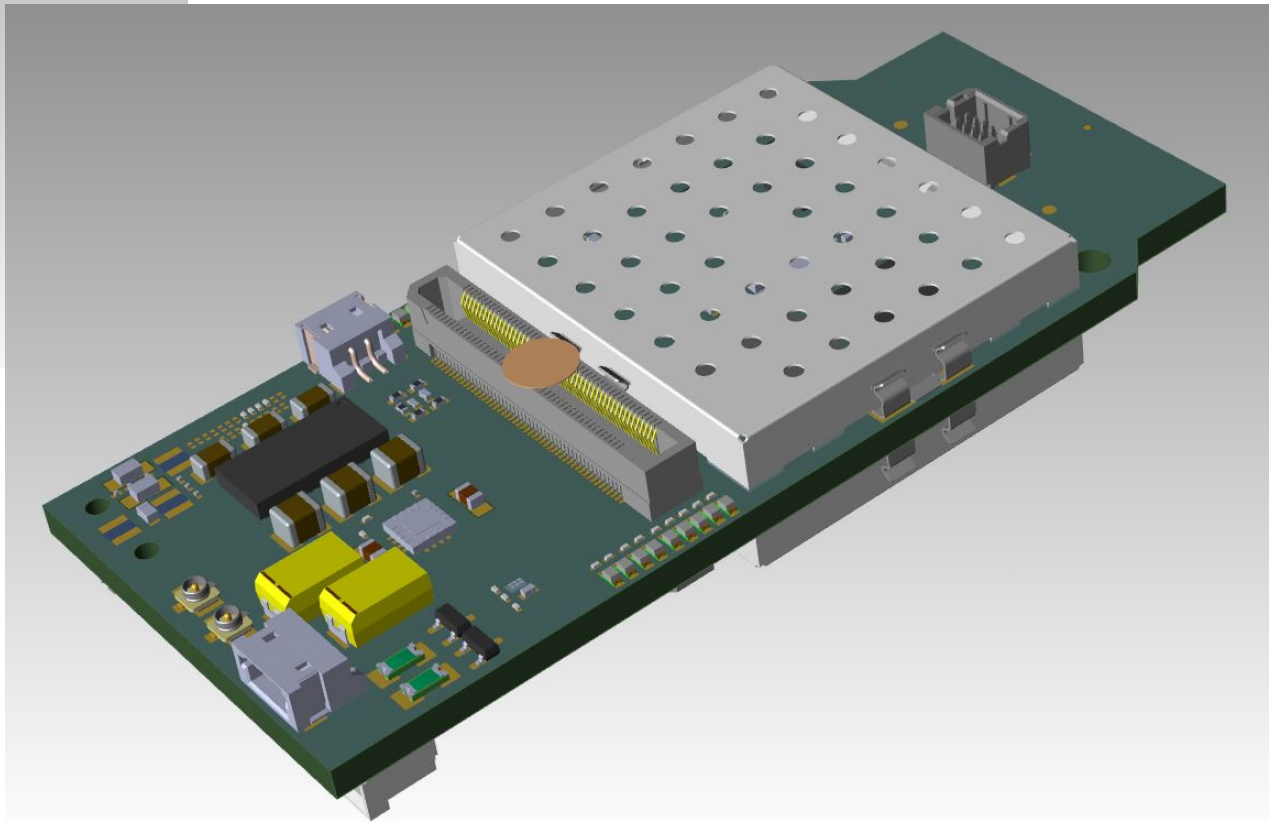


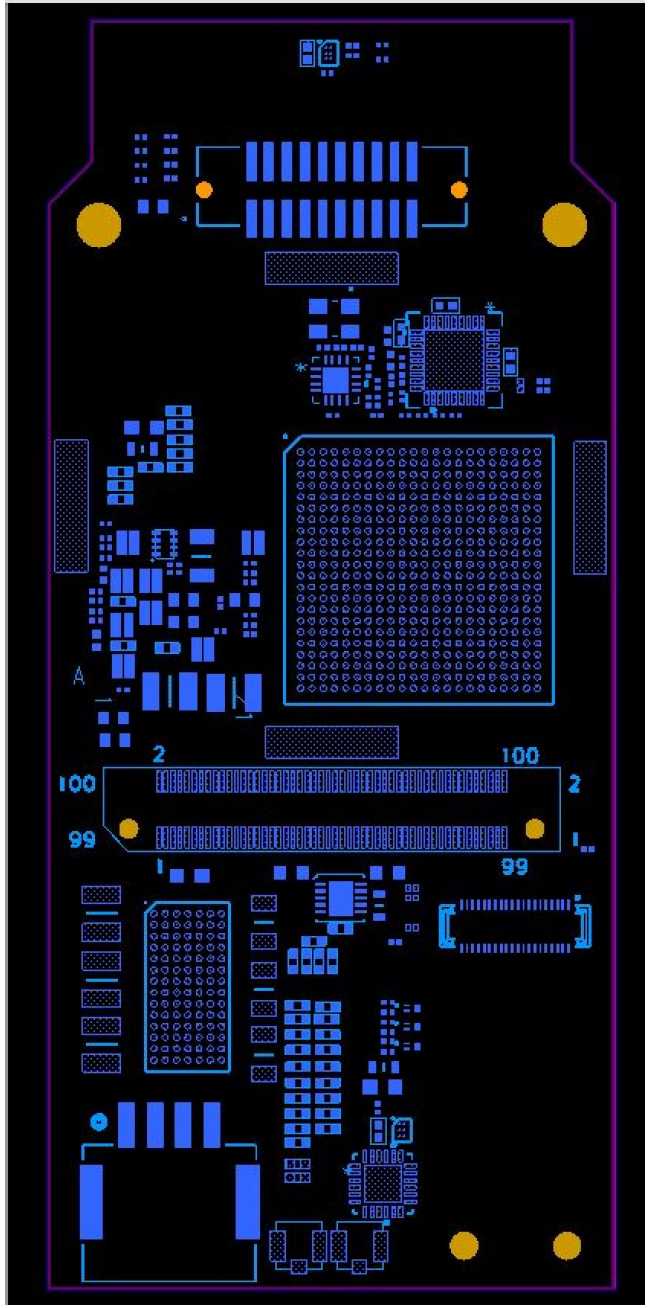
modified shape to allow space in dRICH PDU of cooling cables

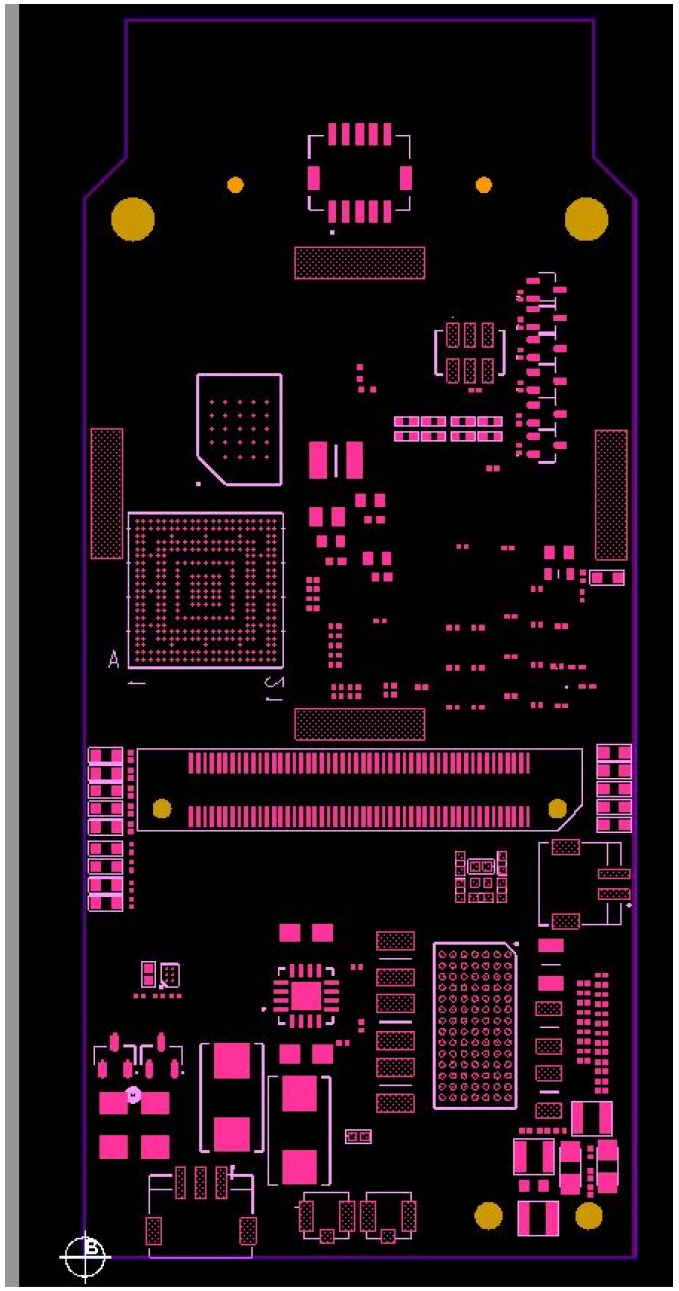




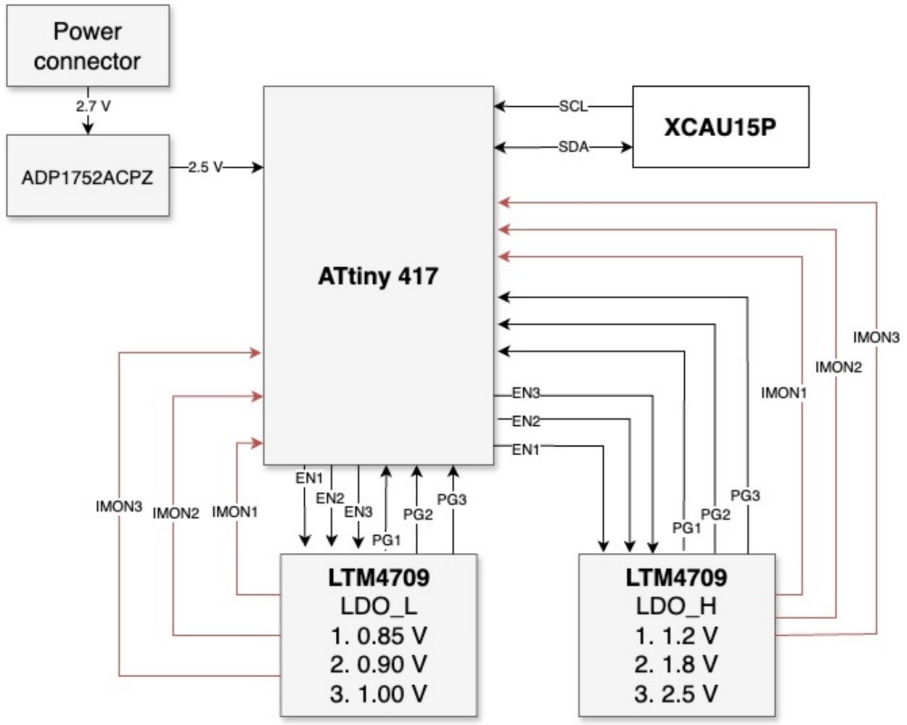
layout modified to allow possibility to mount cages (over FPGA) to shield EMI emission (to be tested real effectiveness/need but layout allows for that)







Plus many details ”fixed” in particular:
- connectors for programming
- moved to ATtiny417 for better control of all voltages: not only “Power Good” signals provided by LDO, but we will monitor also currents



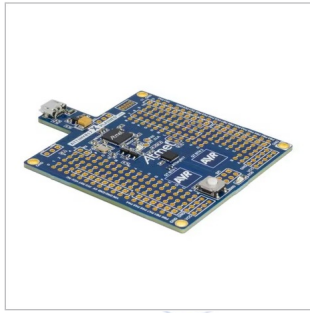
ATtiny417:

Product Selection Guide

Datasheet

Irradiation tests

- realistically dRICH RDO will be available January 2025
- scheduled irradiation session at Trento next 12-14 December
- plan to test following components irradiating evaluation boards available on the market
  1. LDO: LTM4709
  2. ATtiny417: https://www.microchip.com/en-us/development-tool/attiny817-xmini
  3. Si5326: https://www.mouser.it/datasheet/2/472/Si5325-2507576.pdf
  4. Xilinx AXAU15 via evb from ALINX https://www.en.alinx.com/Product/FPGA-Development-Boards/Artix-UltraScale-plus/AXAU15.htm



DUT	Test/what we want to learn
LTM4709	SEL, output voltages stability under irradiation, TID test
ATtiny417	SEL, TID, check programming
Si5326	SEL, SEU (in programmed registers), clock stability under irradiation, TID test
AUX15	check existing literature on SEU (conf. bits + SEU in RAM + SEU in flip-flops)

Milestones check

- Design and realisation of a specific ePIC RDO card prototype, housing a FPGA, LDO, optical transceiver and I/O and LV power connections to provide the read-out to four ALCOR v3 ASIC. A high degree of integration is foreseen between the RDO card and the 4 FEBs that will house each an ALCOR64 v3 chip.

Milestone scheduled for October 2024.

Order will be placed by October, however we will not have in hands - realistically – the card up to January 2025

The high degree of integration with FEB and PDU design was a challenge with respect to requirements and - overall – constraints specifications. The card will be however, available through all 2025 for intensive tests in preparation of final TDR.