

# ALCOR - dRICH Readout

Fabio Cossio on behalf of the ALCOR group  
INFN Torino

EPIC Electronics & DAQ WG meeting  
eRD109 Monthly Progress Reports

03.10.2024

# ALCOR irradiation tests

SEU/SEL and TID tests at Centro of Proton-Therapy in Trento with ALCOR v2.1 (July 2024)

- Beam: 100 MeV proton
- Intensity: 10 - 100 nA
- Runs: typically 600 s
- Fluence collected per run:  $10^{11}$  -  $10^{12}$  p/cm<sup>2</sup>

**TID steps:** 0, 47, 163, 328, 436 krad → Perform **TDC** and **VTH** scans

- **Total TID: 436 krad**
- **Total fluence:  $4.64 \cdot 10^{12}$  p/cm<sup>2</sup>**



# Other requirements: radiation tolerance



The dRICH-PDUs are in a moderately hostile radiation environment

- $\Phi$  (p+n > 20 MeV) = 200 Hz/cm<sup>2</sup>
  - TID  $\cong$  650 rad (for 1000 fb<sup>-1</sup>) < 1 krad
- } note these values include a safety factor 5

## SEU-SEL

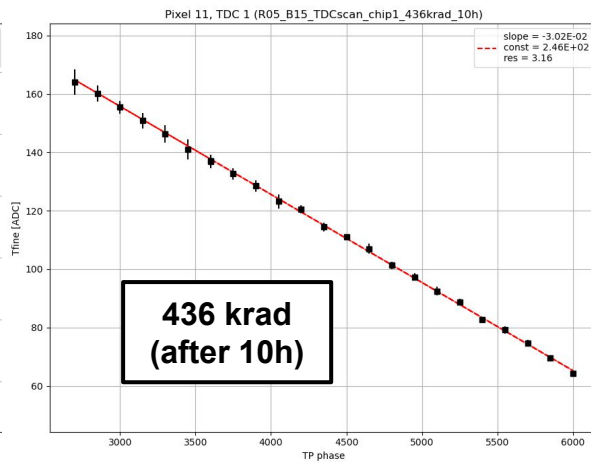
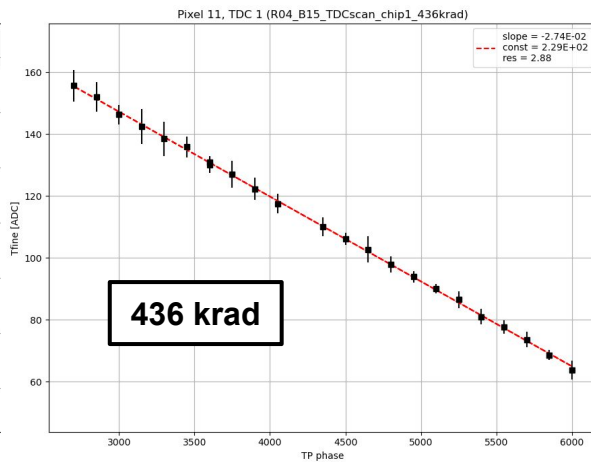
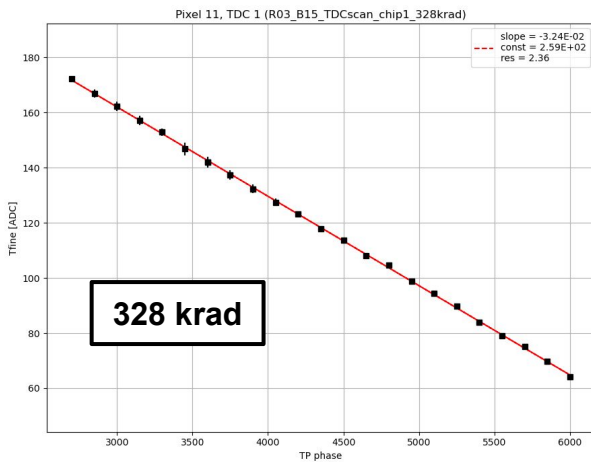
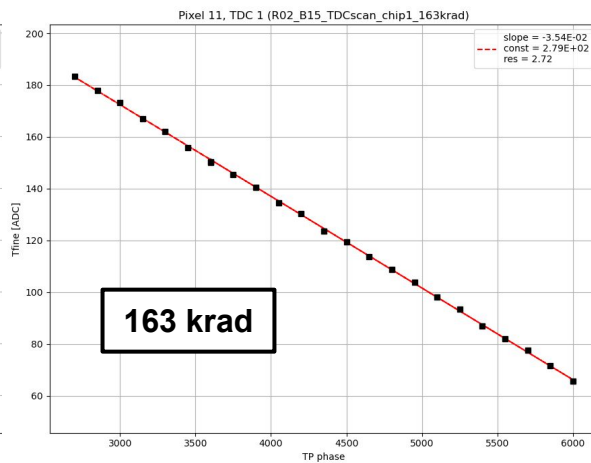
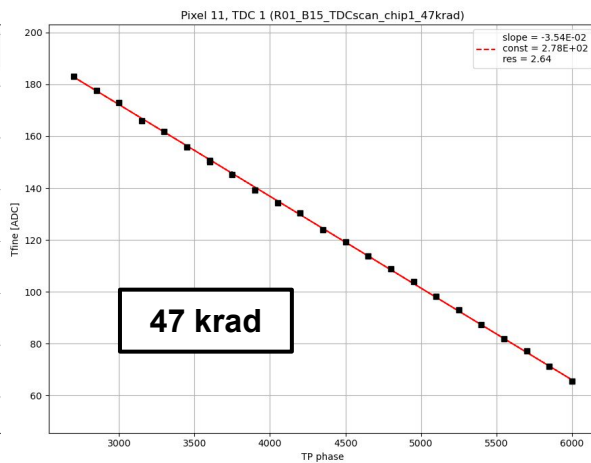
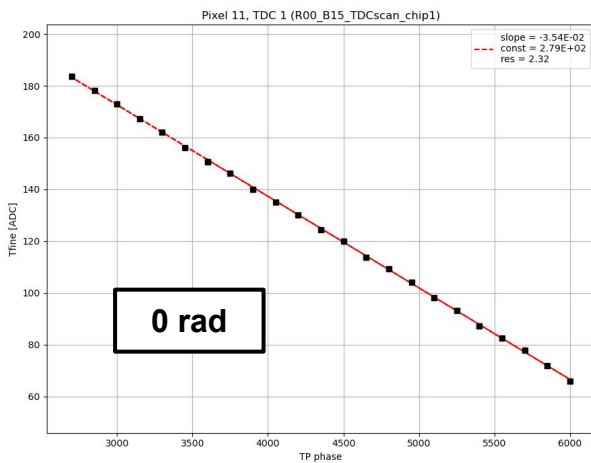
- **Pixel** configuration registers and FSMs **already protected against SEU** in ALCOR v2
- TMR SEU **protection added also for periphery** configuration registers, Hamming code SEU protection for FSMs: Single Error Correction, Double Error Detection codes (SECDED)
- On board prevention of SEL: **current monitor** on FEB regulators

## TID

- Same technology already verified for TID up to a **few hundreds of krad**
- Also other FEB components will be tested and validated

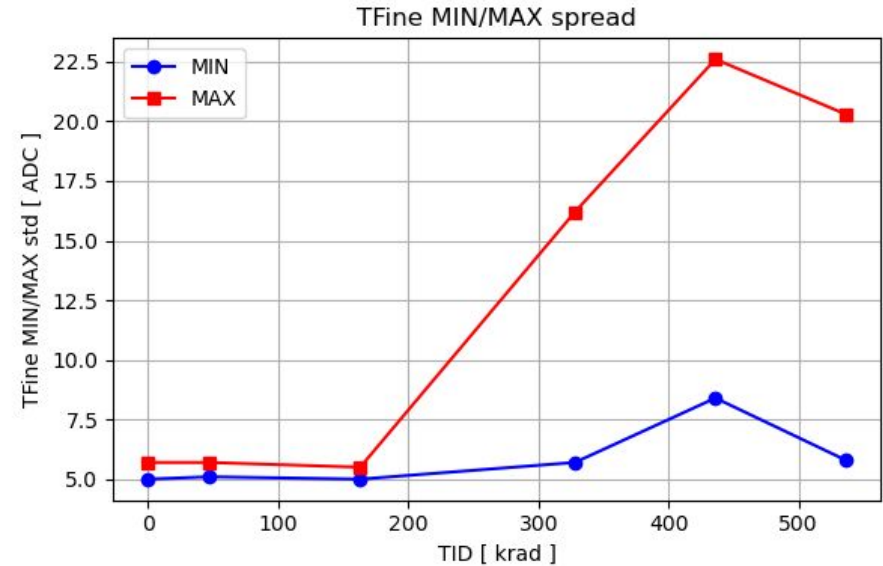
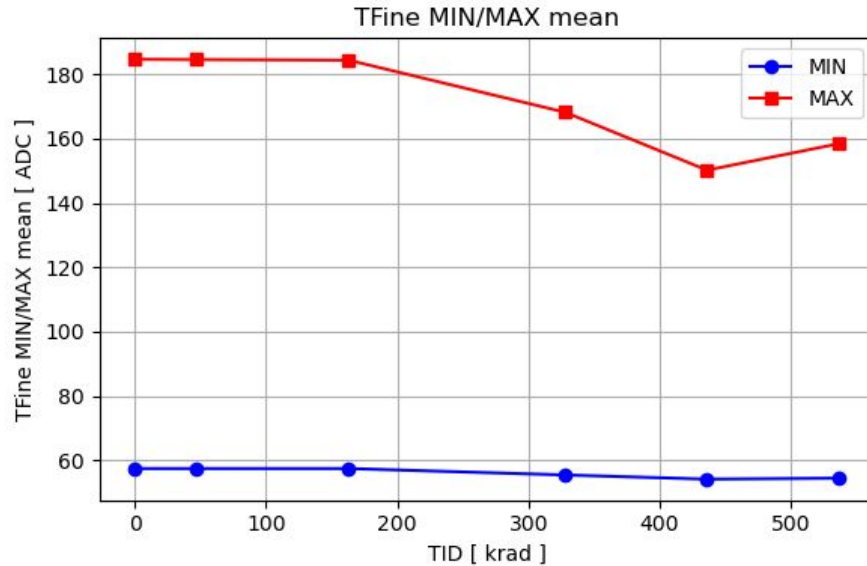
- Irradiation tests campaign: SEU/SEL and TID tests at Centro of Proton-Therapy in Trento with ALCOR current version foreseen in July 2024

# ALCOR TID - TDC response



TP phase scan (3600 → 1 clk cycle) at different TID → check TFine MIN, MAX, sigma, slope, IF, LSB

# TDC results - TFine MIN & MAX (32 channels - 128 TDCs)



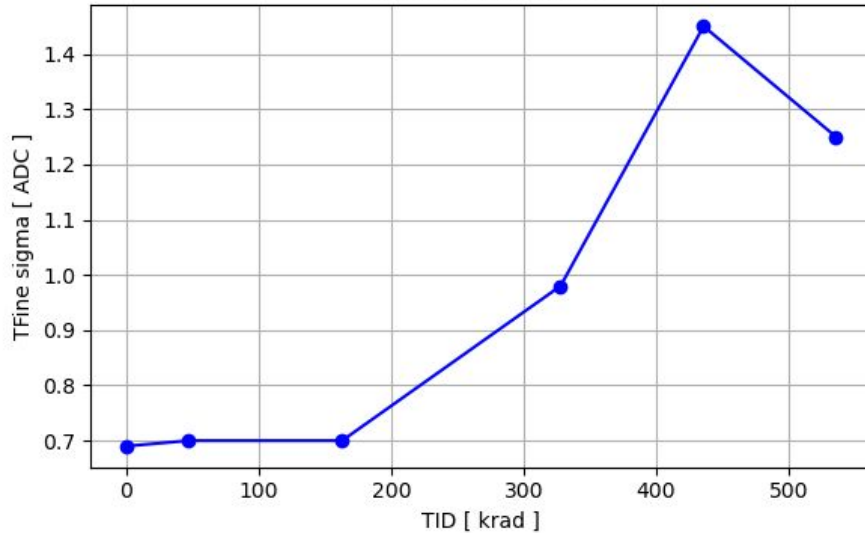
- **TFine MIN** distribution not affected too much
- **TFine MAX** distribution degraded after 328 krad
- \*last point seems to show some annealing

\*last point = 436 krad after 10 hours

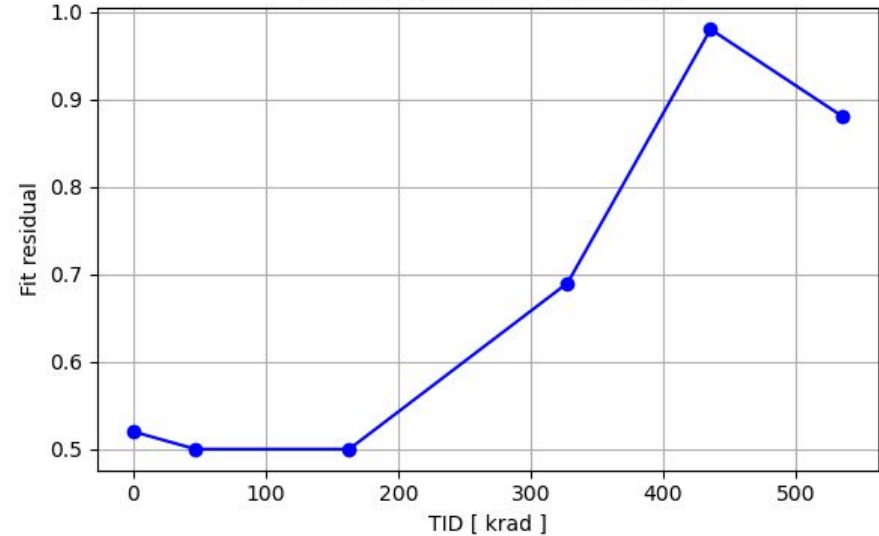
# TDC results - TFine sigma & Fit residual

$$S_{res} = \sqrt{\frac{\sum (Y - Y_{est})^2}{n - 2}}$$

TFine Sigma Mean

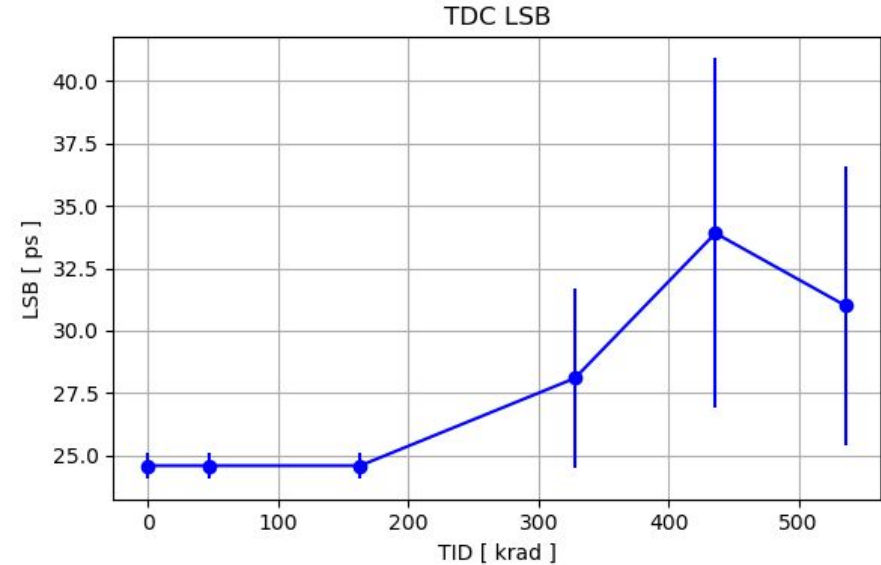
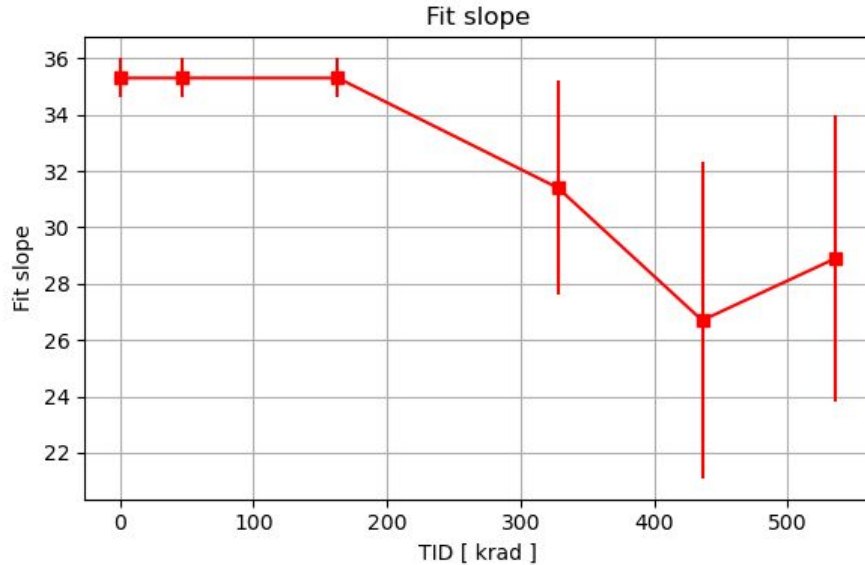


Fit residual standard deviation



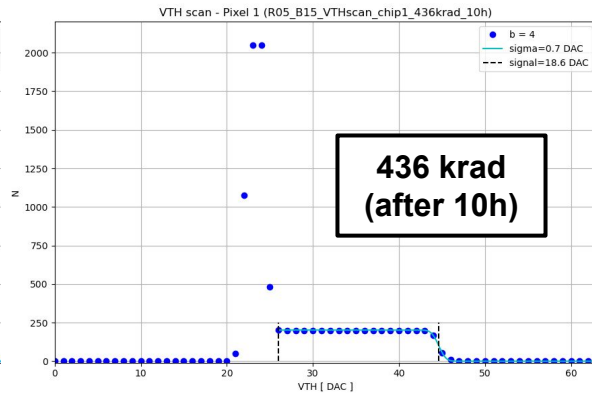
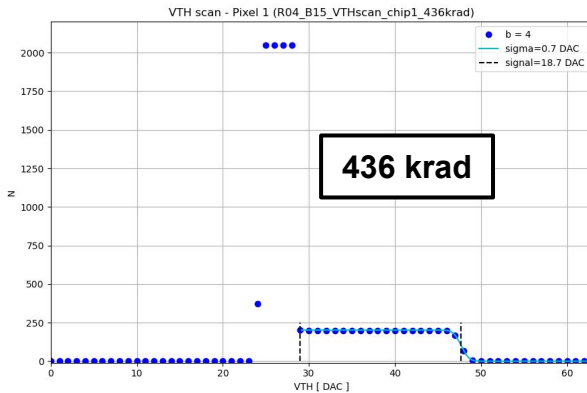
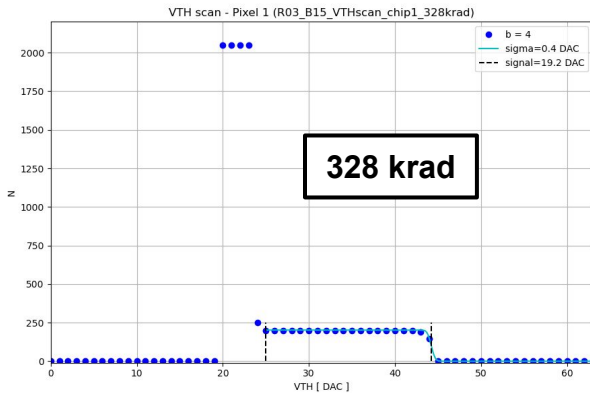
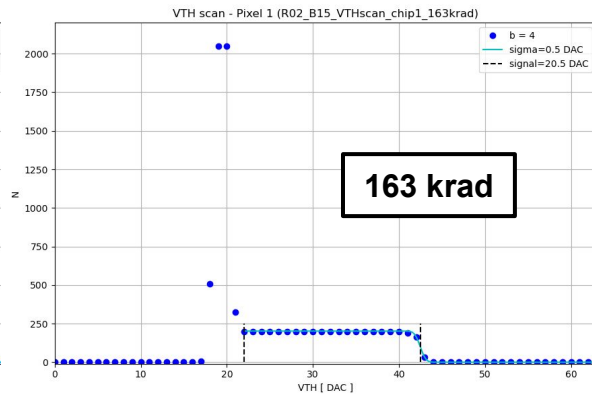
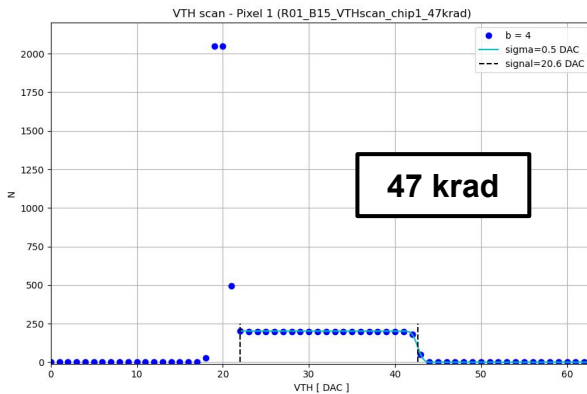
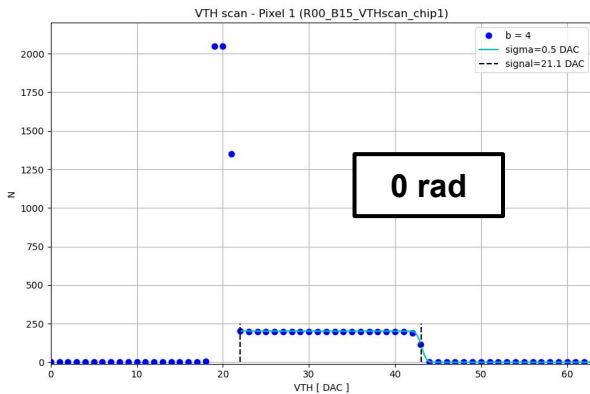
- **TFine sigma** starts to increase after 328 krad, >2 ADC after 436 krad on several pixels/TDCs
- **Fit residual** shows linearity degrading after 328 krad, much worse after 436 krad
- \*last point seems to show some annealing

# TDC results - Fit slope and TDC LSB



- Fit slope degraded after 328 krad → worse **linearity** and very broad **LSB** distribution
- \*last point seems to show some annealing

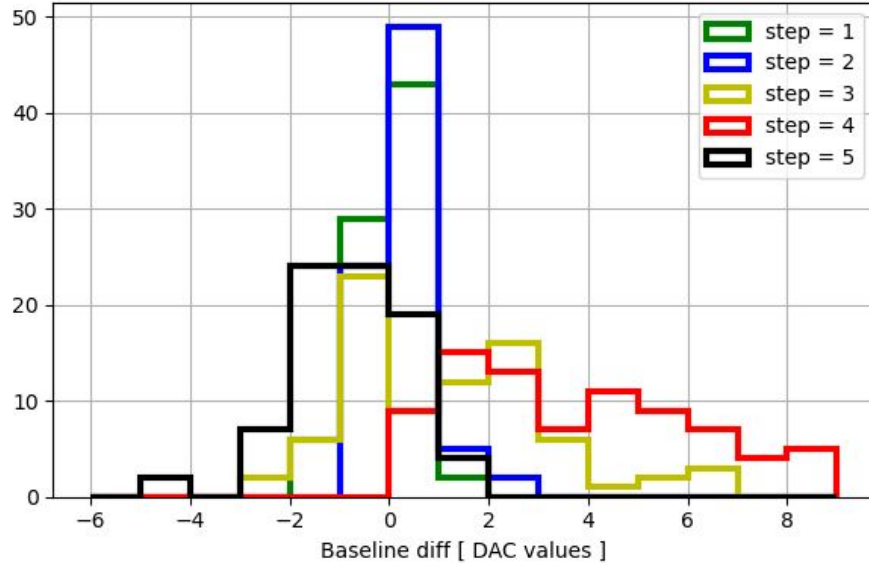
# ALCOR TID - FE response



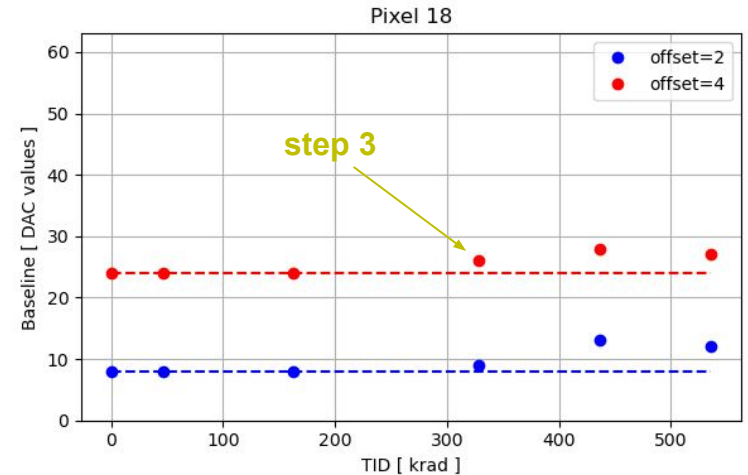
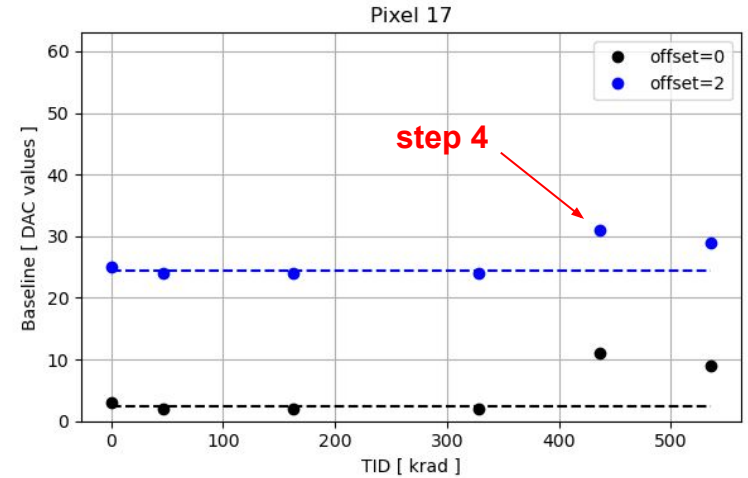
VTH scan (6-bit DAC) with internal TP at different TID → check baseline level, signal amplitude and sigma



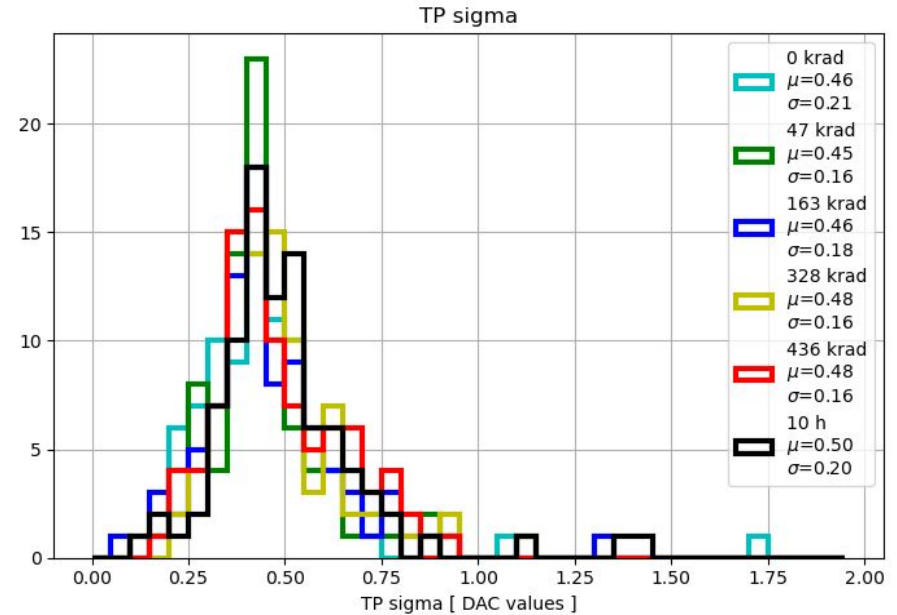
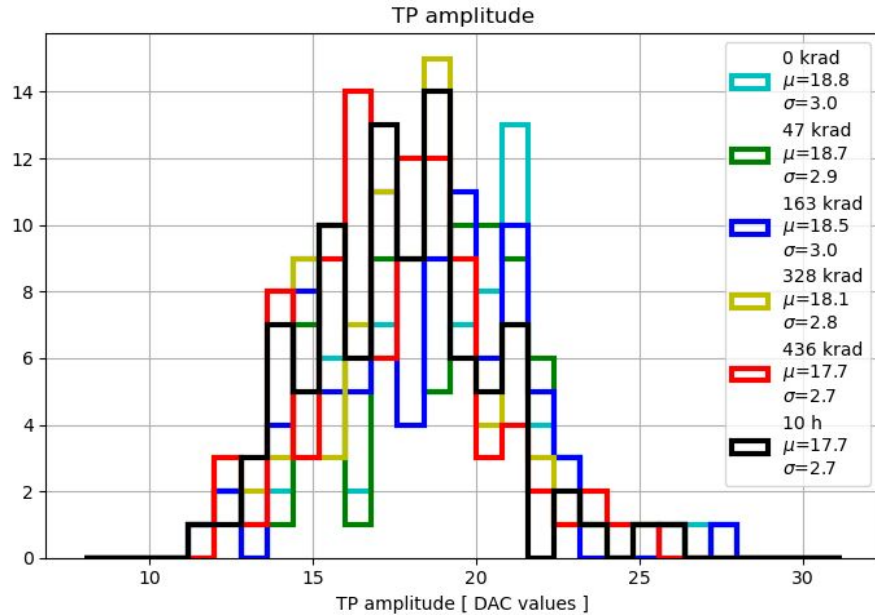
# Front-End results - Baseline



**Signal baseline** slightly moving up after **step 3** (328 krad) and/or **step 4** (436 krad), but it can also be VTH moving down



# Front-End results - Signal



- Very small decrease in **signal amplitude**
- Very small increase in **signal sigma**

# ALCOR SEU/SEL

**ALCORv3:** TMR SEU protection added also for periphery registers, Hamming code SEU protection for FSMs

ECCR/BCR/PCR registers checked against SEU (every second)

- ECCR  $\sigma = (9.4 \pm 1.8) \cdot 10^{-14} \text{ cm}^2/\text{bit}$
- BCR  $\sigma = (7.6 \pm 1.1) \cdot 10^{-14} \text{ cm}^2/\text{bit}$
- PCR  $\sigma = (3.3 \pm 0.5) \cdot 10^{-15} \text{ cm}^2/\text{bit}$

periphery register → no TMR in ALCOR v2.1  
periphery register → no TMR in ALCOR v2.1  
pixel register → TMR

## SEU rate in ePIC:

- dRICH Flux = 20 (h > 20 MeV) / (cm<sup>2</sup> s)
- ALCOR bits: (2048 + 192) = 2240 → ALCOR-64 bits will be 4480
- Total ALCOR: 4992
- Total bits: 4992 · 4480 = 2.2 · 10<sup>7</sup> bits

➤  $\sigma = 3.3 \cdot 10^{-15} \text{ cm}^2/\text{bit} \rightarrow \text{MTBF} = 6.9 \cdot 10^5 \text{ seconds} \rightarrow \text{every 191 hours}$

➤ No latchup events (from currents monitoring)

Found minor bug in pixel TMR  
**MTBF expected to improve with ALCORv3**

# TID-SEU tests summary

- ALCOR tolerance for total ionizing dose (TID) effects has been tested up to 436 krad
  - No significant effects on Front-End response for TID up to 436 krad
  - Some decrease on TDC performance only after TID of 328 krad
- These results match well with [1] and show that the technology is sufficiently radiation tolerant to be used in the ePIC dRICH environment
  - No special design techniques were adopted to increase the TID tolerance of ALCOR
  - TDC performance worsening likely due to some radiation induced leakage current in one of the switches controlling the dual-ramp operations, where very small currents are employed
- MTBF due to SEU more than adequate for dRICH operations
- Repeat TID-SEU tests, together with RDO irradiation tests, to have more TID points and SEU statistics

# ALCOR submissions plan

**ALCOR is designed in UMC 110 nm CMOS technology (submission to IMEC)**

**ALCOR is part of INFN in-kind contribution**

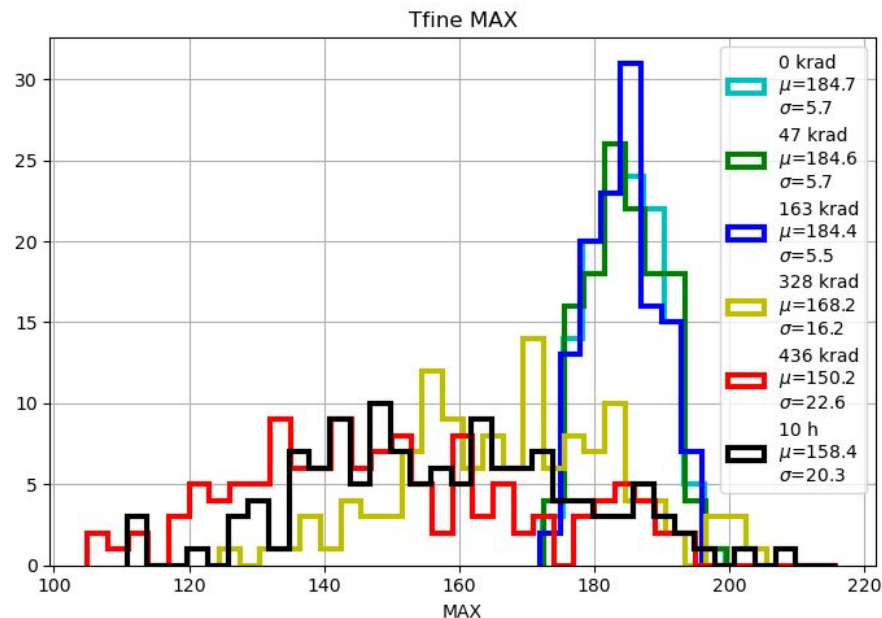
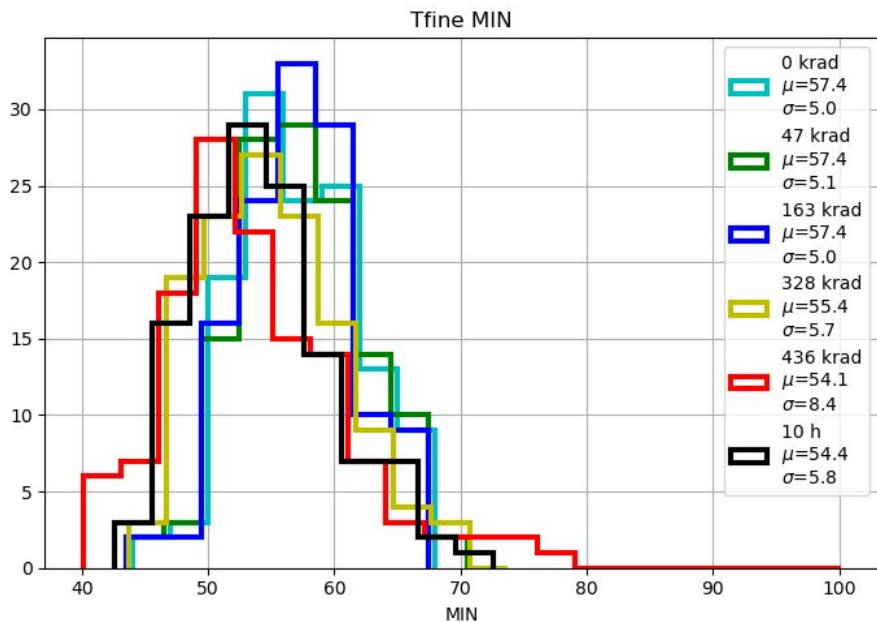
- ALCORv3 MPW was planned for 25th Nov 2024: run canceled by UMC
  - We have to go to the first MPW shuttle of next year, waiting for 2025 schedule
  - Quotation for BGA packaging available
  - Purchase orders for MPW and packaging already started
  
- ALCOR mass production in 2026
  - Preliminary quotations for ALCOR **engineering run** and **packaging assembly** already available

# Milestones

- ❑ Readiness at 75% of the final design of ALCOR v3 by September 2024
  - MPW run canceled by UMC, waiting for 2025 MPWs schedule from UMC and IMEC
  - Top level integration and verification ongoing
  - Optimization of ALCOR data frames structure to match EIC orbit period
  - ALCOR v3 will be ready for tapeout by the end of 2024
  
- ❑ Completion of irradiation tests on ALCOR v2 and evaluation of SEU cross-section by July 2024
  - Results show good radiation tolerance for dRICH requirements
  - No effects from TID up to 200-300 krad
  - MTBF due to SEU more than adequate for dRICH operations

Backup Slides

# TDC results - TFine MIN & MAX (32 channels - 128 TDCs)

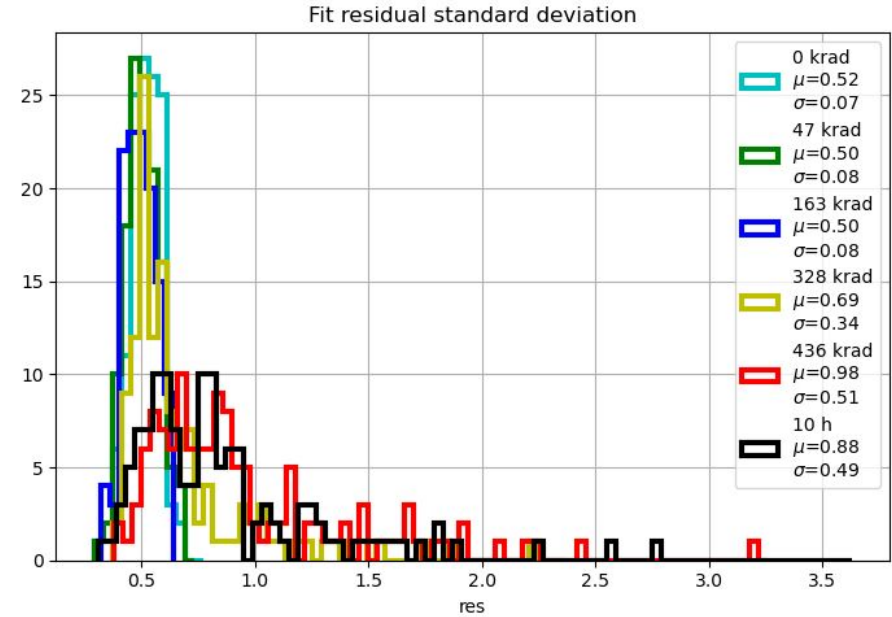
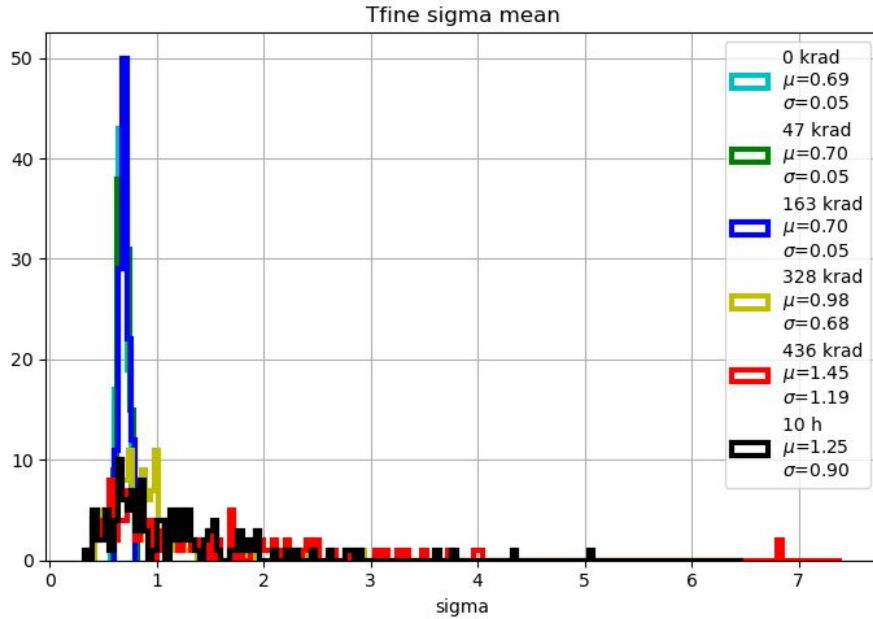


- **TFine MIN** distribution not affected too much
- **TFine MAX** distribution degraded after 328 krad



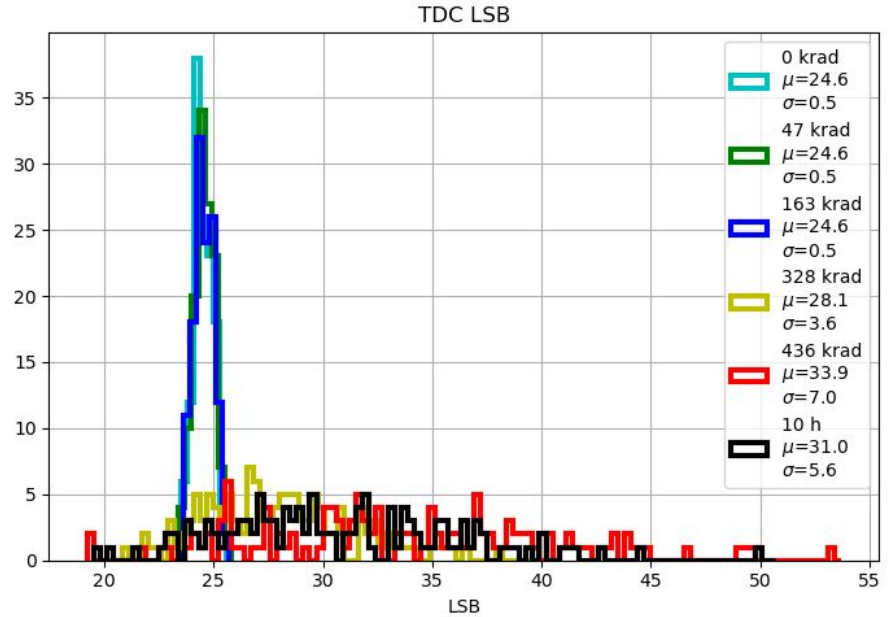
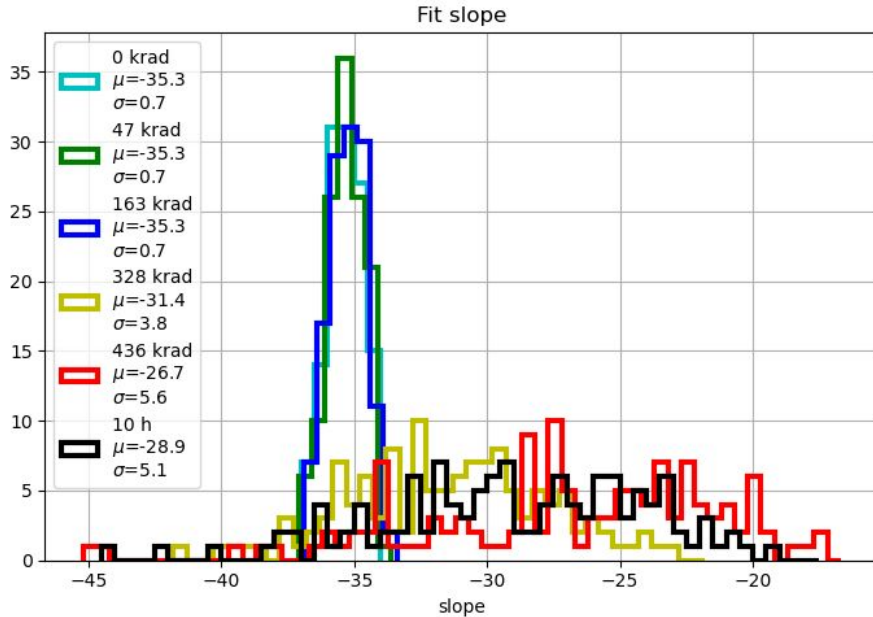
# TDC results - TFine sigma & Fit residual

$$S_{res} = \sqrt{\frac{\sum (Y - Y_{est})^2}{n - 2}}$$



- **TFine sigma** starts to increase after 328 krad, >2 ADC after 436 krad on several pixels/TDCs
- **Fit residual** shows linearity degrading after 328 krad, much worse after 436 krad

# TDC results - Fit slope and TDC LSB



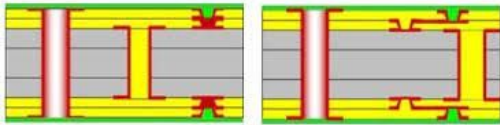
- Fit slope degraded after 328 krad → worse **linearity** and very broad **LSB** distribution



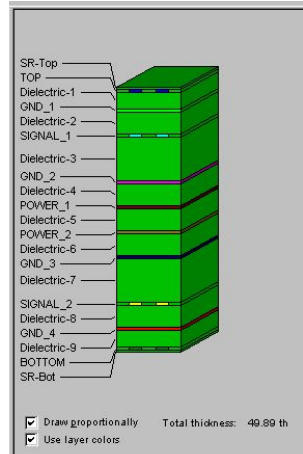
# ALCOR BGA package

**BGA substrate designed by INFN Torino, package assembly done by external company**

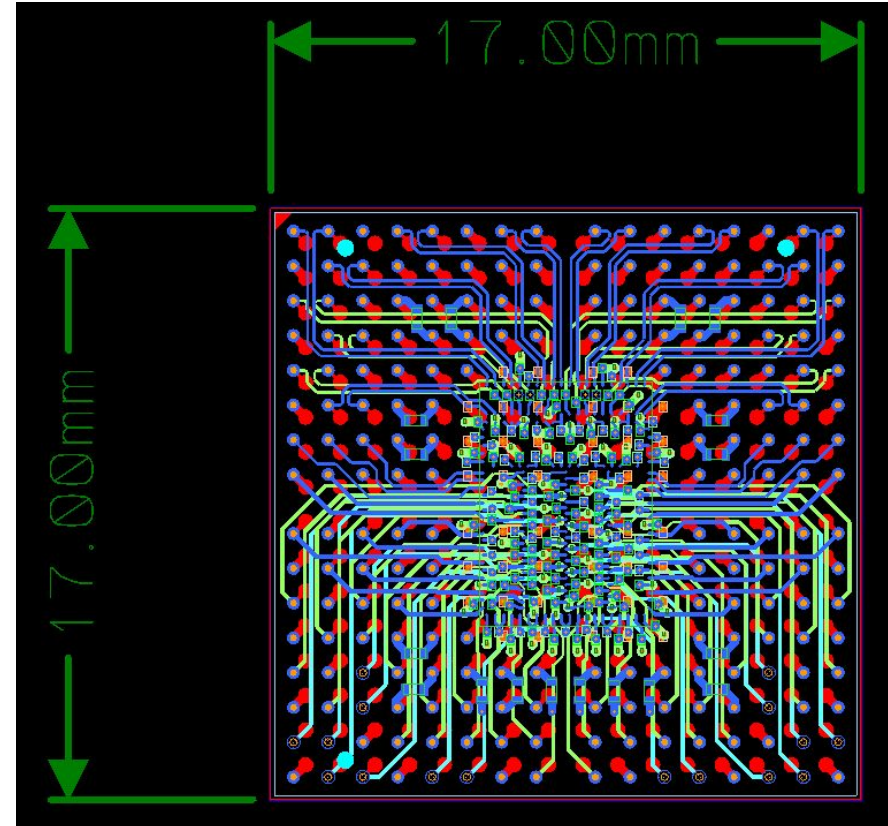
- Size: 17 x 17 mm<sup>2</sup>
- Balls number: 256 (16x16)
- Pitch: 1 mm
- Material: BT-Epoxy
- 10 layers (2+N+2)
- Total thickness = 1.27 mm



2+N+2 HDI PCB Structure



Draw proportionally    Total thickness: 49.99 th  
 Use layer colors



# ALCOR v3 MPW run

## 25<sup>th</sup> Nov MPW run canceled by UMC

- We have to go to the first MPW shuttle of next year, waiting for 2025 schedule

UMC

Old schedule

MPW € MPW mini@sic € mini@sic

UMC MPW	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
UMC 28N Logic/Mixed-Mode – HPC		19		22			22	26	30	28		
UMC 40N Logic/Mixed-Mode – LP			11			24	29	26			18	
UMC 65N Logic/Mixed-Mode/RF – LL	2	26							2	21		
UMC L110AE Logic/Mixed-Mode/RF		26				3			2		25	
UMC L180 Logic GII, Mixed-Mode/RF			4					26				

UMC

New schedule

MPW € MPW mini@sic € mini@sic

UMC MPW	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
UMC 28N Logic/Mixed-Mode – HPC		19		22			22					
UMC 40N Logic/Mixed-Mode – LP			11			24	29	26			18	
UMC 65N Logic/Mixed-Mode/RF – LL	2	26							2			
UMC L110AE Logic/Mixed-Mode/RF		26				3			2			
UMC L180 Logic GII, Mixed-Mode/RF			4					26				