OAK RIDGE National Laboratory

# eRD109 Update – H2GCROC3A

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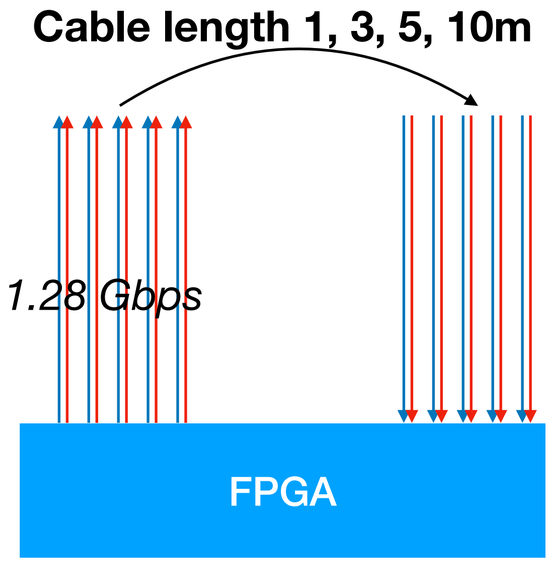
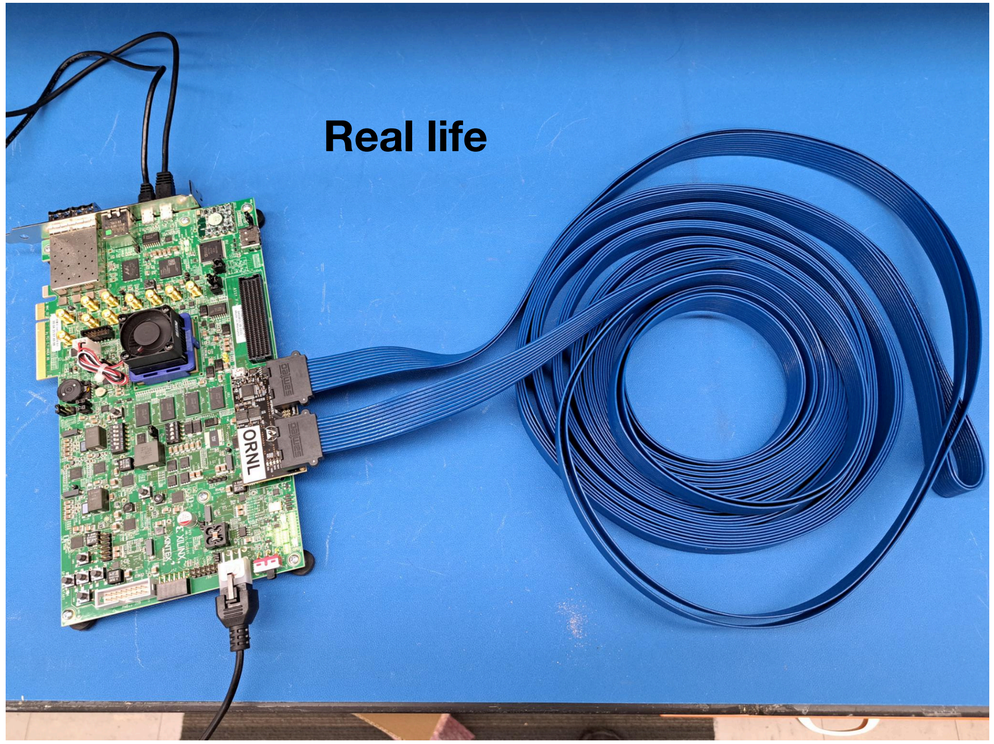
ORNL is managed by UT-Battelle LLC for the US Department of Energy

# Cable testing




**Ordered 1, 3, 5 and 10m cable from Samtec, HQDP**

**The cable is rated up to 14 Gbps for up to 40 inches (==1 meter)**

```
epical@epical-Latitude-E5570:~/Desktop/Firmware/ct$ python3 998_CableTest_Ping.py

-------------------------------------------------------------------------------------------------
>>> Test Script for Cable testing                          <<<
>>>     998_CableTest_Ping.py                              <<<
-------------------------------------------------------------------------------------------------

>>> Ping Cable testing                                     <<<
>>> Start time: 08:00:14
>>> Test length: 10,400,000,000,000 cycle
>>> It takes approximately 72.2 hour

Header Rdy Test Length      / Remain cycles    ErrCnt0  ErrCnt1  ErrCnt2  ErrCnt3  ErrCnt4  - %
a00006  01 00000975704e4000 / 0000000000000000 00000001 00000001 00000001 00000001 00000001 - 0.00%

>>> END <<<
```

**Cable test was running for ~72 hours continuously with the 10 meter cable:**

- Similar 32-bit data word than in H2GCROC3, running at 1.28Gbps
- The data is also shifted from each other that neighboring cable sees opposite binary value
- One error is injected manually for crosscheck
- Otherwise no error is observed

Will make some additional tests where we make more ‘noise’ around the cable.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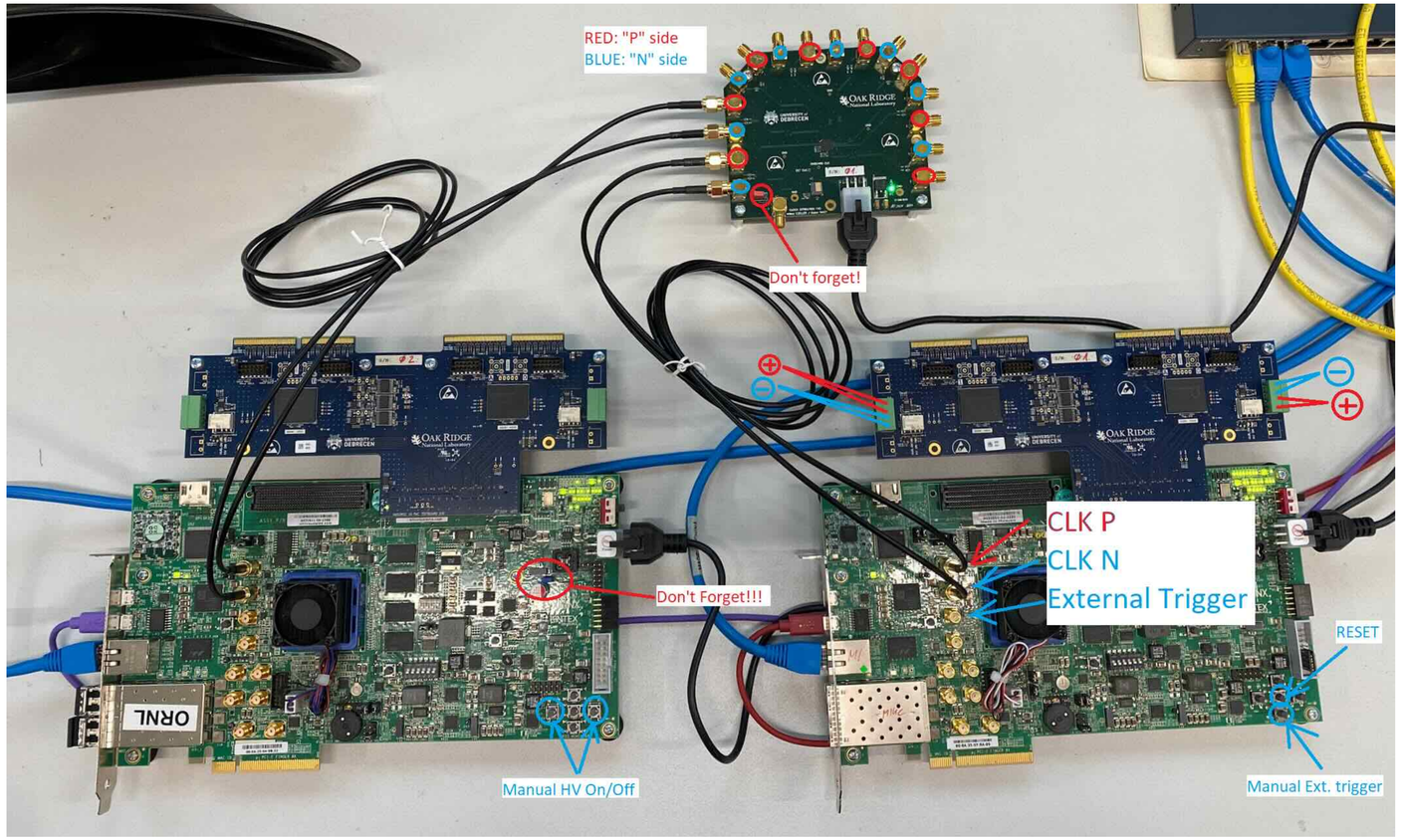
# ProtoBoard2.0 – second iteration with the H2GCROC

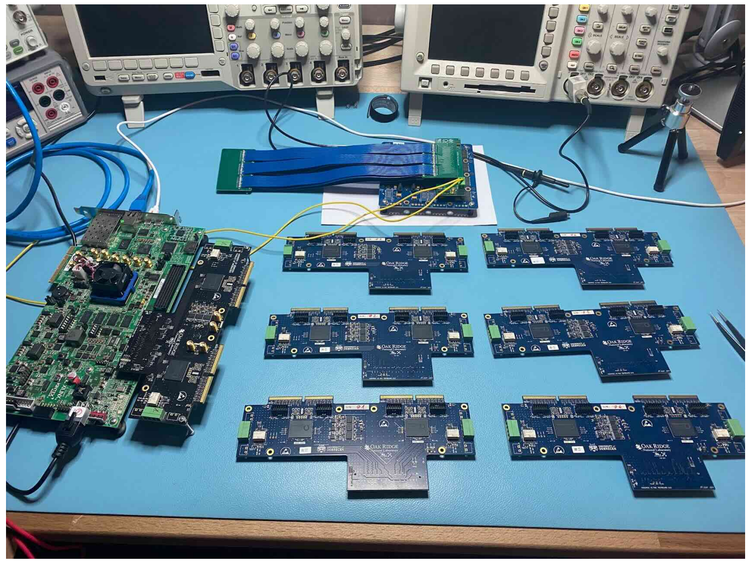



**Compatible design with the commercial CAEN unit:**

- Ease of testing with many collaborators:
  - CAEN has slow readout, capable of 10kHz only in reality

Started with the commercial KCU105 FPGA evaluation board:

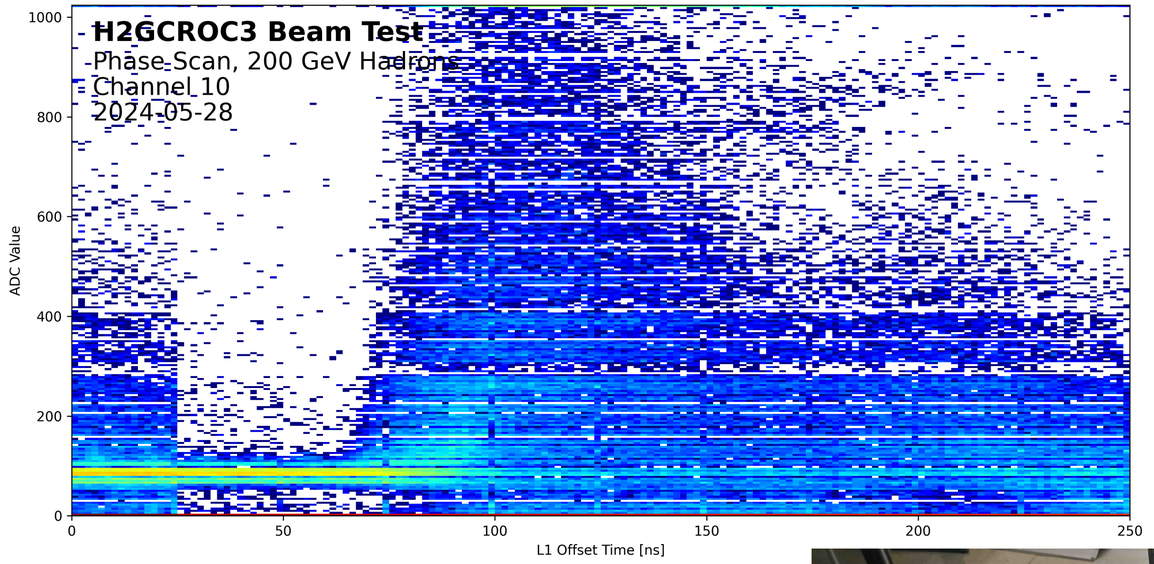
- Multiple KCU's are possible to combine with single clock and trigger distribution boards



Produced multiple boards total 864 channels

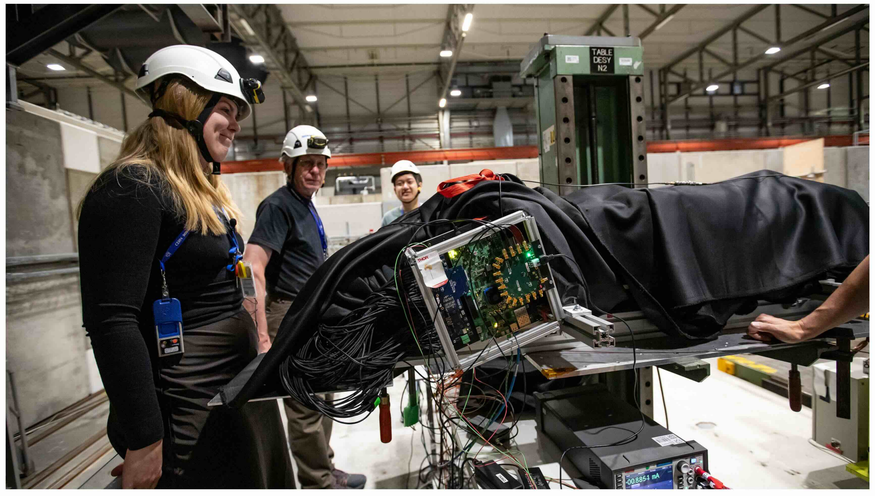
Synergy also with other detectors using HXGCROC (same firmware)

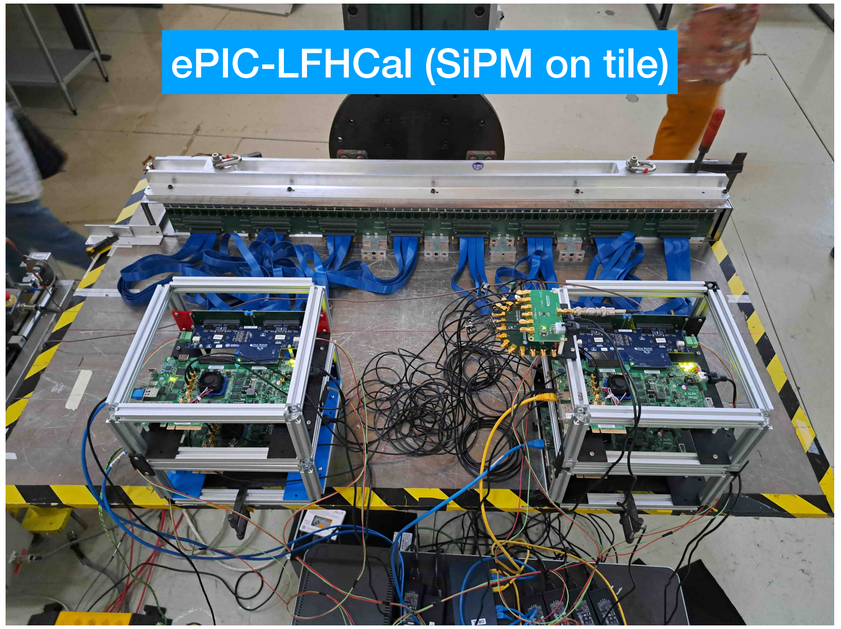
# Testbeams – Early results from in May–Aug 2024




One channel example on the phase scan (sum of 16 runs), ADC only. Overall makes sense, there is a dip in 150-200ns (could be TOT dip, pile up, etc)

ALICE-FoCal (capillary tubes with fiber)





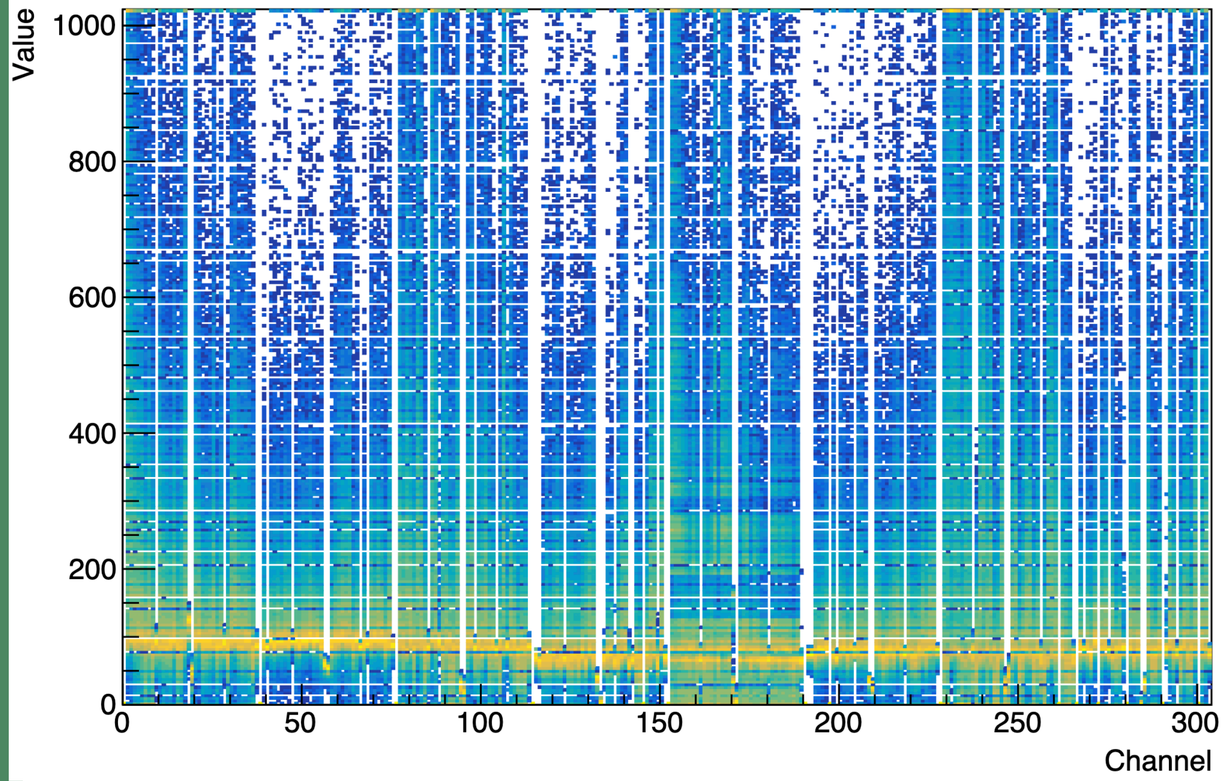

**There were two testbeams:**
**May was cancelled for LFHCal, but we ran with the FoCal-H:**

- This was very useful for debugging. We had a lot of lost UDP packets and low reconstruction efficiency (10-50%).

**Sept was first LFHCal and then FoCal-H:**

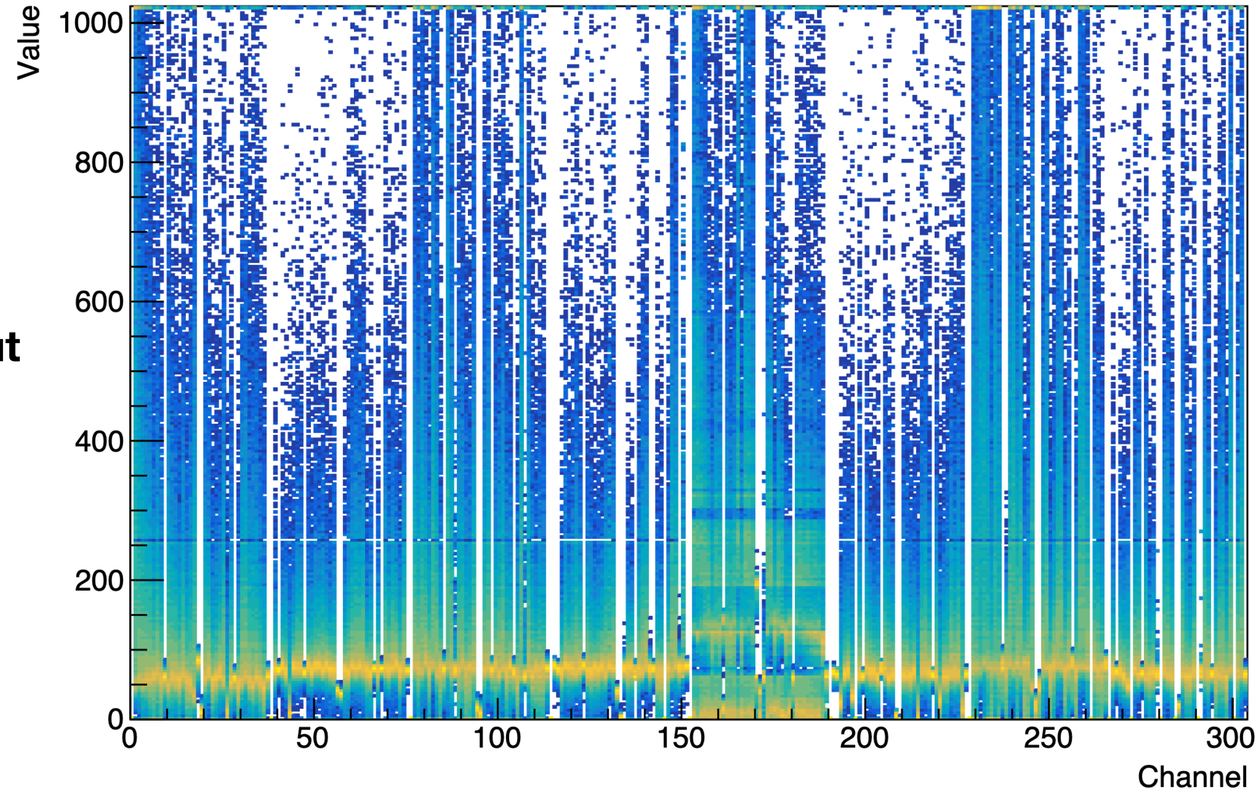
- Much smoother data taking - minimal losses in packets (>95% overall efficiency)

# Some fixes with the ADC delays




**Lot of missing codes in the ADC distribution:**

- This is completely normal, one could update the ADC delays in the I2C register

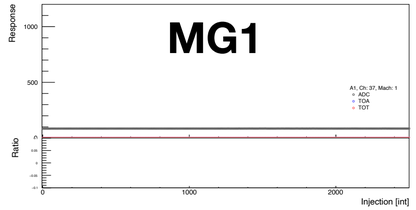



**After adjustments, there is still one missing ADC code, but overall looks much better:**

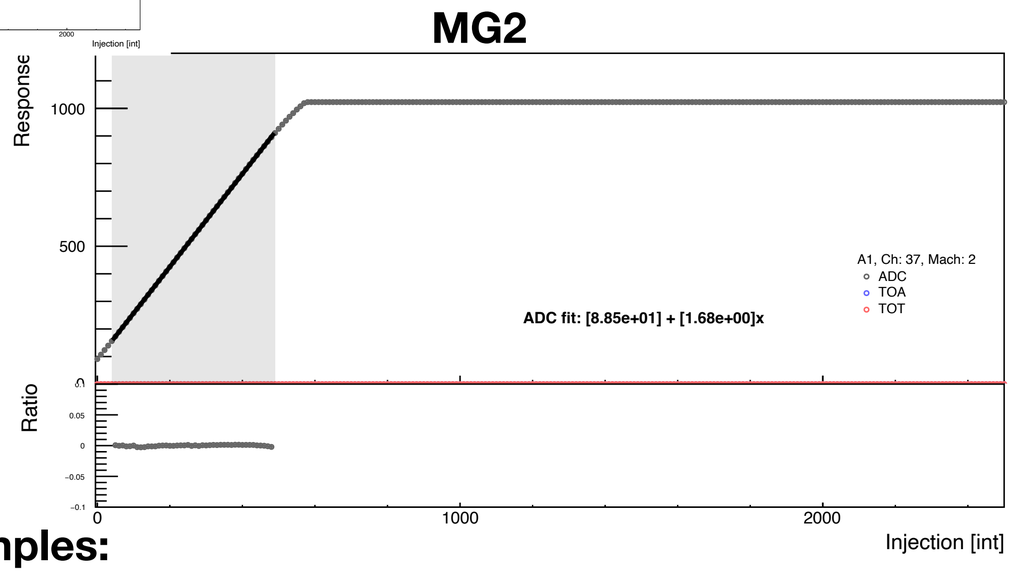
- Only drawback here is that the pedestals change and therefore one has to recalibrate everything again (pedestal, TOA, TOT thresholds)

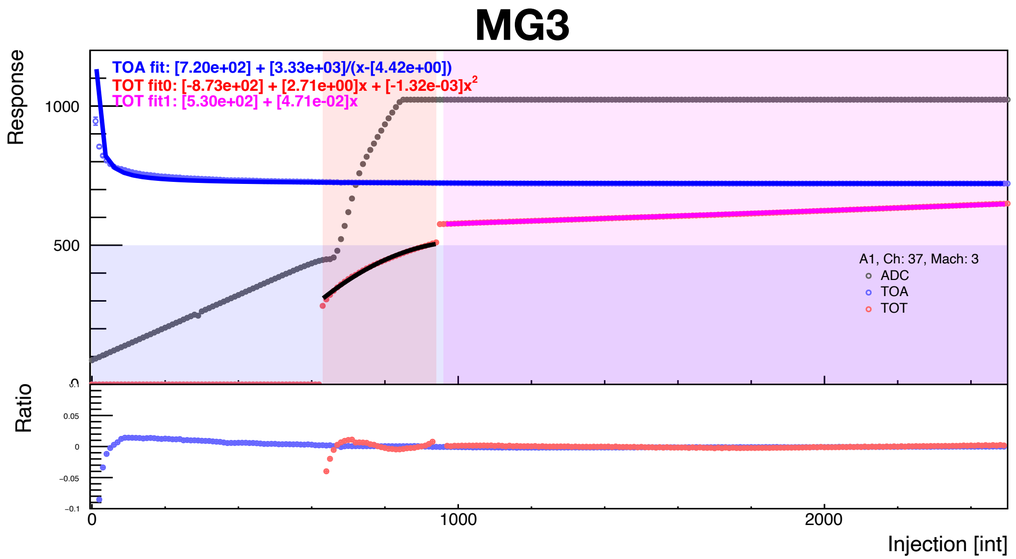
# Calibration runs with TOT – this is to combine ADC-TOTs together

**Even in calibration run, we run with machine gun trigger (multiple samples per hit)**




Internal injection of the chip can help identify the ADC/TOA/TOT behavior



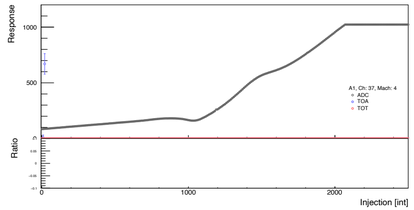




**Different samples:**

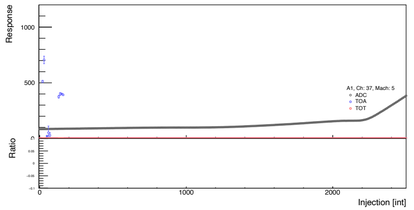
- MG0-1 - just pedestal before the signal
- MG2 - only ADC fires, it goes up to saturation
- MG3:
  - TOA has the slewing in the beginning
  - TOT has two regions:
    - < 512 - more quadratic function than linear
    - > 512 - very stable linear function

**After the signal samples**

**MG4**




**MG5**



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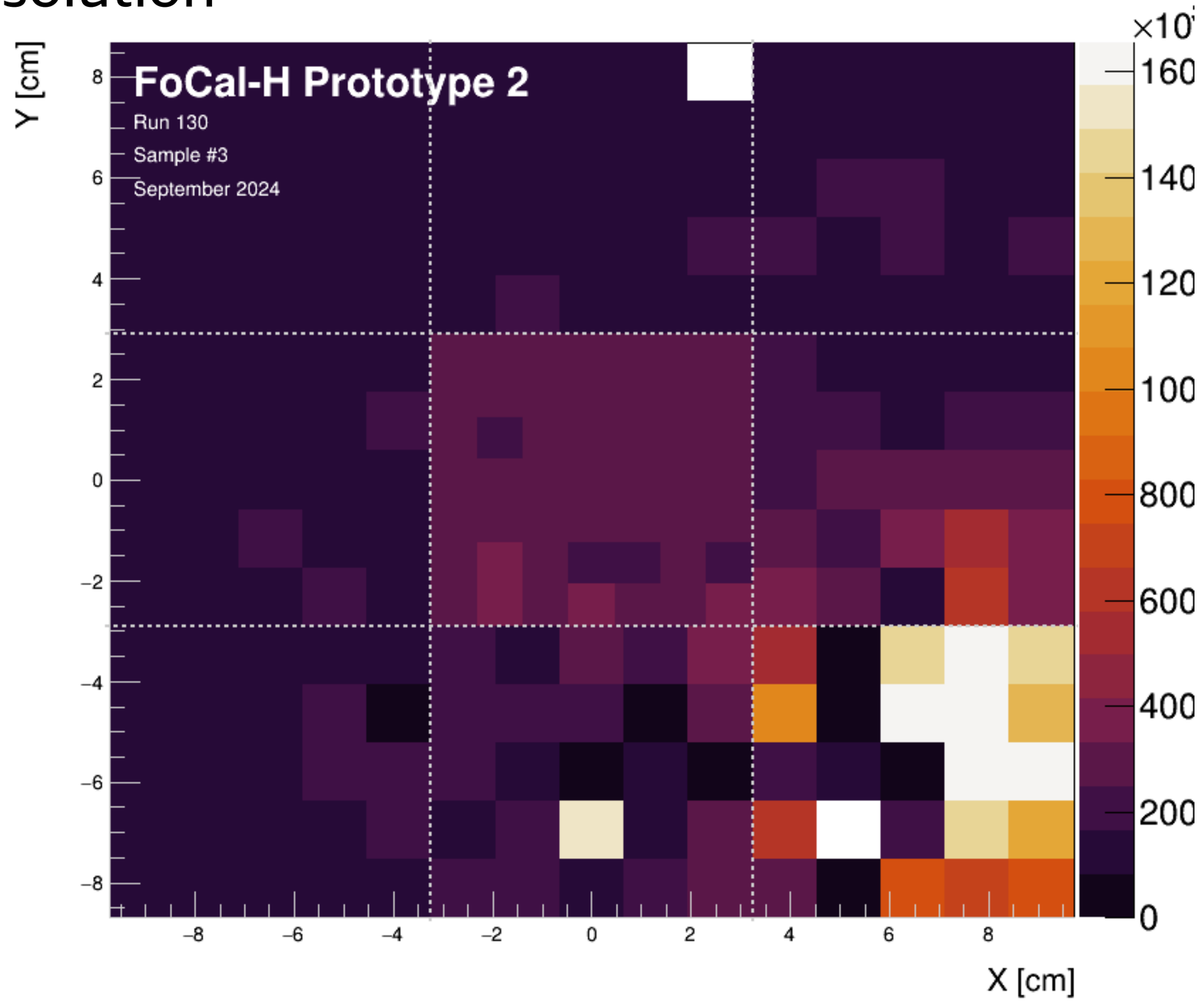
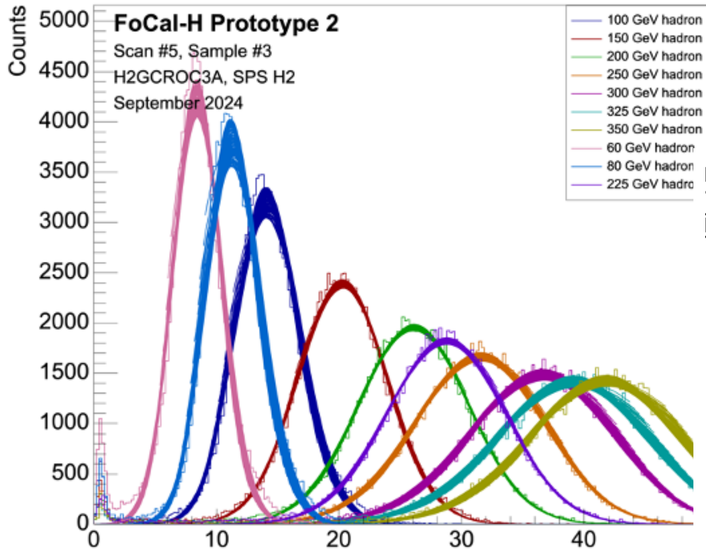
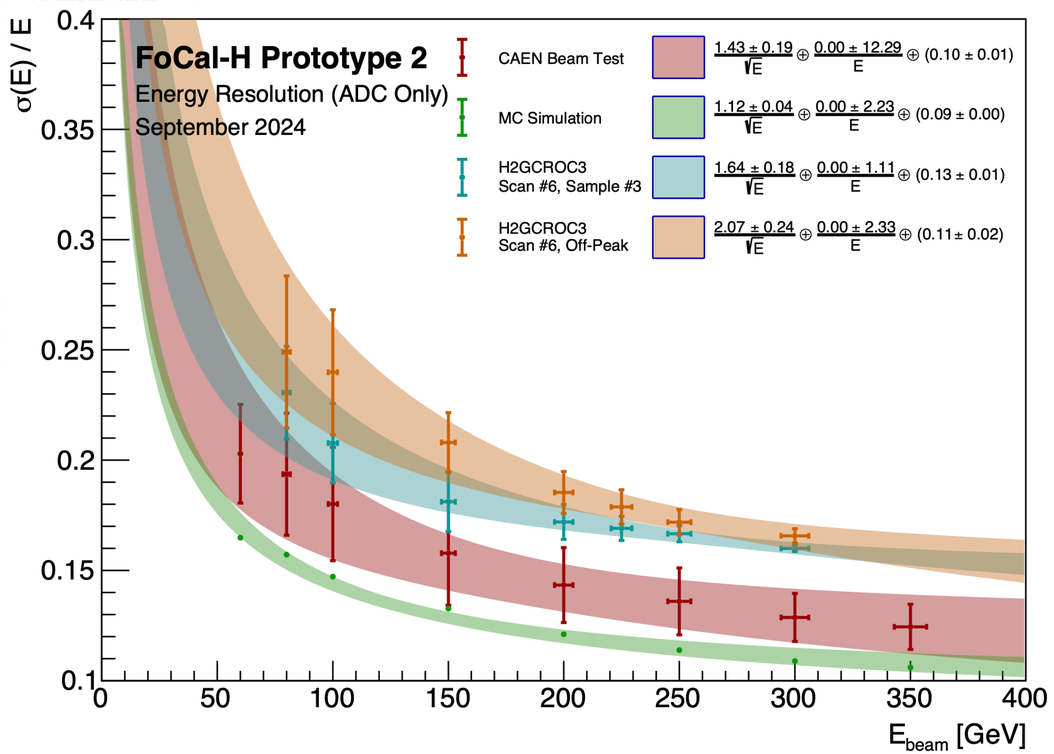
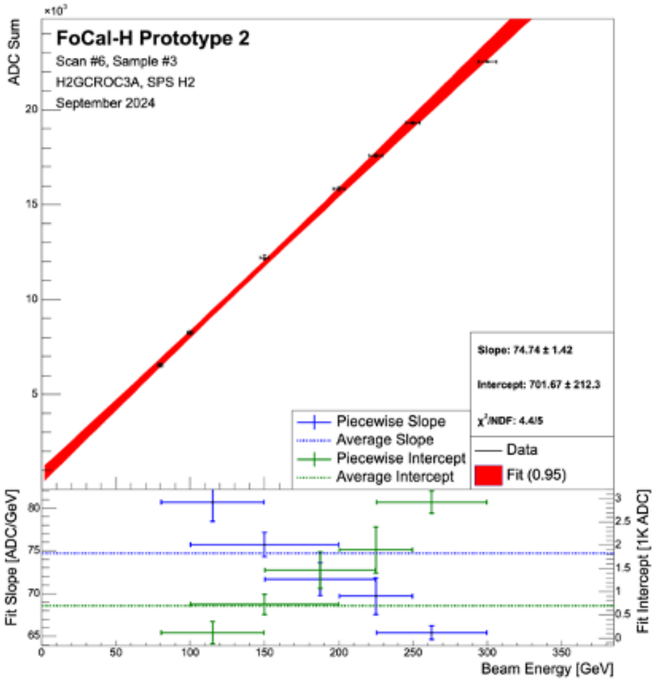
# Position resolution



# Some very early resolution figures



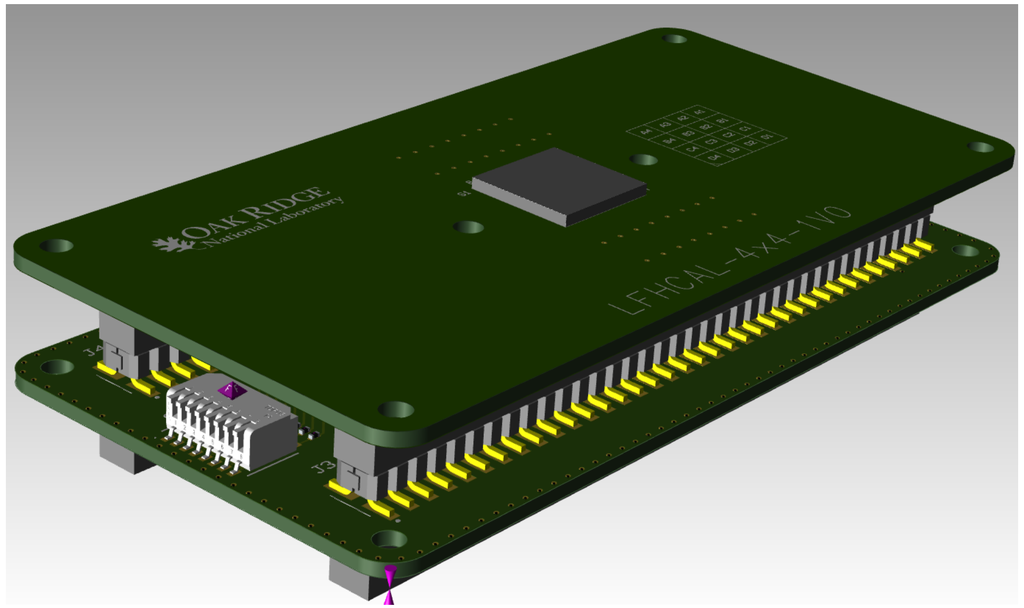




**These are just teaser plots, the analysis is still ongoing and we are working on combining the TOT into the analysis**

# Some future tests

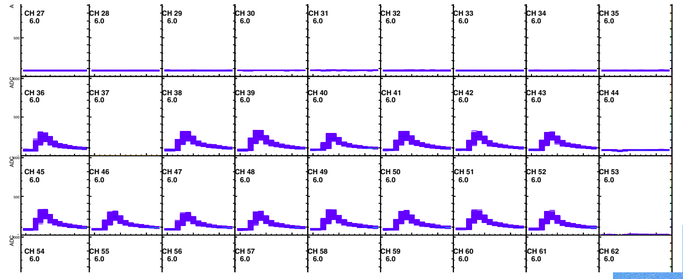
**Finally starting to sum:**

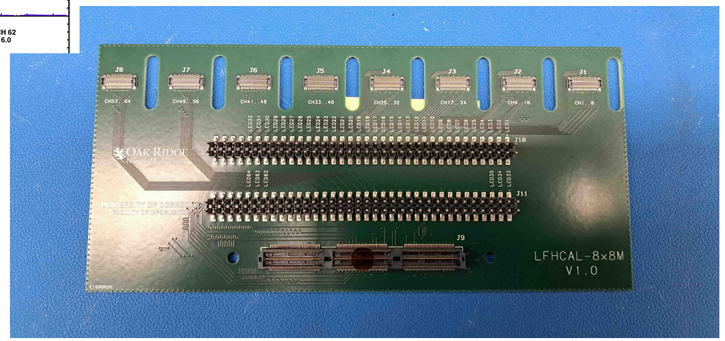
- The summing board is designed
  - Passive summing, this one should result in longer signal
  - There is a switch to ‘sum’ 1-8 SiPM’s, using the BIC 4x4 SiPM array for this




**LED calibration circuit:**

- We saw a nice LED signal from the PWO4 tests
- We rerouted the SiPM pulser from the H2GCROC to the FPGA
- Now redoing the same exercise with the LFHCal setup
  - Work in progress…
  - Then designing a daughter board for the LED pins in order setup which LED will be flashed



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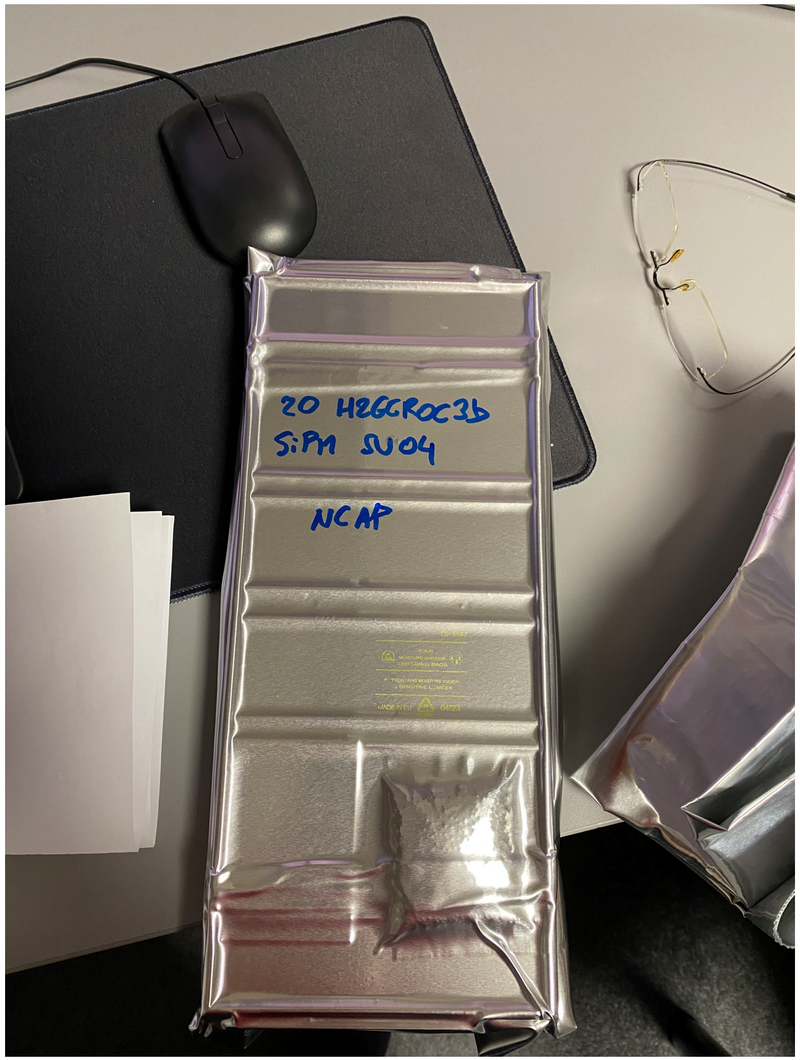
# New boards can be produced




**20 new chips are now available, that's 10 new boards:**

- These are H2GCROC3B (previous was 3A), should be the same for this version
- I ran out of money, so I cannot pay a single one
- It is about 1000$/board now

Who wants them:

- Me :)
- Miguel from UCR (Insert, ZDC)
- Carlos from IJCLab (EEEMCal)
- Henry from ANL (BIC)
- Po-Ju Lin from NCU Taiwan (ZDCe)
- Stefan, Martin, John from BNL (BHCal)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