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Status report of the eRD109 project on SALSA chip development

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EPIC DAQ/electronics WG meeting

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SALSA CHIP TARGET SPECIFICATIONS

Versatile front-end characteristics

- Dedicated to MPGD detectors and beyond
- 64 channels
- Large input capacitance range, optimized for 50-200 pF, reasonable gain up to 1nF
- Large range of peaking times: 50-500 ns
- Large choice of gain ranges: 0-50, 0-250, 0-500 fC or 0-5 pC
- Large range of input rates, up to 100 kHz/ch with fast CSA reset (limit assumed for EPIC: 25 kHz/ch)
- Reversible polarity
- Front-end elements can be by-passed

Digital stage

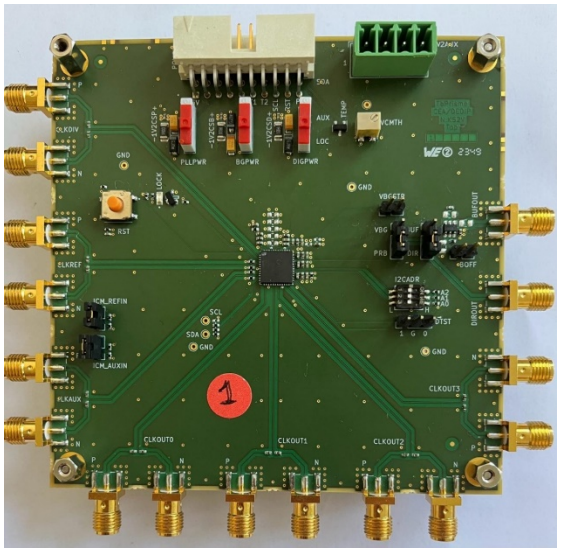
- Fast sampling ADC for each channel on 12 bits (> 10 effective bits) at up to 50 MS/s
- Possibility under study to double rates by coupling pairs of channels
- Integrated DSP for internal data processing and size reduction, treatment processes to be selected according to user needs
- Continuous readout compatible with streaming DAQ foreseen at EIC, triggered mode also available
- Several 1 Gb/s output data links

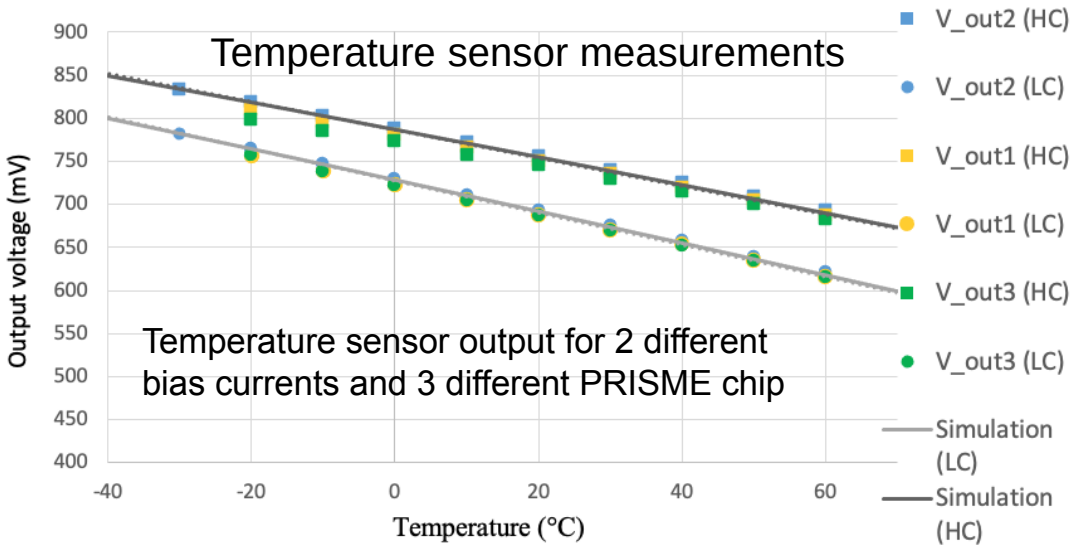
General characteristics

- ~1 cm² die size, implemented on modern TSMC 65nm technology
- Low power consumption ~ 15 mW/channel at 1.2V
- Radiation hardened (SEU, TID)

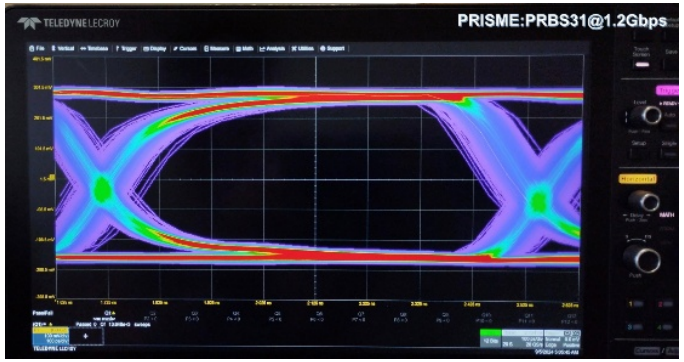
LAST UPDATES ON SALSA PROTOTYPES

- **PRISME tests** (PLL test chip)
  - Temperature probe: functional
  - CERN Bandgap: functional
  - CERN LVDS Rx and Tx: functional, speed up to 1.2 Gb/s
  - I2C: functional
  - 4 phase and frequency adjustment output clocks: functional
  - Radiation sensor output nominal in non-radioactive environment
  - TID radiation tests foreseen in November at CERN
  - PLL noise performance not optimal (cf next slide)
  - Probably a new PRISME prototype by end of 2024





Tx output with PRBS patterns at 1.2 Gb/s



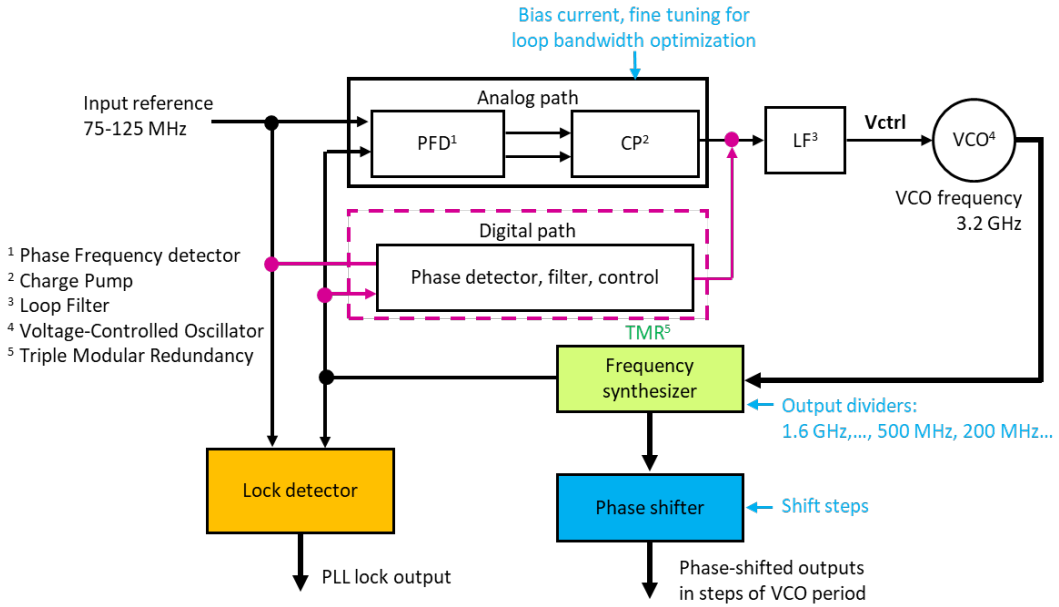
PRISME PLL measurements

Recall: hybrid PLL with coarse digital + fine analog control

- PLL bloc functional, with automatic digital tuning working as expected
- Wide input dynamic range achieved on range 80 -105 MHz
  (ok for CERN and EIC environments)
- Random jitter component as low as 2.5 ps RMS
- However deterministic component larger than expected, up to 50 ps RMS

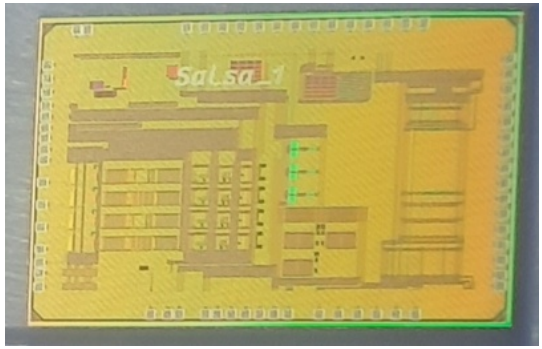
After simulations:

- Origin of the issue identified, from low frequency noise of internal 3 GHz oscillator
- Solution found to correct the design, could be submitted by end 2024



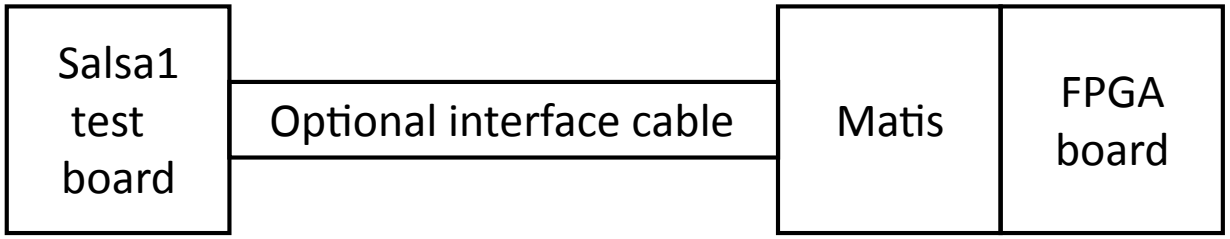
LAST UPDATES ON SALSA PROTOTYPES

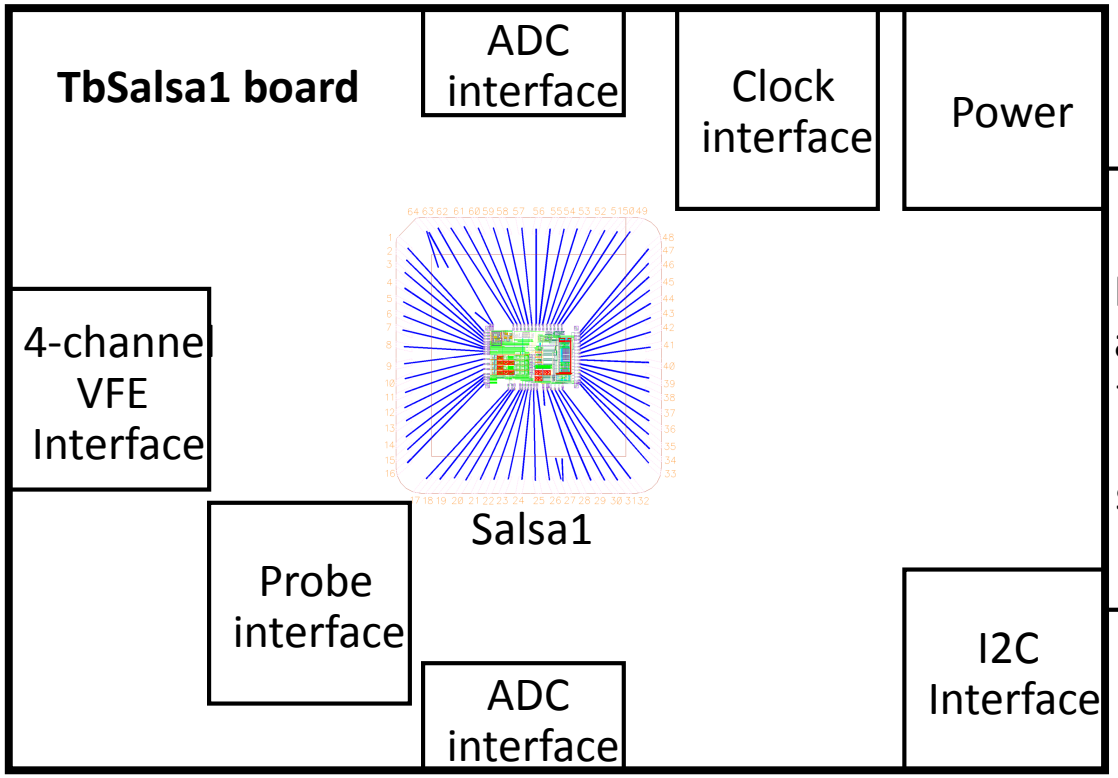
- **SALSA1** (front-end + ADC on 4 channels, + 2 channels ADC only)
  - Naked dies just arrived at Saclay, sent to packaging company
  - QFN 64 package selected, bonding diagram defined, order done
  - Datasheet and user manual being written
  - Test-board schematics done, layout design in progress, component procurement in progress
  - Most ADC characteristics will be tested with main test-board, specific test-board for fine evaluation later if necessary
  - In-house MATIS system board will control and read SALSA1 test cards

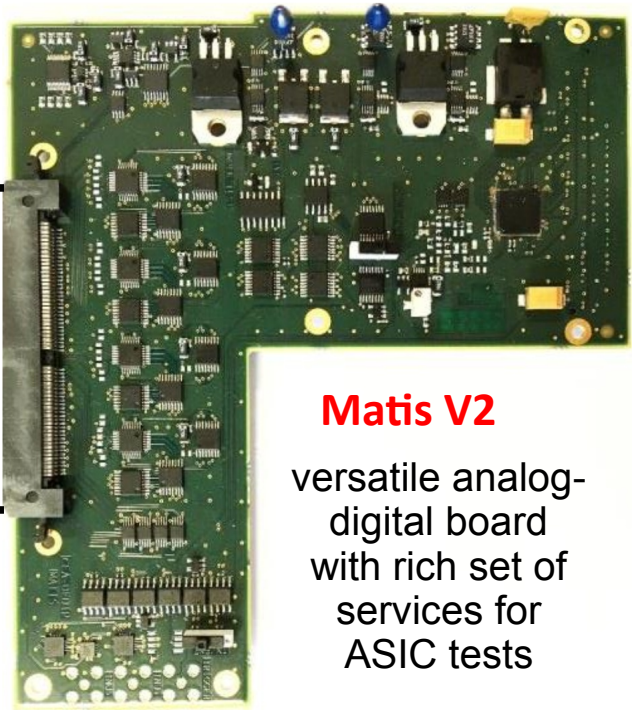


- **SALSA2** (fully featured prototype on up to 32 channels)
  - Main DSP blocks and associated algorithms mostly defined. Work ongoing on HDL code
  - Detailed definition of the I/O interfaces in progress, impact from choice at EPIC of lpGBT or Firefly for the I/O FEB interface
  - Specification document being written to gather details on architecture and block internal structures

SALSA1 TEST SETUP







Matis V2

versatile analog-digital board with rich set of services for ASIC tests

PROJECT MILESTONES AND NEXT STEPS

eRD109 FY23 project milestones

- Specifications of SALSA1 design → done
- Production of SALSA1 prototypes → dies delivered to SERMA (packaging company)
- Test card production → to begin soon
- Performance evaluation → expected end of 2024 / beginning of 2025

Milestones of generic R&D program for EIC project (new 65nm PLL block)

- PRISME prototype submission → done July 19th 2023
- Packaging and test card production → done February 2024
- Radiation tests → November 2024

eRD109 FY24 project milestones

- SALSA2 specifications → July 2024, details in progress
- SALSA2 submission → March 2025
- Beginning of SALSA2 tests → September 2025

Very next steps

- SALSA1 packaging and test-bench → October-November 2024
- Tests on PRISME prototypes → TID tests in November
- SALSA2 specifications and architecture → in progress, Autumn 2024

SALSA PRODUCTION PLAN

SALSA2: half size prototype (32 channels with main DSP operators)

- TSMC 65nm, MPW via CERN + IMEC
- 100 dies in BGA package (16x16, 1mm pitch, tbc). Targeted company: NCAP (http://www.ncap-cn.com/en/)
- Should be 1mm pitch on PCB size and 300um on ASIC size. TBC
- Tests on chips done by IRFU-USP consortium, samples available for EPIC

SALSA3: full size prototype (64 channels with full DSP)

- TSMC 65nm, MPW via CERN + IMEC if the final size is compatible.
- 100 dies in BGA package
- Should be 1mm pitch on PCB size and 300um on ASIC size. TBC
- Tests on chips done by IRFU-USP consortium, samples available for EPIC

SALSA: production chip

- TSMC 65nm, engineering run, depending on the (ASIC size)/(Max number of wafers)
- 5000 dies in BGA package=> Call for tender needed for dicing+packaging
- Test: could be done by IRFU-USP to avoid tender. TBC