CyMBaL

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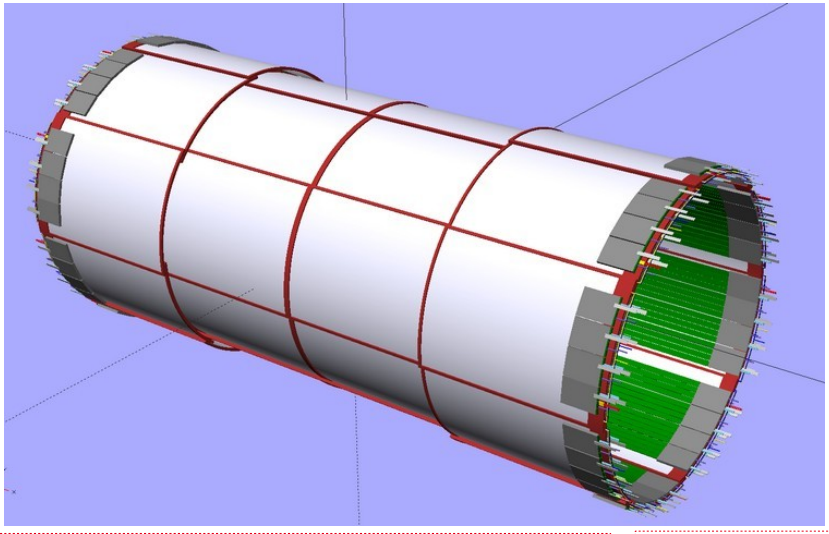
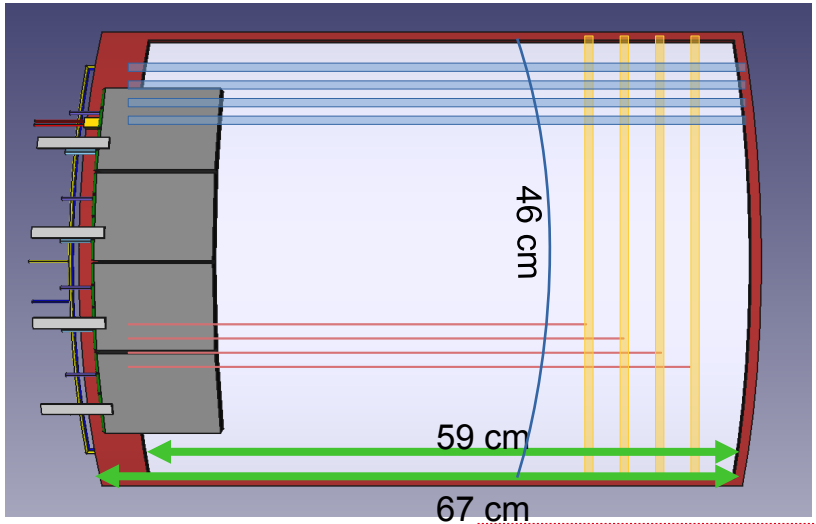
Oct 2nd 2024

CyMBaL

CyMBaL: Cylindrical Micromegas Barrel Layer



Design of a module



Requirements:

- Spatial resolution ~150µm
- Time resolution ~10ns
- Light, less than 1% X0
- Hermetic
- Tight space: ~5cm in R
- Magnetic field: ~2T

- 32 module: 8 modules in ϕ times 4 modules in z
- Overlaps in ϕ and in z for hermeticity
- 1024 readout channels/module
- 32K readout channels

Module dimensions

Z = 67 cm

R*phi = 48 cm

Active zone dimensions

Z = 59 cm

R*phi = 46 cm

CyMBaL – Module

Module dimensions

Z = 67 cm

R*phi = 48 cm

Active zone dimensions

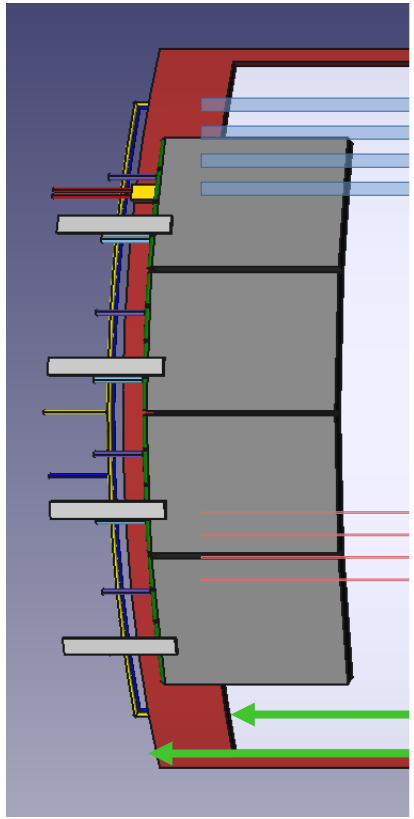
Z = 59 cm

R*phi = 46 cm

Z; (r phi)

C; (z)

return trail for C strips



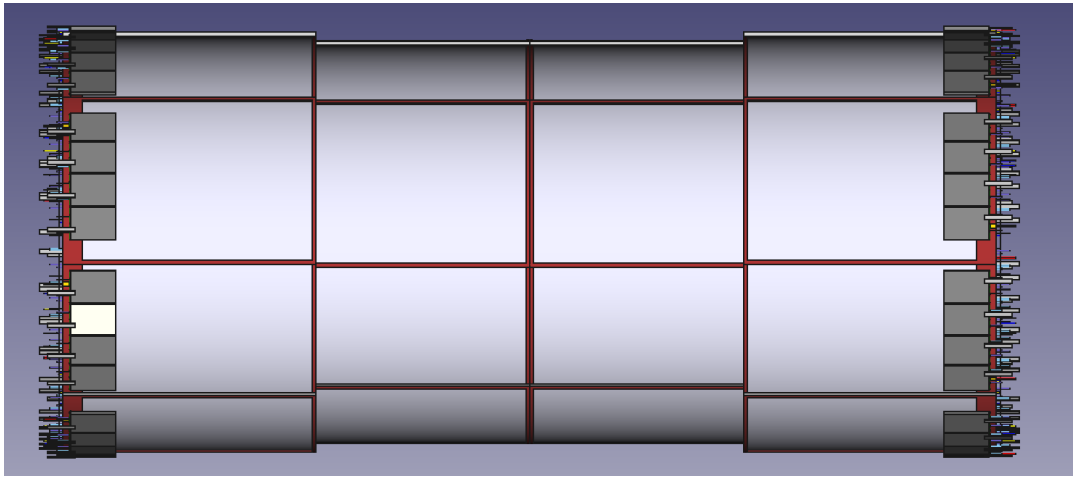
Dimensions:

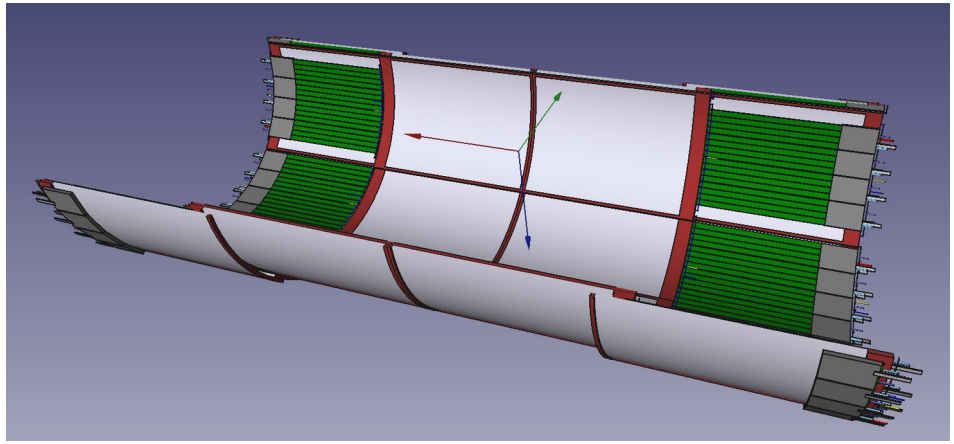
- Size: 65 x 46 cm^2
- Active area: 59x44 cm^2
- r/o strips: ~1 mm pitch in both directions
- Readout strips per module: 1024
- 32 channels per connector → 32 connectors

Services:

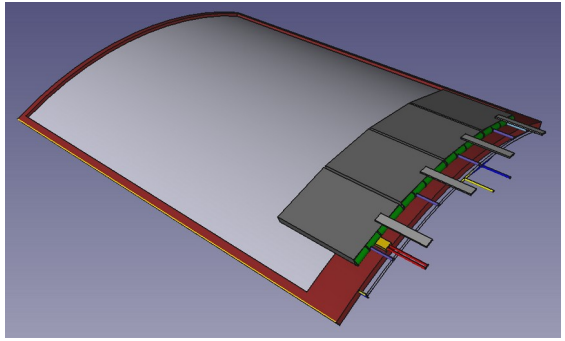
- HV: 2 channels (drift and resistive layer)
- Gas: 2 tubes (in and out)
  - Two tiles can be in series
- 4 FEBs per module
- 4 ASICs per FEB:
  - 1 4-lines bidirectional optical fiber FireFly to RDO
  - 2 short flex cables per ASIC (SALSA)
  - Low voltage
  - Cooling in and out, possibly in series

CyMBaL – Layout

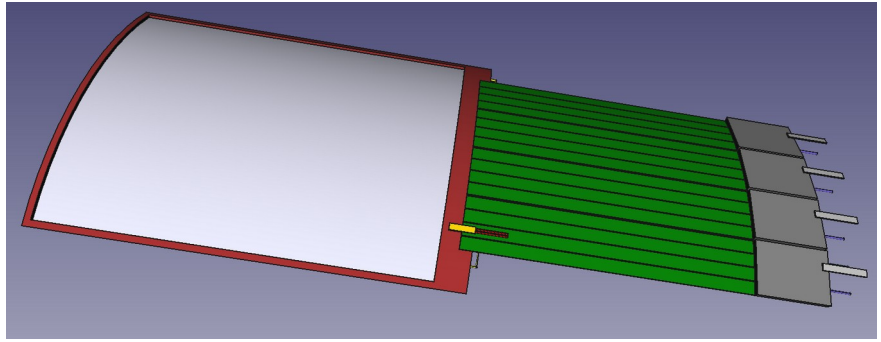




- Four modules in length
- Eight modules in phi
- Overlap in phi and z
- FEB to the periphery
- Inner modules connected to FEB with flex cables



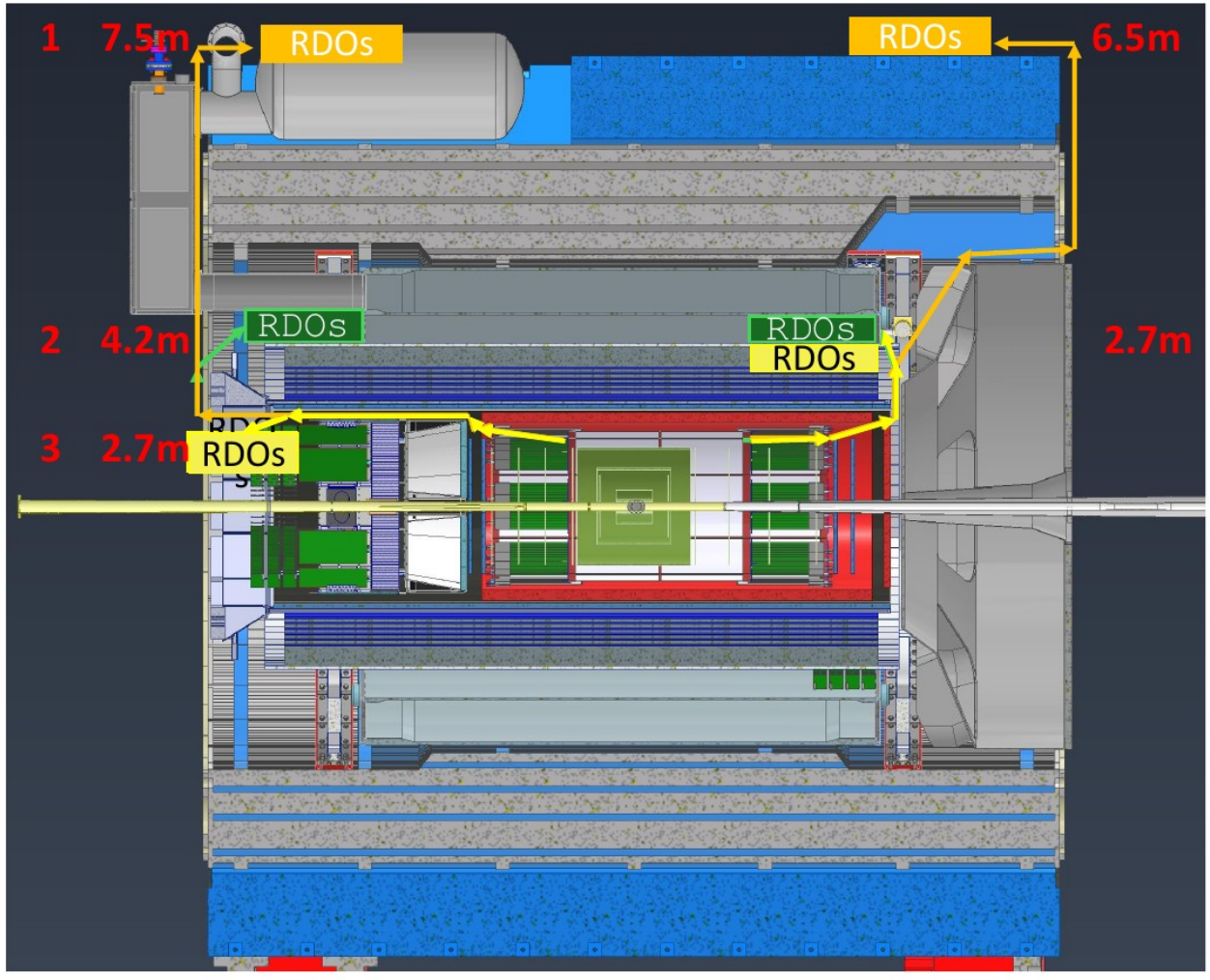
Outer module



Inner module

Options for placing the RDOs

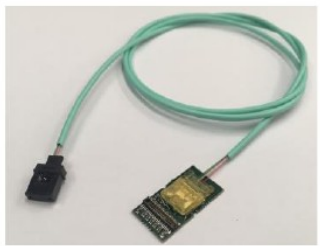
- 3 options
- Option 1 :
  - → Better for installation and maintenance
  - → Better for powering
- Options 1-2-3
  - → Difficult for bulky data cables
    - In addition to services
- Impact on FEB – RDO interface
  - → Optical versus electrical
  - → ASICs per FEB
- Impact on power consumption and cooling



FEB with optical interface: VTRX+

- FE ASICs are directly interfaced to VTRX+
  - → Downlink with embedded clock / sync / async data distributed with high fidelity fan-out
  - → Requires an “innovative” ASIC interface
    - Working on CDR circuitry for Salsa

CERN VTRX+



- FEB
  - → Radiation hardened ASICs
  - → Minimal power consumption after electrical interface option: only VTRX+ consumption added
    - ~ 32-35 mW / channel - 8% increase compared to a FEB with electrical RDO interface
    - 0.9 mm^2 (DC/DC + LDO) or 5.8 mm^2 (LDO only) wires to FEB
- RDO : common hardware