

*We would like to meet with you at this time, to discuss mechanical and electronics/readout integration questions, topics are services, cooling envelope issues and so on.*

*If possible please prepare 2-5 slides summarizing the current status.*

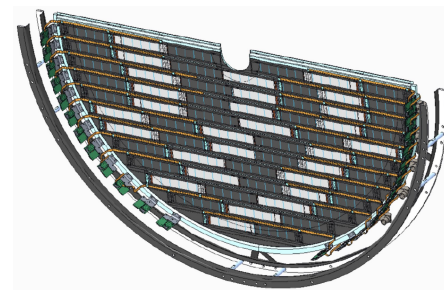
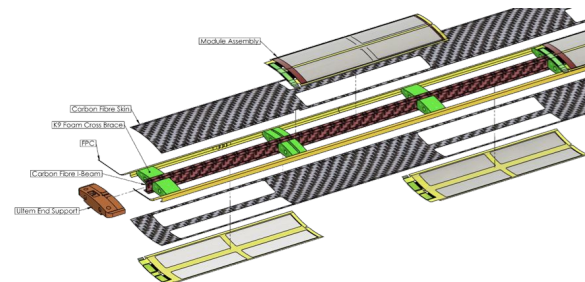
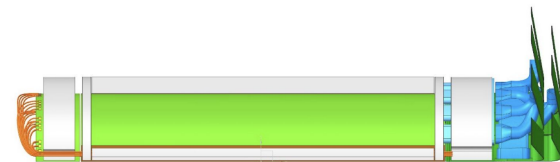
*Please feel free to invite others as you feel it will help the discussion. Everybody is welcome.*

SVT status

# Mechanics

Increasingly realistic CAD designs for IB L0 and L1, OB, and disks

- IB L0 and L1 was one of the main topics at the SVT workfest at Lehigh, c.f. <https://indico.bnl.gov/event/20727/sessions/7434/>
  - IB L2 has been less advanced,
  - OB most recently discussed in the SVT general meeting this past Tuesday, c.f. <https://indico.bnl.gov/event/25115/>
  - Disk design has likewise been worked out further; update at an upcoming SVT general meeting,
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- Initial designs for several of the global supports have been developed, including the support cylinder – its outer radius is the outer envelope (SVT services will be routed inside),
  - Models have been brought together, of course bringing out some interferences (none fundamental). These are being worked through as part of internal integration, c.f. <https://indico.bnl.gov/event/25161/>



# Assembly sequence

- Worked out at the (satellite to the) 12<sup>th</sup> Forum on Tracking Detector Mechanics at Purdue U., c.f. <https://indico.cern.ch/event/1336746/>
- OB: Staves are shipped from the UK to BNL for assembly into L3 and L4
- Disks: US sites will ship half disks to BNL for assembly into electron and hadron endcaps
- IB: INFN will ship assembled L0+L1 half-barrels to BNL
  - L2 half barrel shipped to BNL from MIT (being worked out)
- Assembly at BNL will proceed in halves inside the support half cylinder:
  - From the outside in for the Barrel; L4 first, then L3, then IB (cone will be segmented),
  - From the inside out for the disks; ED0 first and ED4 last,
  - Ordering of ED vs HD is to be determined; it could be a sequence of ED0, HD0 etc. Or, ED0, ED1, .. HD0, HD1, ... (or the other way around),
- Assembled SVT halves are then joined together (including the beampipe),
- Services will enter and exit SVT at max |z|
- Note: this is a change compared to the tracking review in March 2024 and supersedes it.
- **Note added after the meeting:** as discussed during the meeting, SVT continues to prefer segmentation in a top and a bottom half (as opposed to left and right).

# Needs during assembly, maintenance

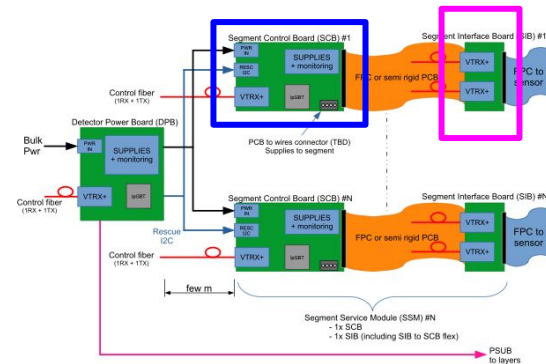
- Clean room (class to be defined) with a length of the beampipe plus margin of  $\sim 3\text{m}$ ; width  $\sim 5\text{m}$ , height  $\sim 3\text{m}$ ,
- Wide access door(s) at one end; personnel access on one or more other sides,
- To include area for reception and storage of IB, OB staves, half disks,
- Capability to lift and move  $\sim 600\text{ kg}$  (? TBC),
- Capability to test – access to power and readout racks, cooling + separated area with cable ducts to clean room and racks (office-like, “DAQ room”),
- Note: *not* factored in – any joint use with MPGD, ToF, etc.  
LAMAT (Laboratory for Assembly of Microelectronics and Testing) idea/initiative, as discussed after HEPIC24, in the instrumentation division BNL (or similar).

# Electronics

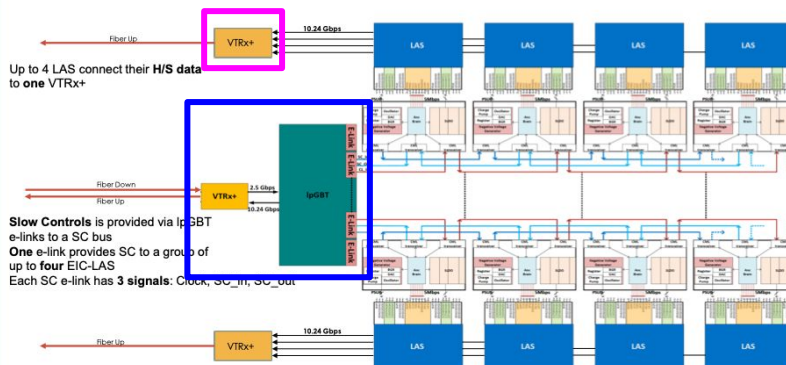
- The SVT will have a set of 4 RDO boards
- **Interface Board**
  - VTRx+ receives data from sensors and sends them via fibers to aggregator board,
  - Close to end of segment (IB), stave ends (OB), and disk outer radii,
  - Tentative dimensions approximately 15x30mm<sup>2</sup> (not wider than a MOSAIX segment),
  - Power estimate from VTRx+: ~100mW
- **Control board**
  - VTRx+ and IpGBT receive control signals on fibers; send them over elinks to AncASIC (OB, disks), or segment (IB),
  - Placement on support cone/cylinder,
  - Tentative dimensions approximately 20x40mm<sup>2</sup> depending connectors,
  - Power estimate from IpGBT and VTRx+: 650mW at 5.12 Gbps,

Graphics from talk by Jo Schambach  
at SVT workfest in July

## IB Readout Architecture



## Outer Barrel and Disk Readout Electronics



- Power board

- Power for RDO boards and IB
- **Aggregator board**
  - Reduces number of fibers between detector and FELIX,
  - Further out, currently thought to be outside of the detector volume

The diagram illustrates the ePIC DAQ system architecture. On the left, the 'Inner Barrel' contains a 'Decoded Chip' (blue rectangle) and a 'Flexible Printed Circuit' (light blue rectangle). The chip is labeled '4x4000' and the circuit is labeled '4x16'. An arrow indicates the length is '< 50 cm long'. The 'Flexible Printed Circuit' is labeled 'Slave(lets)'. The 'Decoded Chip' is connected to the 'Flexible Printed Circuit'. The 'Flexible Printed Circuit' is connected to the 'Readout Electronics' (dashed box). The 'Readout Electronics' contains 'Optical Transmitters' and 'Power Regulators'. The 'Optical Transmitters' are connected to a 'Fiber' line. The 'Fiber' line is connected to a 'Fiber Aggregation Board' (green rectangle). The 'Fiber Aggregation Board' is connected to the 'ePIC DAQ' system. The 'ePIC DAQ' system contains a 'GTU' (General Trigger Unit) and a 'DCS' (Data Control System), both connected to a 'FELIX' (Fiber Event Logic Interface) unit. The 'FELIX' unit is connected to the 'Fiber Aggregation Board'. The 'Fiber Aggregation Board' is also connected to 'Power Infrastructure' (blue rectangle).

Figure 1: Block diagram of the Segment Service Module (SSM) architecture. The diagram illustrates the flow of power and data through various boards and connectors. Key components include:

- Bulk Pwr**: Input power source.
- Detector Power Board (DPB)**: Receives Bulk Pwr and outputs **SUPPLIES + monitoring** and **VTRX+** to the **PCB**.
- Segment Control Board (SCB) #1**: Receives **Control fiber (100x ~ 170x)** and outputs **SUPPLIES + monitoring** and **VTRX+** to the **PCB**.
- Segment Interface Board (SIB) #1**: Receives **Control fiber (100x ~ 170x)** and outputs **VTRX+** to the **PCB**.
- PCB to wires connector (TBD)**: Supplies to segment.
- Segment Control Board (SCB) #N**: Receives **Control fiber (100x ~ 170x)** and outputs **SUPPLIES + monitoring** and **VTRX+** to the **PCB**.
- Segment Interface Board (SIB) #N**: Receives **Control fiber (100x ~ 170x)** and outputs **VTRX+** to the **PCB**.
- FPC or semi rigid PCB**: Connects the SIB to the PCB.
- FPC to sensor**: Connects the SIB to the sensor.
- PSUB to fibers**: Output from the SSM.

[illegible]

# Services – VTRx+

VTRx+ pig-tails connect at the support cylinder to patch-harnesses that end in patch panels (MTP12) at or near max-|z|; the necessary pig-tail length(s) remain to be determined – we assume a similar approach is or will be taken in other VTRx+ use cases in ePIC,

VTRx+ needs 1.2V, 2.5V, and I2C – this likely holds across all use cases in ePIC and may benefit from a common approach. Associated services will need to be folded into the overall service update.



# Services

Series of writeups available in sharepoint ([link](#)). Main evolution discussed at the Lehigh workfest, c.f. <https://indico.bnl.gov/event/20727/sessions/>

In a nutshell, compared to the most recent writeup:

- SVT overall configuration is unchanged; 3 inner barrel layers, 2 outer barrel layers, 5 disks on either side of the interaction point; overall dimensions,
- Sensor (number) estimates continue to hold – see e.g. Jo Schambach's talk at the lpGBT/VTRx+ FDR,
- Sensor power dissipation estimates have changed from the previously assumed 1W per left endcap (for a total of a 4kW subsystem) – estimating the increase, however, is currently not straightforward and has knock-on effects e.g. on cooling; update on sensor power dissipation estimates at an upcoming SVT general meeting,
- Ancillary IC power dissipation is now known to be non-negligible – similar holds here as for the sensor power estimate,
- Better knowledge exists for the serial powering chain in L3; the estimate for the disks on this point can also be refined,
- In our current baseline design, the ancillary IC supplies the bias voltages,
- Power needs for VTRx+ and lpGBT are known, though 1.2, 2.5V, I2C remains open,
- Grounding remains partially open,
- Cooling – more is known, but open questions remain in particular on the power and power densities of EIC-LAS and the ancillary IC. Space-wise, this of course continues to be significant in the case of air-cooling. The recent DAC comment to further work out liquid cooling in strategic places will of course be followed.