Digital Control Special Run Proposal

RIKEN/RBRC

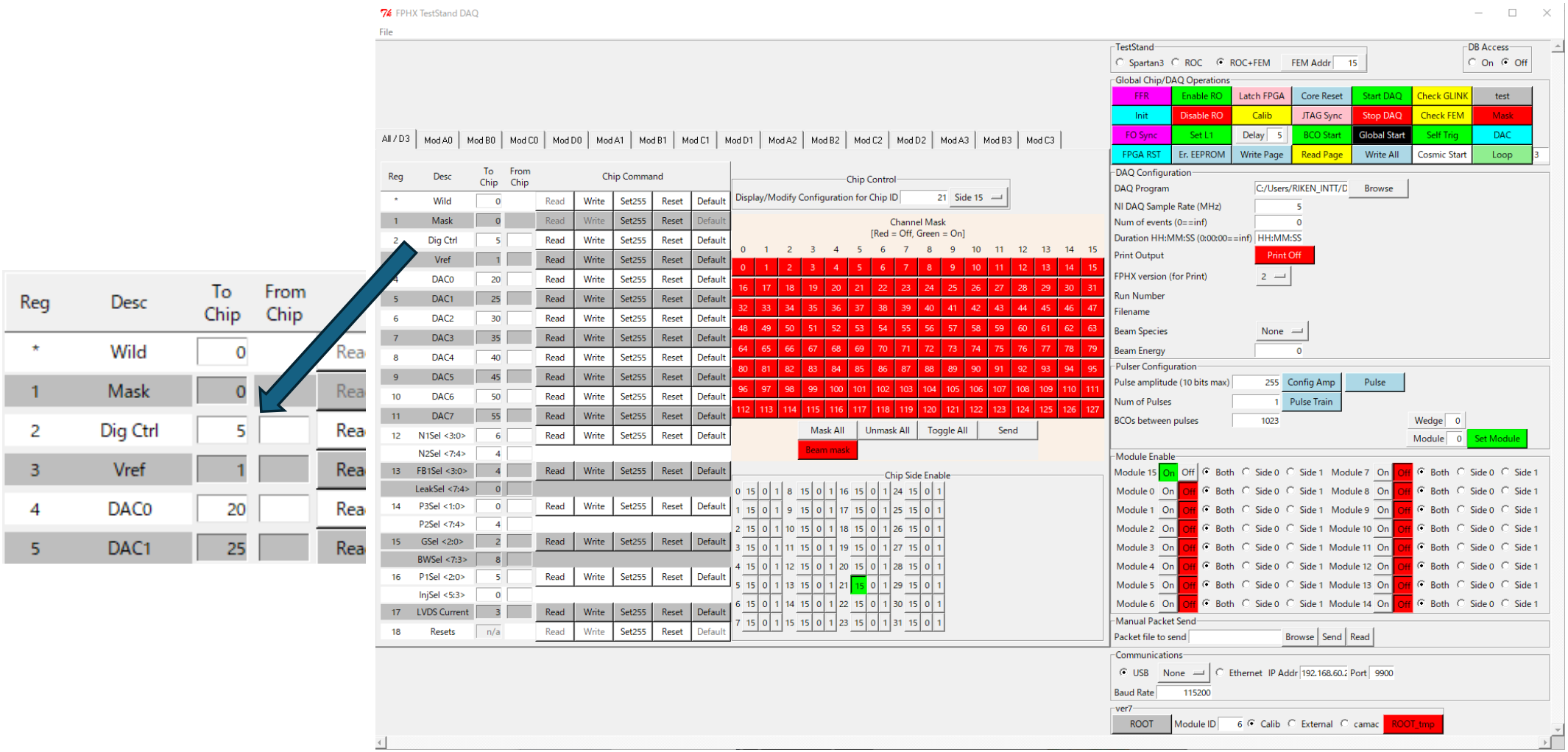
Itaru Nakagawa on behalf of

Takahiro Kikuchi, Yusuke Fujino, Hayato Yanagawa, Tomoki Hrada

The registers, their addresses and defaults are shown in .

Table 2 - Register Addresses and Defaults

Address	Name	Bits	Default	Notes
1	Mask	N/A	N/A	Set Command = Mask Channel Reset Command = Unmask Channel Data bits D6-D0 = Channel Address Data bit D7 = Global Command (i.e. Mask all channels or Unmask all channels)
2	Digital Control	7:0	1	Bit 0 = Active Serial Lines (1=Two, 0=One) Bit 1 = Accept (1=Accept Hits, 0=Reject) Bit 2 = Global Inject Enable Bit 3 = Serial Output Order
3	Vref	1:0	1	
4	Threshold DAC 0	7:0	8	
5	Threshold DAC 1	7:0	16	
6	Threshold DAC 2	7:0	32	
7	Threshold DAC 3	7:0	48	
8	Threshold DAC 4	7:0	80	
9	Threshold	7:0	112	



The digital control=5 is actually overwritten by 7 at Enable RO process.

Digital Control Proposed Parameters

Function	Serial Out Order	Global Injection Enable	1:Accept 0:Reject Hits	Active Serial Line 1:Two 0:One	Decimal
Bit	3	2	1	0	
Nevis GUI Default	0	1	0	1	5
Tested Pattern w/ Noise	1	1	0	0	10
	0	1	0	0	2
Calibration Default	0	1	1	1	7
For Calibration	1	1	0	0	12
	0	1	0	0	4
For Beam Data Taking	1	0	1	0	**10**
	0	0	1	0	**2**

Required Statistics

- 100 counts/chip should be able to distinguish half entries ~50 within more than 3 sigma systematic precision.
- This yields 100x26chipx14module=73k hits/FELIX
- 73k/FELIX x 8FELIX = 0.6 Mhits/INTT
- With contingency factor x10 ~ 6MHits/INTT/Run should be OK.