

Digital Control Special Run Proposal

RIKEN/RBRC

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The registers, their addresses and defaults are shown in [in](#).



Table 2 - Register Addresses and Defaults

Address	Name	Bits	Default	Notes
1	Mask	N/A	N/A	Set Command = Mask Channel Reset Command = Unmask Channel Data bits D6-D0 = Channel Address Data bit D7 = Global Command (i.e. Mask all channels or <u>Unmask</u> all channels)
2	Digital Control	7:0	1	Bit 0 = Active Serial Lines (1=Two, 0=One) Bit 1 = Accept (1=Accept Hits, 0=Reject) Bit 2 = Global Inject Enable Bit 3 = Serial Output Order
3	Vref	1:0	1	
4	Threshold DAC 0	7:0	8	
5	Threshold DAC 1	7:0	16	
6	Threshold DAC 2	7:0	32	
7	Threshold DAC 3	7:0	48	
8	Threshold DAC 4	7:0	80	
9	Threshold	7:0	112	

74 FPHX TestStand DAQ

File

All / D3 Mod A0 Mod B0 Mod C0 Mod D0 Mod A1 Mod B1 Mod C1 Mod D1 Mod A2 Mod B2 Mod C2 Mod D2 Mod A3 Mod B3 Mod C3

Reg	Desc	To Chip	From Chip	Chip Command
*	Wild	0		Read Write Set255 Reset Default
1	Mask	0		Read Write Set255 Reset Default
2	Dig Ctrl	5		Read Write Set255 Reset Default
3	Vref	1		Read Write Set255 Reset Default
4	DAC0	20		Read Write Set255 Reset Default
5	DAC1	25		Read Write Set255 Reset Default
6	DAC2	30		Read Write Set255 Reset Default
7	DAC3	35		Read Write Set255 Reset Default
8	DAC4	40		Read Write Set255 Reset Default
9	DAC5	45		Read Write Set255 Reset Default
10	DAC6	50		Read Write Set255 Reset Default
11	DAC7	55		Read Write Set255 Reset Default
12	N1Sel <3:0>	6		Read Write Set255 Reset Default
	N2Sel <7:4>	4		
13	FB1Sel <3:0>	4		Read Write Set255 Reset Default
	LeakSel <7:4>	0		
14	P3Sel <1:0>	0		Read Write Set255 Reset Default
	P2Sel <7:4>	4		
15	GSel <2:0>	2		Read Write Set255 Reset Default
	BWSel <7:3>	8		
16	P1Sel <2:0>	5		Read Write Set255 Reset Default
	InjSel <5:3>	0		
17	LVDS Current	3		Read Write Set255 Reset Default
18	Resets	n/a		Read Write Set255 Reset Default

Chip Control

Display/Modify Configuration for Chip ID: 21 Side 15

Channel Mask (Red = Off, Green = On)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127

Mask All Unmask All Toggle All Send

Beam mask

Chip Side Enable

0	15	0	1	8	15	0	1	16	15	0	1	24	15	0	1
1	15	0	1	9	15	0	1	17	15	0	1	25	15	0	1
2	15	0	1	10	15	0	1	18	15	0	1	26	15	0	1
3	15	0	1	11	15	0	1	19	15	0	1	27	15	0	1
4	15	0	1	12	15	0	1	20	15	0	1	28	15	0	1
5	15	0	1	13	15	0	1	21	15	0	1	29	15	0	1
6	15	0	1	14	15	0	1	22	15	0	1	30	15	0	1
7	15	0	1	15	15	0	1	23	15	0	1	31	15	0	1

TestStand

Spartan3 ROC ROC+FEM FEM Addr 15 DB Access On Off

Global Chip/DAQ Operations

FFR	Enable RO	Latch FPGA	Core Reset	Start DAQ	Check GLINK	test
Init	Disable RO	Calib	JTAG Sync	Stop DAQ	Check FEM	Mask
FO Sync	Set L1	Delay 5	BCO Start	Global Start	Self Trig	DAC
FPGA RST	Er. EEPROM	Write Page	Read Page	Write All	Cosmic Start	Loop

DAQ Configuration

DAQ Program C:/Users/RIKEN_INTT/D Browse

NI DAQ Sample Rate (MHz) 5

Num of events (0==inf) 0

Duration HH:MM:SS (0:00:00==inf) HH:MM:SS

Print Output Print Off

FPHX version (for Print) 2

Run Number

Filename

Beam Species None

Beam Energy 0

Pulsar Configuration

Pulse amplitude (10 bits max) 255 Config Amp Pulse

Num of Pulses 1 Pulse Train

BCOs between pulses 1023 Wedge 0 Module 0 Set Module

Module Enable

Module 15 On Off Both Side 0 Side 1 Module 7 On Off Both Side 0 Side 1

Module 0 On Off Both Side 0 Side 1 Module 8 On Off Both Side 0 Side 1

Module 1 On Off Both Side 0 Side 1 Module 9 On Off Both Side 0 Side 1

Module 2 On Off Both Side 0 Side 1 Module 10 On Off Both Side 0 Side 1

Module 3 On Off Both Side 0 Side 1 Module 11 On Off Both Side 0 Side 1

Module 4 On Off Both Side 0 Side 1 Module 12 On Off Both Side 0 Side 1

Module 5 On Off Both Side 0 Side 1 Module 13 On Off Both Side 0 Side 1

Module 6 On Off Both Side 0 Side 1 Module 14 On Off Both Side 0 Side 1

Manual Packet Send

Packet file to send Browse Send Read

Communications

USB None Ethernet IP Addr 192.168.60.2 Port 9900

Baud Rate 115200

ver7

ROOT Module ID 6 Calib External camac ROOT_tmp

The digital control=5 is actually overwritten by 7 at Enable RO process.

Digital Control Proposed Parameters

Function	Serial Out Order	Global Injection Enable	1:Accept 0:Reject Hits	Active Serial Line 1:Two 0:One	Decimal
Bit	3	2	1	0	
Nevis GUI Default	0	1	0	1	5
Tested Pattern w/ Noise	1	1	0	0	10
	0	1	0	0	2
Calibration Default	0	1	1	1	7
For Calibration	1	1	0	0	12
	0	1	0	0	4
For Beam Data Taking	1	0	1	0	10
	0	0	1	0	2

Required Statistics

- 100 counts/chip should be able to distinguish half entries ~ 50 within more than 3 sigma systematic precision.
- This yields $100 \times 26 \text{ chip} \times 14 \text{ module} = 73\text{k hits/FELIX}$
- $73\text{k/FELIX} \times 8\text{FELIX} = 0.6 \text{ Mhits/INTT}$
- With contingency factor $\times 10 \sim 6\text{MHits/INTT/Run}$ should be OK.