Salsa – lpGBT interface : Feasibility and constraints

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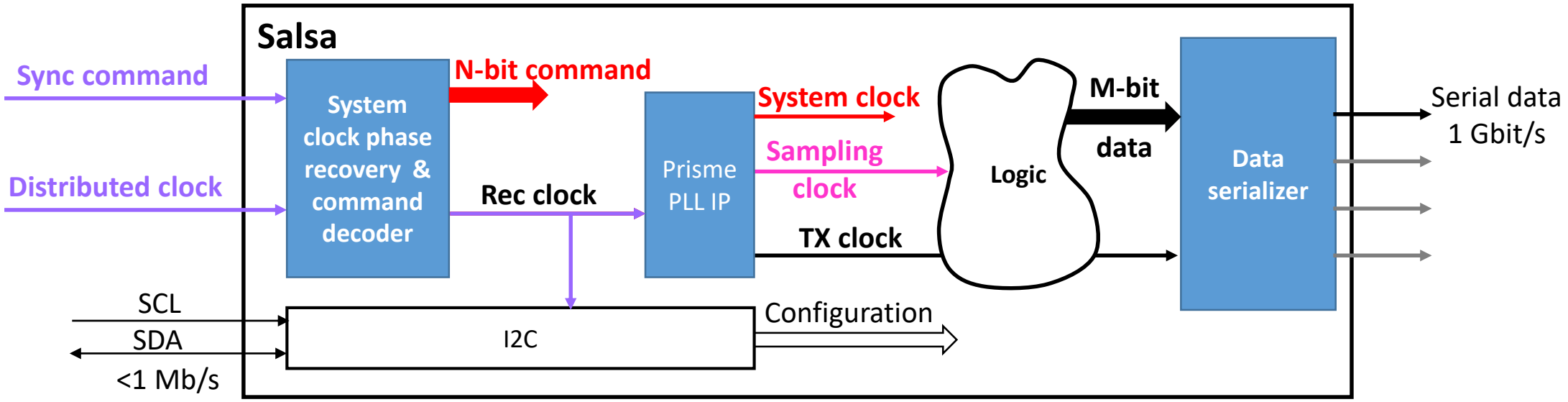
Outlook

- Interface with lpGBT
  - → Clocks
  - → Synchronous commands
  - → Data
- Backend FPGA (ROD, DAM) interface
- System
  - → MPGD readout options
- Backup
  - → Reminder : Salsa’s direct interface with VTRX+

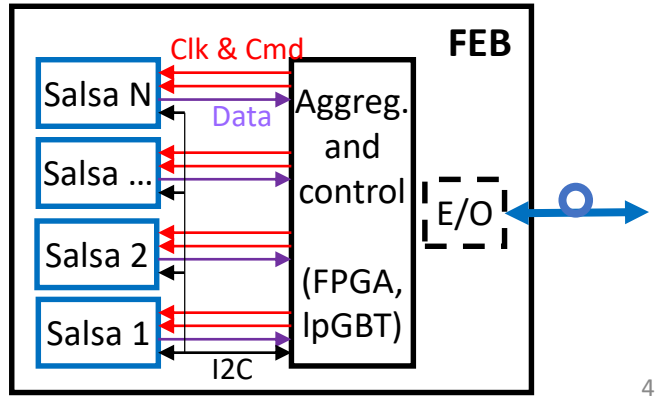
lpGBT Interface

Support of “traditional” prevalent interface

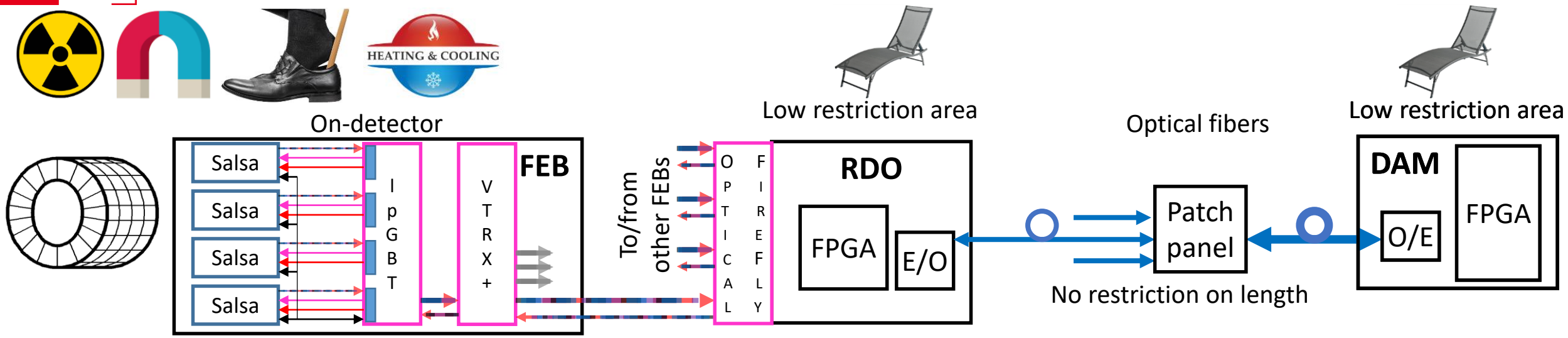


- Important number of heterogeneous external interface signals proper for each functionality
  - → Clock_diff_in, SynCmd_diff_in
    - Synchronous commands decoding options in backup
  - → SCL_in, SDA_io
    - Configuration of ASICs on a FE board in series : longer startup and recovery times
  - → Up to 4 Data_diff_out serial links
  - → Additional IOs like Trigger_diff_in, TrigPrim_diff_out

- Most adapted for FEB with an on-board companion intelligence
  - → for control & aggregation



FEB based on Salsa's heterogeneous interface with lpGBT

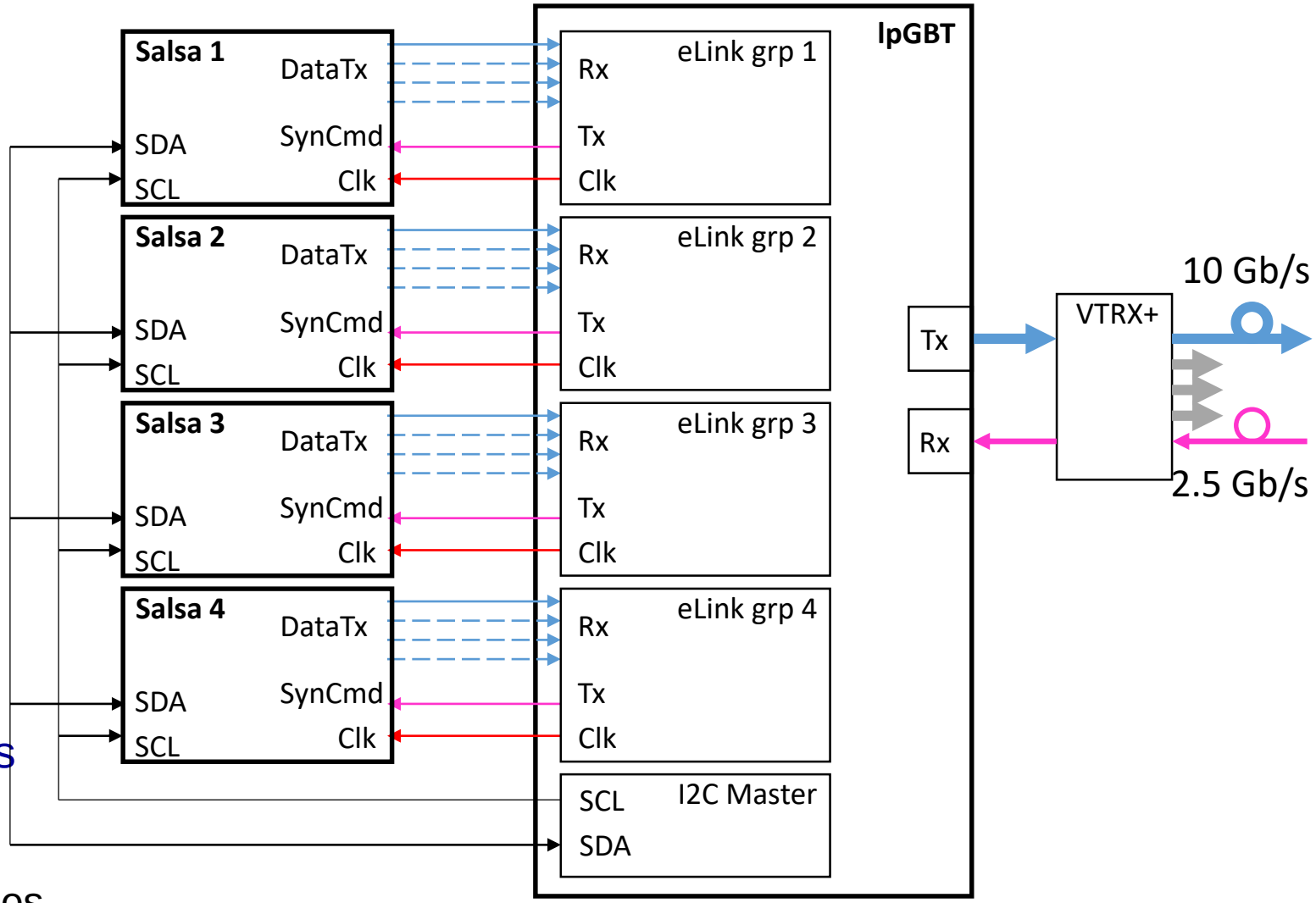


- 256-channel FEB
  - → Salsa receives recovered clock and sync data from an lpGBT eLink group
  - → Salsa sends physics, calibration and monitoring data to a number of lpGBT lines of the eLink group
  - → Salsa's are configured over daisy chained I2C interface from lpGBT
  - → lpGBT provide a bidirectional interface between 4 Salsas and remote FPGA on RDO
  - → VTRX+ is used with only one TX line
  - → All ASICs are radiation hard

- 1024-channel RDO : common hardware with adaptation based on FireFly transceivers from Samtec
  - Single 4-lane bidirectional FireFly is enough to serve 4 FEBs
  - → Placed anywhere in user friendly area
  - No particular restrictions on power consumption, cooling infrastructure, radiation, magnetic field

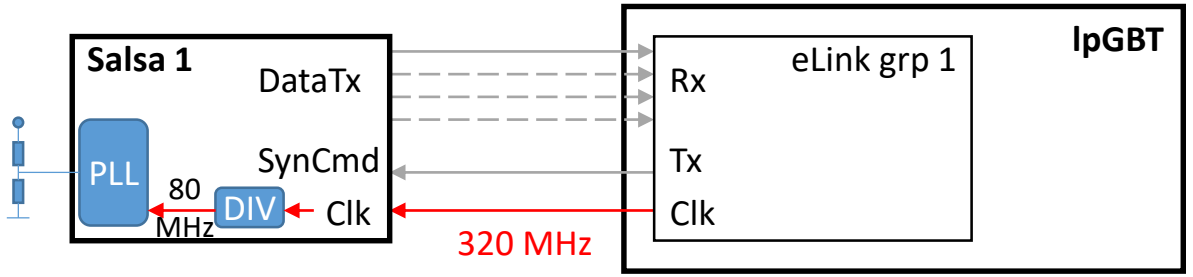
FEB based on Salsa's heterogeneous interface with lpGBT

- 4 Salsa-s per FEB
  → 256 channels
- 4 lpGBT eLink groups
  → For data, clock, synchro
  → An eLink group / Salsa
- I2C chain for configuration
- lpGBT GPIO and analog peripherals
  → Control / monitor IO pins of Salsa
    - Reset, PLL lock, error, etc.
  → Control / monitor on board resources
    - ADC, DAC



Clock

- Salsa can be configured to operate in CERN clock environment
  - → Via external pins
  - → Prisme PLL IP accepts 80 MHz clock
  - → What can be input clock frequency and divider ?
    - 80 MHz : divider 1
    - 160 MHz : divider 2
    - 320 MHz : divider 4



→ Anyway, whatever is eLink clock frequency, EIC clock is in phase with eLink clock every 5th tick

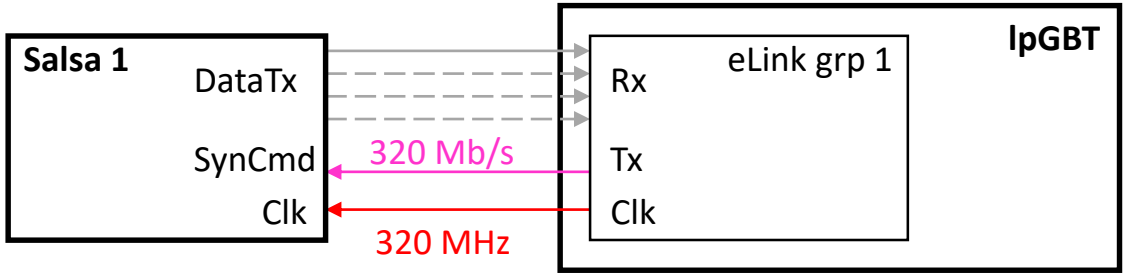
EIC cllk 100 MHz	10 ns				10 ns				10 ns				10 ns				10 ns		
40 MHz	25 ns								25 ns										
80 MHz	12.5 ns				12.5 ns				12.5 ns				12.5 ns						
160 MHz	6.25 ns		6.25 ns		6.25 ns		6.25 ns		6.25 ns		6.25 ns		6.25 ns		6.25 ns				
320 MHz	3.125 n	3.125 n	3.125 n	3.125 n	3.125 n	3.125 n	3.125 n	3.125 n	3.125 n	3.125 n	3.125 n	3.125 n	3.125 n	3.125 n	3.125 n	3.125 n			

- 320 MHz eClock is the preferred option
  - → See the following

Synchronous commands

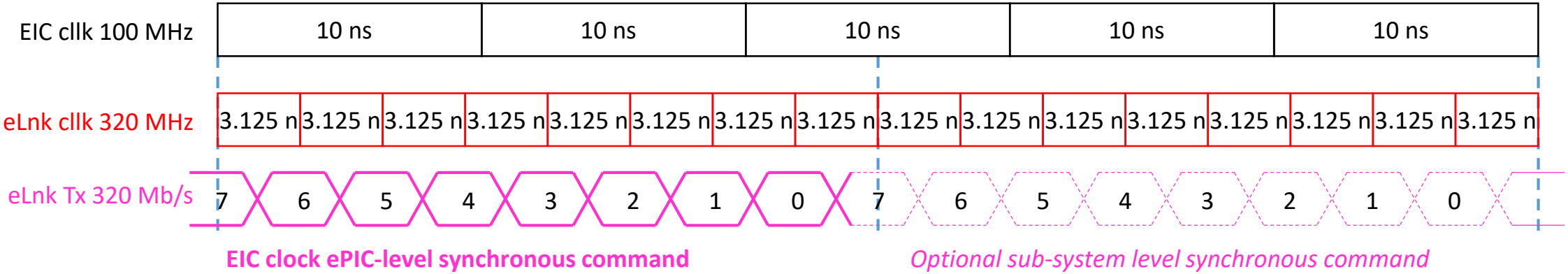
- Some ePIC-wide commands should be in phase with EIC clock (if not all)
  - *e.g.* RevTick (BC0), Sync…

  → They should be distributed every 5th EIC clock that is in phase with eLink clock
  - Meaning there are always at least 50 ns between 2 EIC machine synchronous commands
    - Up to 240 commands per EIC revolution – should be enough



- Option of 320 MHz eLink clock and 320 Mbit/s downlink

  → Allows to decode a large number of synchronous commands from 8-bit wide received word
  - And to recover the base 40 MHz clock

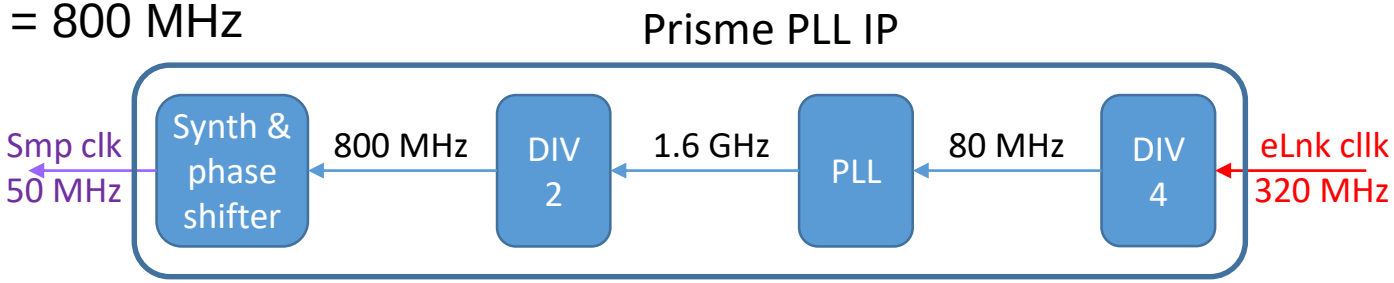


- Note : an additional sub-system specific command can be sent within the same 5 EIC clock period

  → e.g. Tx link realign, fire internal pulser, calibrate, …

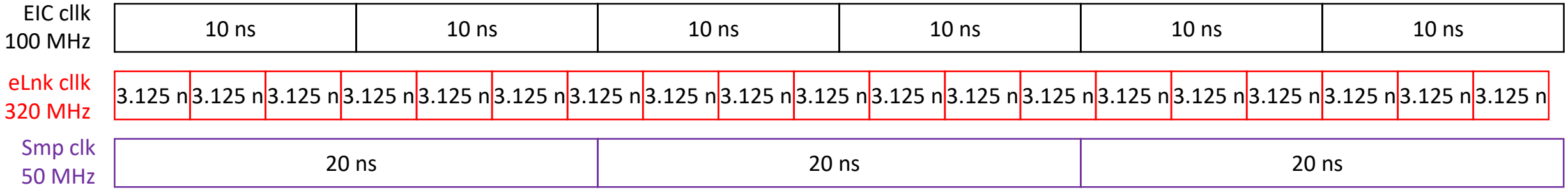
Sampling

- With lpGBT recovered clock, the reference clock frequency of Salsa's Prisme PLL is 80 MHz
  - → Divider 4 for 320 MHz eLink clock
  - → The PLL produces 1.6 GHz clock out of 80 MHz
  - → Clock synthesizer operates at 1.6 GHz / 2 = 800 MHz

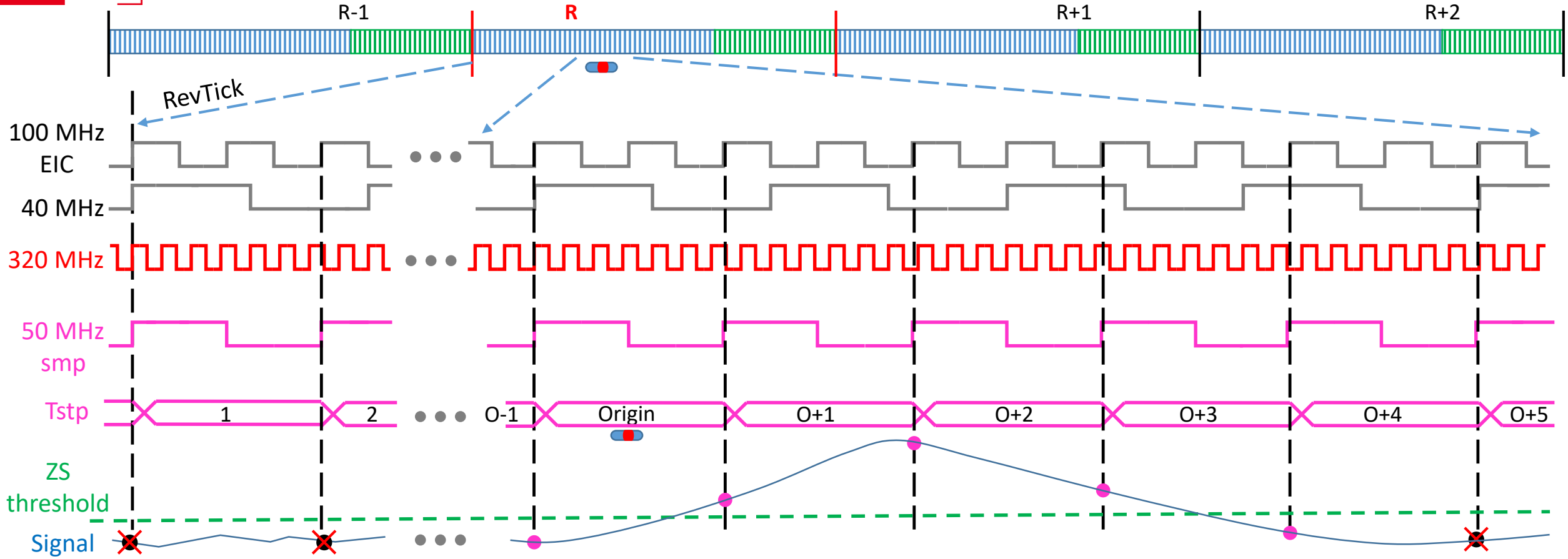


- Sampling clock is derived by dividing 800 MHz synthesizer clock
  - → 50 MHz : divider 16
    - Reminder: this frequency is the baseline when working with 100 MHz distributed system clock

- Despite of 320 MHz distributed clock, looks like sampling can still be done at 50 MHz
  - → And samples can be tagged with timestamps from EIC revolution ticks – being in "natural" EIC time units



Signal timing



- Periodic “Sync” command generated when EIC and 40 MHz clocks are in phase
  - → RevTick in this example
  - → Allows phase alignment and monitoring of clocks within Salsa
- In this example Salsa is programmed to keep one sample before and after threshold crossing
  - → Salsa data for the signal : Tstp(O-1) Smp(O-1) Smp(Origin) Smp(O+1) Smp(O+2) Smp(O+3)

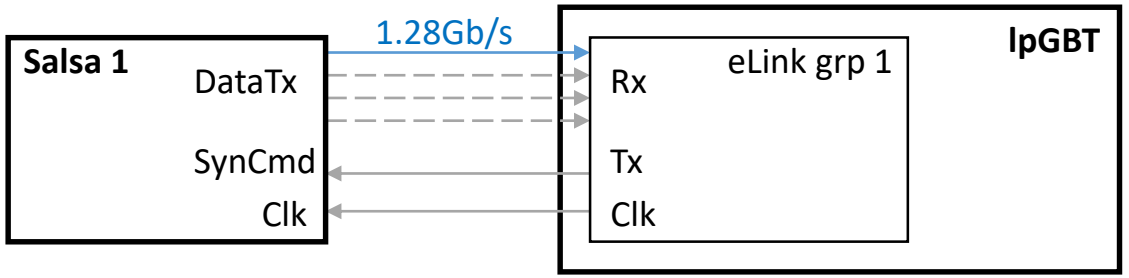
Data Tx

- Salsa output bandwidth for ePIC : < 400 Mbit/s
  → Direct VTRX+ interface provides single 1 Gbit/s link for data communications

- lpGBT : operate with FEC5 or FEC12 10 Gbit/s uplink
  → More than fine for mild radiation environment of EIC
  → FEB-RDO roundtrip monitoring capability

- Salsa has 4 serial links with ~1 Gbit/s bandwidth

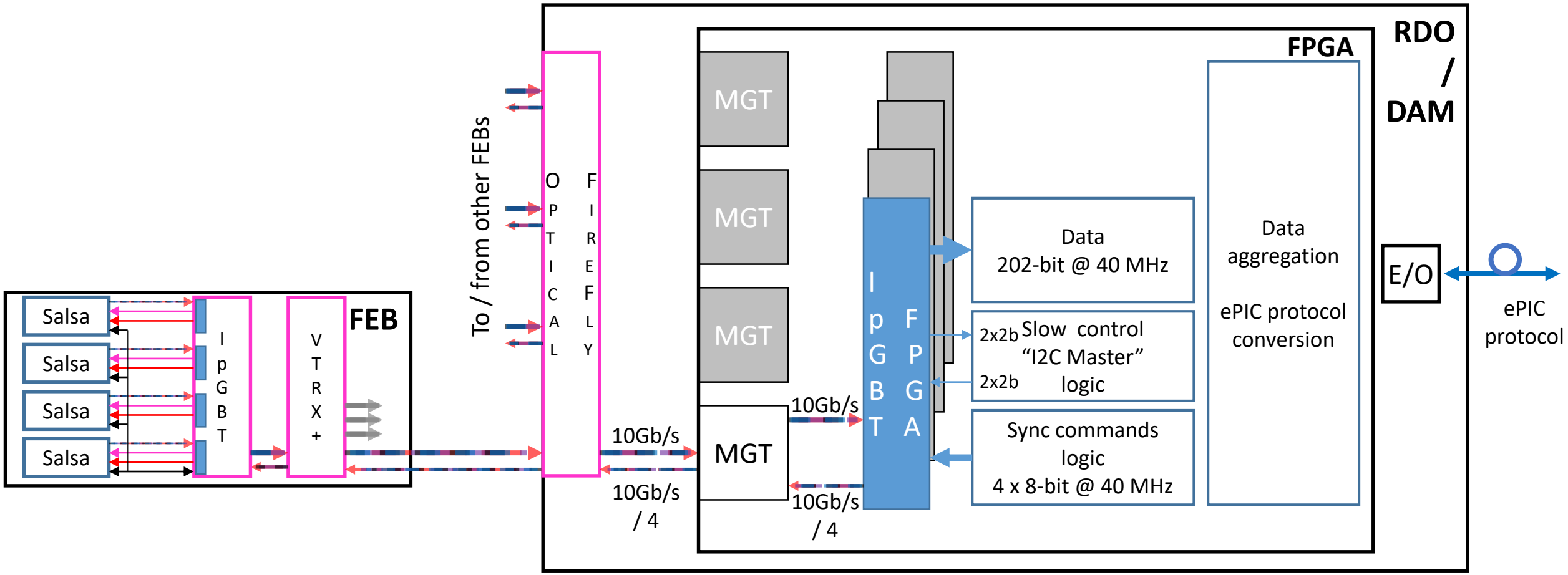
- 3 options to consider for connectivity with lpGBT
  → Four 320 Mbit/s links per ASIC
    - 16 links for all 4 ASICs out of 24 available
  → Two 640 Mbit/s links per ASIC
    - 8 links for all 4 ASICs out of 12 available
  → Single 1280 Mbit/s link per ASIC
    - 4 links for all 4 ASICs out of 6 available
    - Assuming this throughput is stably supported by Salsa



- Current preferred option : single 1280 Mbit/s link
  → Assessing the feasibility

RDO (DAM) Interface

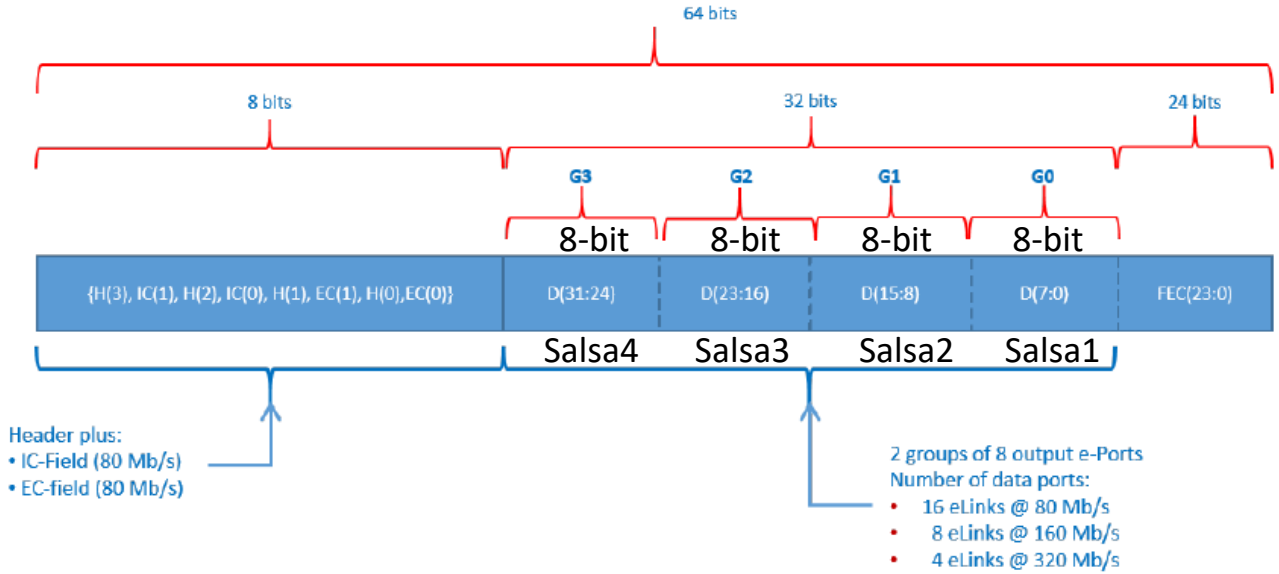
lpGBT – backend FPGA communication



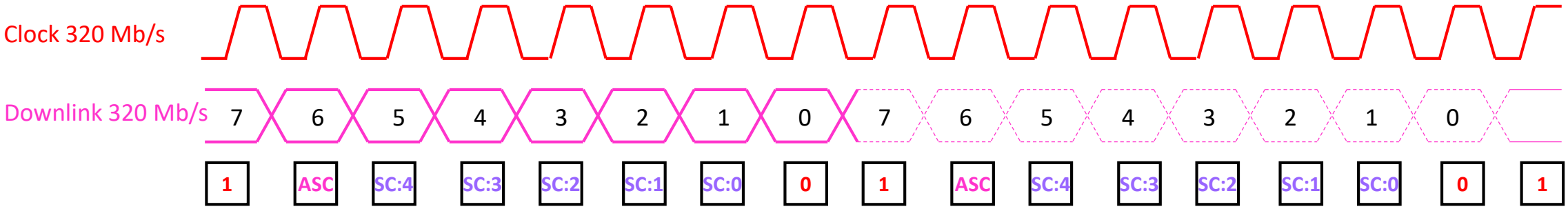
- lpGBT-FPGA IP from CERN on backend FPGA to communicate with lpGBT on FEB
  - → Four 8-bit @ 40 MHz synchronous commands transparently delivered to 4 Salsas over 4 eLink groups
    - It is one of the possibilities – may allow parallel communication with Salsas
      - Others possibilities (*e.g.* port mirroring) not discussed
  - → Data from Salsa are 32-bit wide words => 128 bits for 4 Salsas out of 202 bits
  - → I2C configuration of Salsas over lpGBT IC/EC channel

Downlink from RDO / DAM FPGA to lpGBT and Salsa

- lpGBT-FPGA IP downlink interface
  - → Input from FPGA fabric:
    - 32-bit user data
    - 2-bit EC data
    - 2-bit IC data



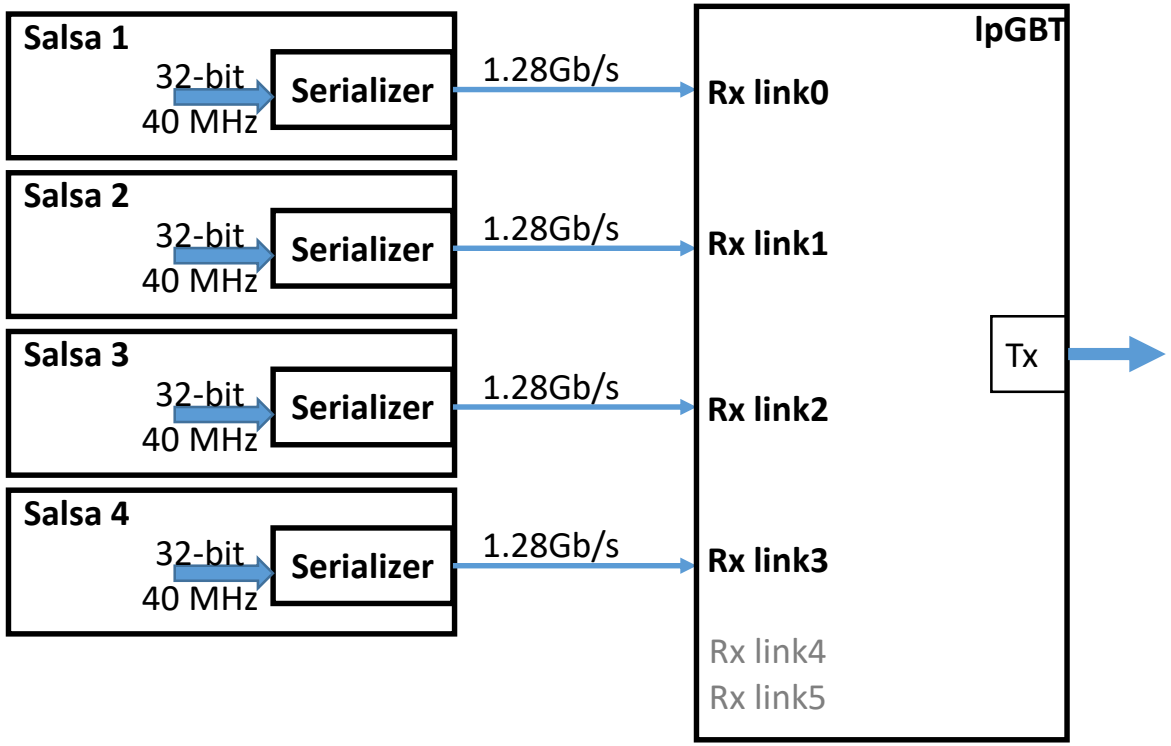
- Salsa clock and data downlink recovered from lpGBT



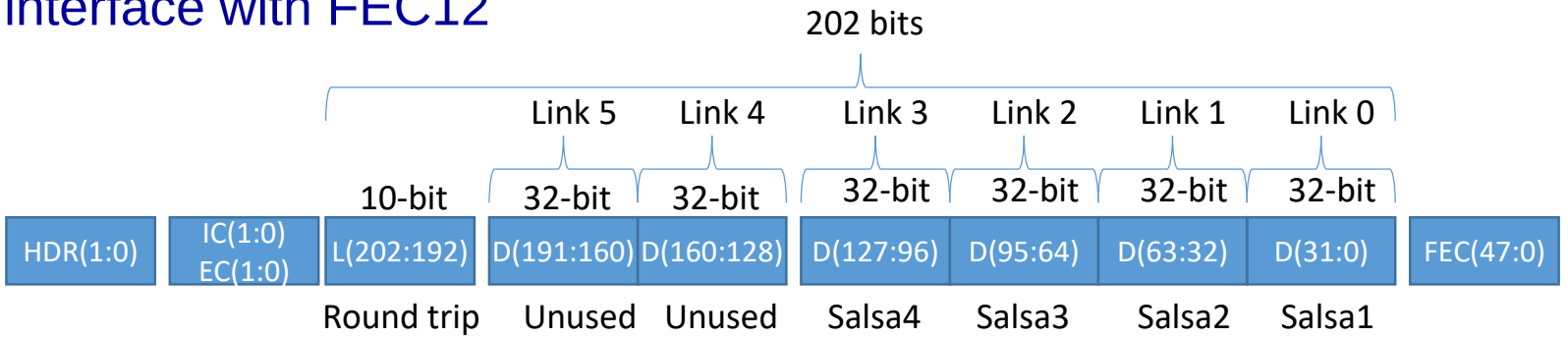
  - → 5-bit fast commands
    - As for direct VTRX+ interface
  - → If clever enough, might try using 1 bit to decode asynchronous slow control commands – 40 Mb/s channel
    - As for direct VTRX+ interface

Uplink from Salsa and lpGBT to RDO / DAM FPGA

- Salsa
  - → Produces 32-bit words @ 40 MHz
    - IDLE word when no user data to be sent
  - → Data is serialized @ 1.28 Gb/s
- lpGBT
    - 4 out of 6 1.28 Gbit/s links are used
  - → Recovers 32-bit words from Salsas
  - → Forms 256 word including IC/EC and other data
  - → Sends them over 10 Gbit/s link



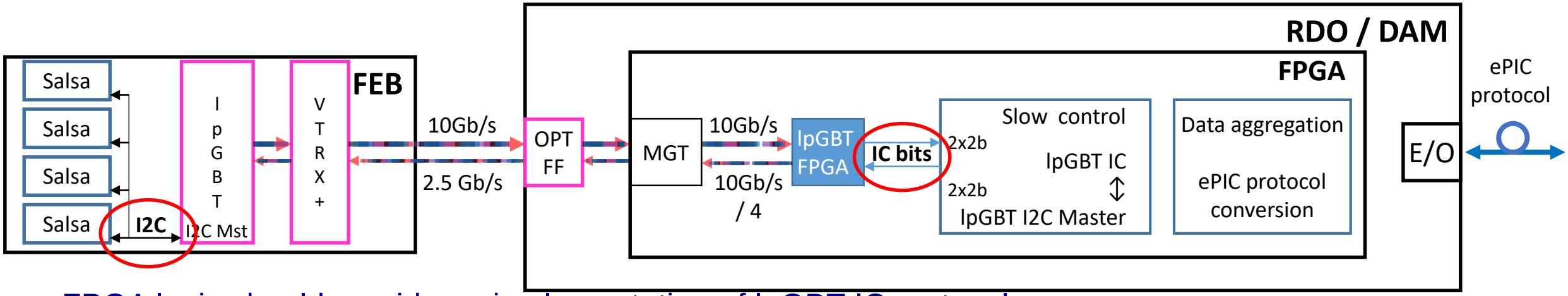
- lpGBT-FPGA IP 10 Gbit/s uplink interface with FEC12
  - → Output to FPGA fabric:
    - 202-bit user data
    - 2-bit EC data
    - 2-bit IC data



  - → 32-bit words from Salsas recovered in the same order as they have been sent

Configuration

- Use lpGBT IC serial channel to produce I2C transactions with Salsas
  - → IC – Internal Control – provides 80 Mb/s line to program lpGBT registers
  - → A set of registers is dedicated to exercise I2C Master port(s) of lpGBT
  - → Various flavors of I2C read and write operations supported
    - Single byte reads or write, multi byte reads or writes, RdModWr, etc.



- FPGA logic should provide an implementation of lpGBT IC protocol
  - → Frame based read-write and read-only commands
    - Constructed by 2-bit @ 40 MHz

- Somewhat long sequence of steps per unitary I2C transaction
  - → Configuration of sub-systems may take considerable time
- Same mechanism to control GPIO pins and environmental analog circuitry (DAC, ADC)

ePIC backend FPGA responsibility

- Derive from ePIC protocol a downstream link per Salsa
  - lpGBT option : 320 MHz clock and 320 Mbit/s downlink
  - Direct VTRX+ option : unified 1 Gbit/s link embedding 100 MHz clock and synchronous commands

  → Salsa will implement ~30 synchronous commands
  - Overlap with ePIC fast synchronous commands must be found
  - ePIC protocol must allow deriving synchronous commands that will guide Salsa's state machine
    - *e.g.* start / stop data taking, Resync, RevTic (BC0), Calib, ResyncTxLink, etc.

- Receive and aggregate uplink data from Salsas
  - lpGBT option : 1.28 Gb/s uplink (link rate to be confirmed)
  - Direct VTRX+ option : 1 Gbit/s uplink

  → Salsa will mix physics / calibration data with slow control / monitoring data
  - The packets of different nature must be separated for on-line processing of physics data
  - Usually some "firmware" checks are done of the integrity of received data (*e.g.* synchronization)
  - Error recovery must be present

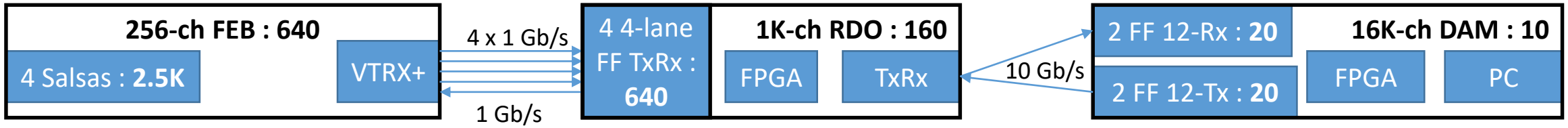
- Configuration and monitoring
  - lpGBT option : sequential configuration of Salsas via I2C transactions over IC channel
  - Direct VTRX+ option : parallel configuration of Salsas via 100 Mb/s config channel in the unified interface

Summary

- With today's knowledge and advancement in Salsa development lpGBT-based FEB seems possible
  - → 320 MHz / 320 Mb/s downlink
  - → 1.28 Gbit/s uplink – to be confirmed
  - → I2C configuration
  - → 50 MHz sampling possible
- FEB on-board control and monitoring over lpGBT Digital GPIO and analog DAC, ADC
  - → Direct VTRX+ option : requires extra functionality from Salsa or extra on-board circuitry
- FEB and RDO-adaptation circuitry become 10 Gbit/s grade
  - → FEB becomes high density grade as well
  - → Direct VTRX+ option : 1 Gbit/s grade
- Power comparison between two options will come later
  - → lpGBT overhead expected to be low
- Implementation
  - → lpGBT option : proven lpGBT-FPGA IP provided by CERN for deployment in backend FPGA
  - → Direct VTRX+ option : Salsa-FPGA IP will be provided by Salsa team

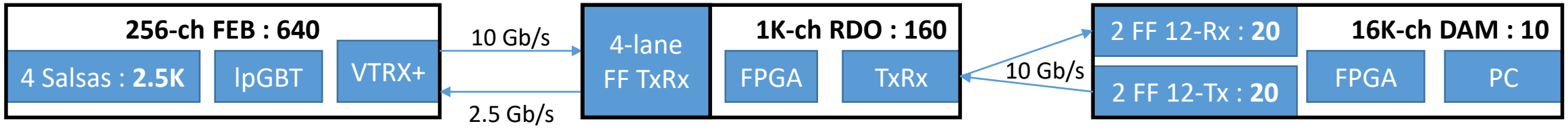
160K-ch MPGD readout configurations and component count

- FEB with direct Salsa-VTRX+ interface



Low density 1 Gb/s grade

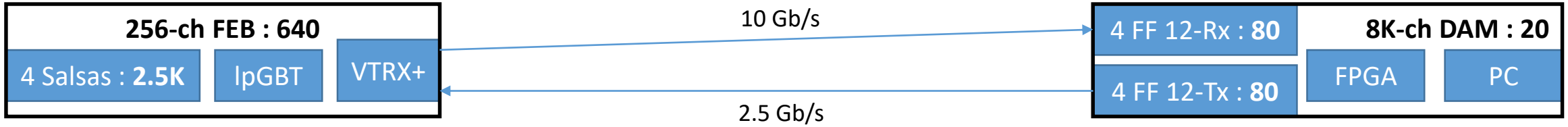
- FEB with lpGBT-VTRX+ interface



High density 10 Gb/s grade

4 times less 4-lane FF

- FEB with direct DAM interface



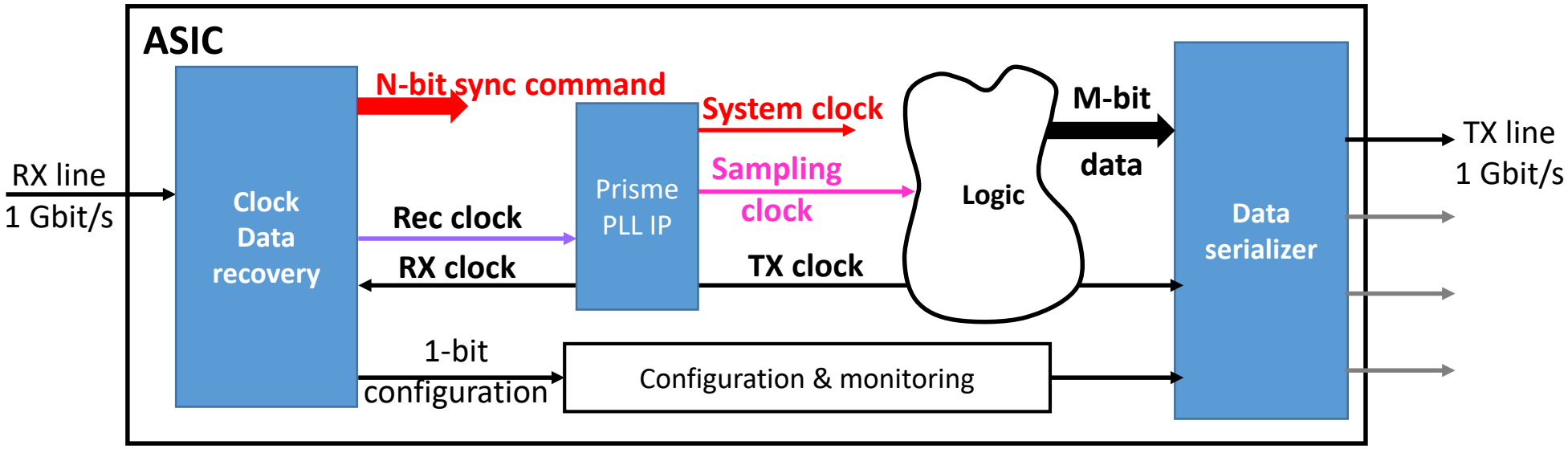
High density 10 Gb/s grade

No RDOs to design, produce, install, debug and maintain

4 times more 12-lane FF pairs
2 times more DAMs

Backup : Reminder of Salsa’s unified backend interface

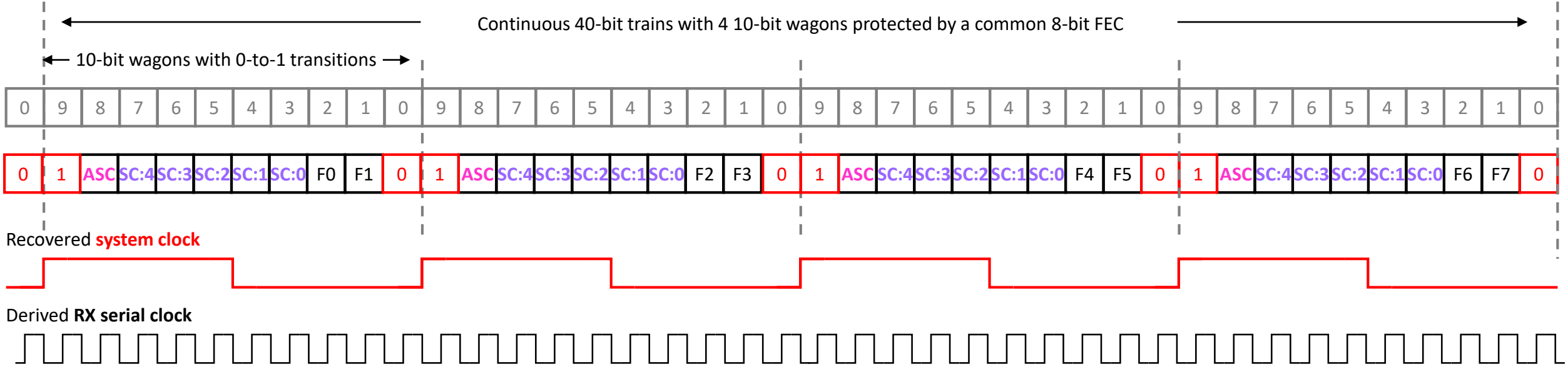
“Unified” interface



- Single encoded RX line for Clock, SynCmd, Trigger, configuration and monitoring
  - → Minimal external interface: a single diff RX line + at least one diff TX line
    - Simplest case: only 4 pins (Rx_p / Rx_n + Tx_p / Tx_n) to communicate with the chip
    - Parallel configuration of ASICs possible : fast startup and recovery time
- Relatively complex initialization phase requiring collaboration from the remote partner (FPGA)
  - → Clock recovery phase followed by
  - → Data reception and transmission phase

Data to Salsa over the serial RX link

F – Parity bits
ASC – asynchronous slow control bit
SC – synchronous command bits



- Periodic 0-to-1 transition for system clock recovery and jitter cleaning in the Prisme PLL IP
- Up to 32 synchronous commands at every system clock cycle
- Asynchronous slow control bit per system clock cycle
  → 100 Mb/s slow control link

- Note : the serialization-deserialization mechanism involves Reed Solomon FEC
  → Capability to recover from up to 13 erroneous bits
    - Precious for robust downstream synchronization

Data from Salsa over the serial TX link

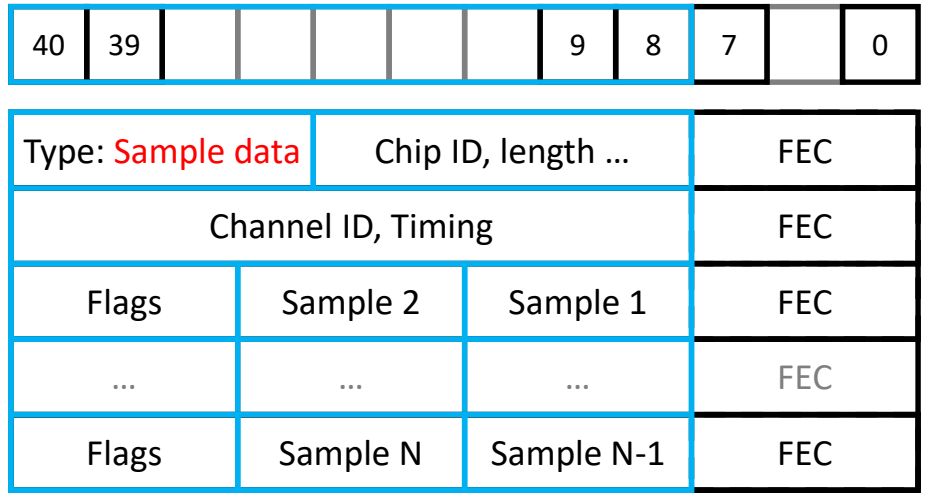
40-bit transmission unit

- Fixed 40-bit length transmission units
  - → 32-bit user payload + 8-bit FEC
    - RS(15,13) Reed Solomon is considered with possibility to correct 4 errors

- Salsa packets transmitted word by word
  - → 20% overhead due to FEC

- Use 40-bit parallel to serial converter
  - → Use single 40-bit RS(15,13) encoder
  - → Interleave four 40-bit encoded words
    - RS(15,13) uses 4-bit symbols
    - Interleave 4-bit by 4-bit
    - Recover from up to 13 consecutive bit errors

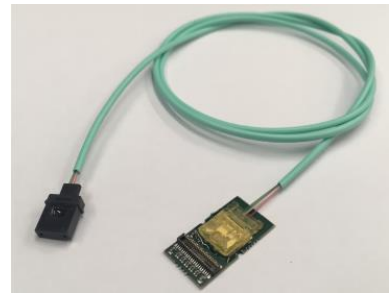
Data packet sketch for illustration only



FEB based on Salsa's unified interface with VTRX+

- FEB
  - → Salsa receives embedded clock / sync / async data over the unified RX interface
    - VTRX+ RX serial link to Salsas via a rad-hard fan-out ASIC
  - → Salsa sends physics, monitoring and slow control data over a single TX line
    - One VTRX+ TX serial link per Salsa
  - → All ASICs are radiation hard

CERN VTRX+



- RDO : common hardware with adaptation based on COTS FireFly transceivers from Samtec
  - Four 4-lane bidirectional FireFly components are needed to serve 4 FEBs
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