Low voltage power for MPGD frontends and VTRX+ pigtail :

Work in progress

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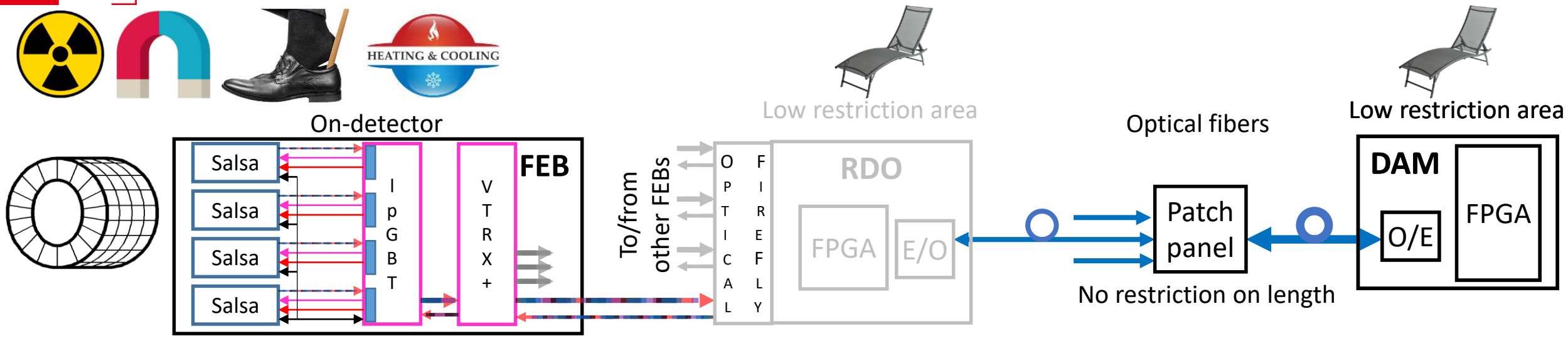
Briefly flashed during eDAQ WG meeting on Oct 24, 2024

FEB based on Salsa's heterogeneous interface with lpGBT



For details see : https://indico.bnl.gov/event/25106/contributions/97861/attachments/57983/99568/241017_IM_lpGbt2Salsa.pdf

- 256-channel FEB
  - → lpGBT provides a bidirectional interface between 4 Salsas and remote backend FPGA (on RDO or DAM)
    - Clock, fast synchronous commands, asynchronous slow control, physics and calibration data, monitoring
  - → VTRX+ is used with only one TX line
  - → All ASICs are radiation hard

- RDO or DAM : common hardware with FireFly transceivers from Samtec
  - → Placed anywhere in user friendly area
    - No particular restrictions on power consumption, cooling infrastructure, radiation, magnetic field

256-channel lpGBT-based FEB for CyMBaL : dimensions

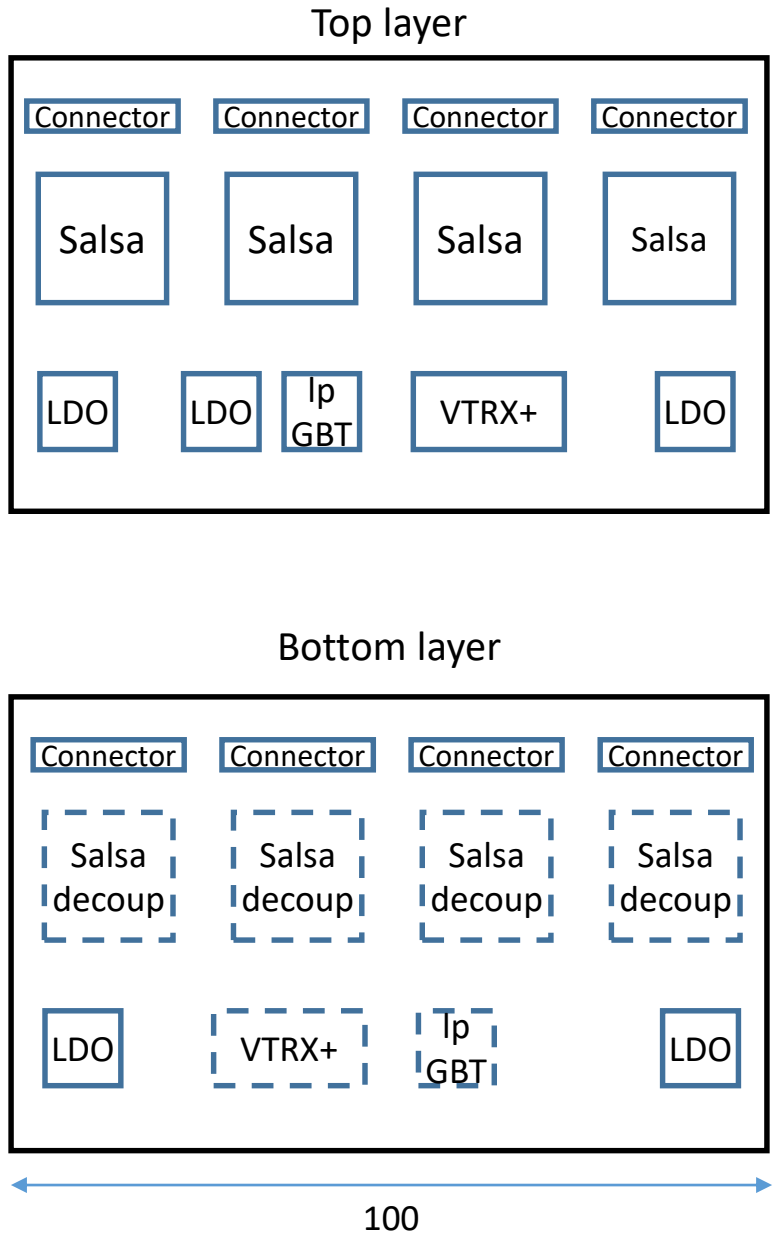
- Assuming 16 x 16 ball 1 mm pitch BGA package for Salsa
- Low profile 40-pin connectors for input signals over micro-coaxial cables
- Active components on both sides of the board

- Length and width give an idea

- Height of the board
  - → Need to accommodate cooling
  - → Need to include mechanical fixture for VTRX+ connector
    - The fragile optical pigtail to be secured within the board

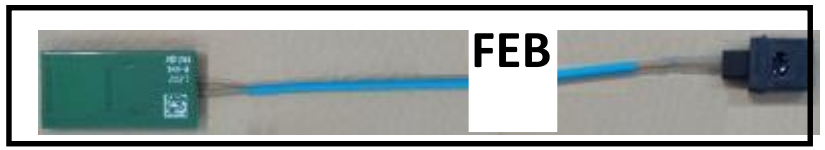
- On-board linear low dropout regulators

- Radiation-hard magnetic field tolerant DC/DC converters
  - → On a companion board
  - → Count on common collaboration efforts
    - Type, surface including air core, height, shielding, cooling



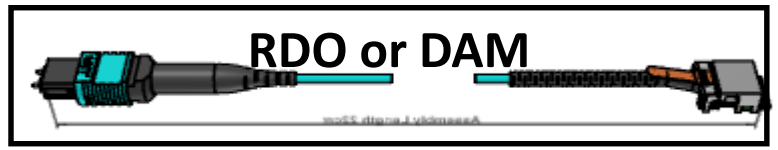
FEB height : ~10 mm

- Protect fragile VTRX+ and its pigtail by containing it within the FEB



Short pigtail / on board

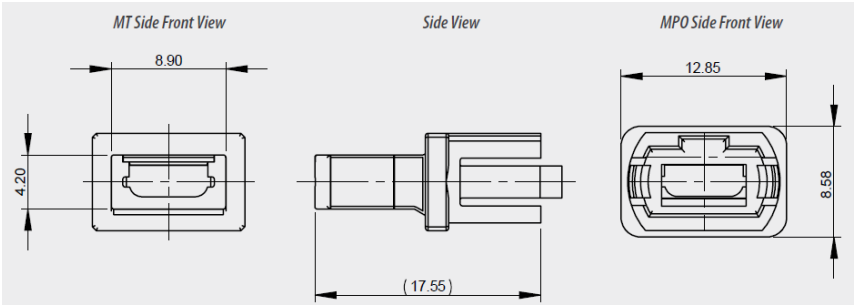
Fibers of adapted length between patch panels



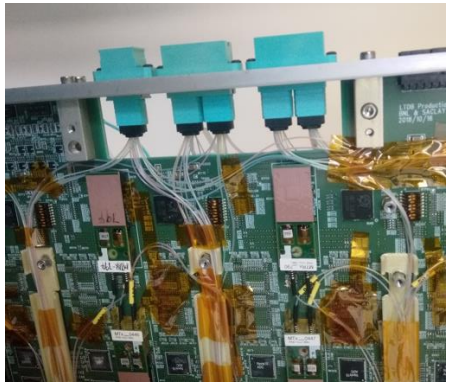
Short pigtail / on board

→ Common practice for commercial FireFly components in industry and VTRX predecessor in HEP community
→ Can limit pigtail length options to very few if not to 1 value : as small as farthest placement from front panel
  - Potential to have a common pool of VTRX+ components for all subsystems
→ Easier maintenance

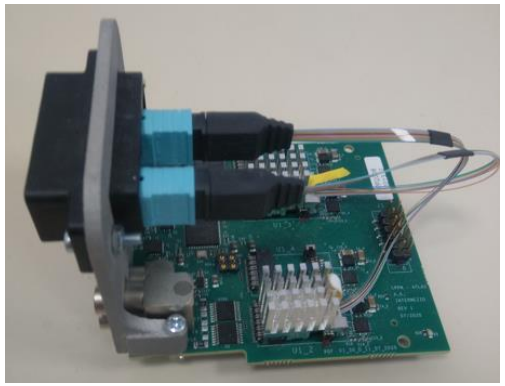
- MT-MPO low-profile adapter from Senko : 7P5-SM-1
  → 8.6 mm height



VTRX example



FireFly example



256-channel lpGBT-based FEB : power

- Raw power budget with minimal margin : ~6.8 W
  - → 27 mW / ch
  - → 1.5V – 6.7 W
  - → 2.8V – 0.2W
- Assume 8.5 W for safety : 25% extra
  - → 33 mW / ch
  - → 1.5 V – 5.6 A
  - → 2.8 V – 90 mA
- Where to place DC/DC converters ?

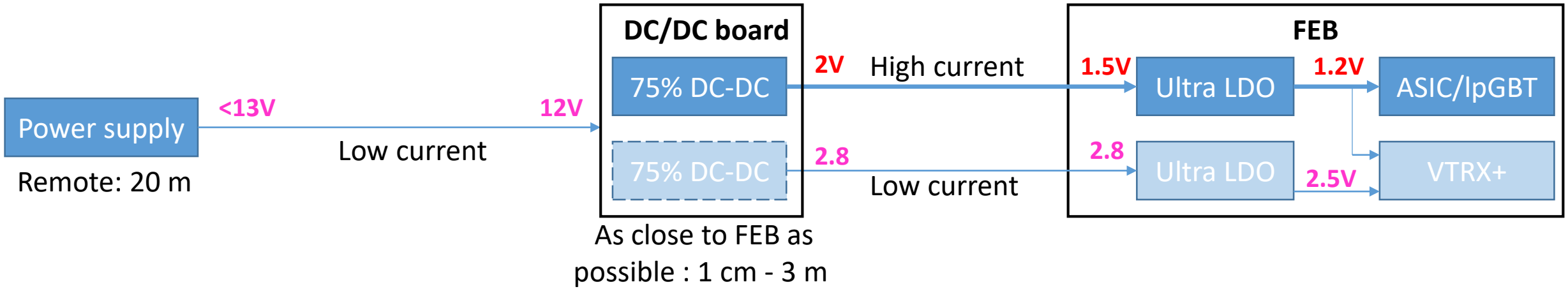
FEB components and their power consumption

Component	Vin V	Current mA	Power mW	Comment
Salsa 1	1.2	1 000	1 200	15 mW/ch
Salsa 2		1 000	1 200	
LDO Salsa 1-2	1.5	2 000	600	Can use 2 LDOs to avoid hotspot
Salsa 3	1.2	1 000	1 200	15 mW/ch
Salsa 4		1 000	1 200	
LDO Salsa 3-4	1.5	2 000	600	Can use 2 LDOs to avoid hotspot
lpGBT	1.2	420	500	Probably 25% overestimated
LDO lpGBT/VTRX+	1.5	440	130	
VTRX+	1.2	20	25	
	2.5	70	175	
LDO VTRX+	2.8	70	20	

FEB power distribution

Reminder : https://indico.bnl.gov/event/22316/contributions/87363/attachments/52727/90159/240215_IM_MpgdPower.pdf

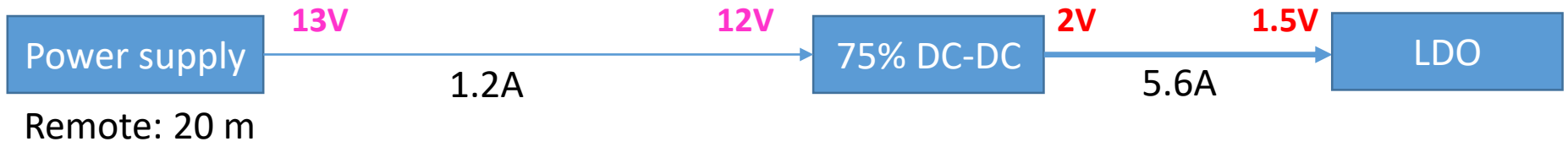
- DC/DC-based LV distribution: to be magnetic field tolerant
  - → Remote power supply distributes 12V with a low voltage drop over ~20 m cables
    - Say less than 1V
  - → Low cross-section power cables
    - The lower the drop the lower the power dissipation in cables but the large is their cross-section



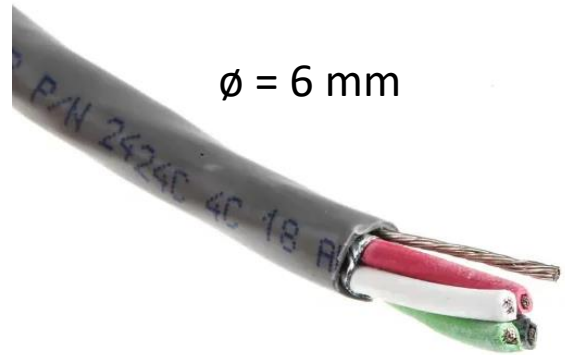
- DC/DC regulators
  - → Might be bulky and a source of EMI
    - Space + extra material for shielding
  - → Distribute high current for 1.2V power
    - Should be close to FEBs
      - Avoid significant power drop and power dissipation in cables
      - Avoid pickup noise and ground-loops

LV cables from power supply to DC/DC regulators

- Assumptions:
  - → Remote LV power supply 20 m away
  - → 1V voltage from between LVPS and DC/DC regulators
    - 13V LVPS output voltage for 12V DC/DC input
  - → 75% DC/DC efficiency
    - 1.2 A over LVPS cables

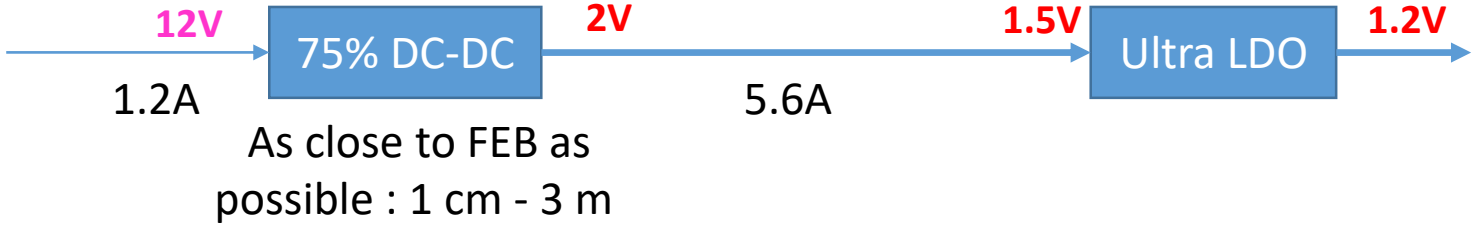


- LVPS power : 15 W / FEB
  - → 60 mW / channel
    - Remember : 15 mW / channel for Salsa !
  - → Power dissipation (loss) over LVPS cables : 1.2 W
- LVPS cables cross-section 0.8 mm^2 or 18 AWG
  - → Cable harness with two power cables and two sense wires
  - → Alpha Wire 2424C : commercial harness including shield and coating : ø = 6 mm
- Reminder : there are 160 CyMBaL FEBs



LV cables from DC/DC regulators to LDO regulators

- Assume 0.5V voltage from between DC/DC and LDO regulators
  - → Reminder : no remote sense regulation
  - → 2V DC/DC output voltage for 1.5V LDO input
  - → 2.8W power dissipation (loss)



Cable cross-section vs DC/DC-LDO distance

DC/DC-LDO Distance	Cross section		Harness + 2.5V cabs
cm	mm^2	AWG	Ø mm
30	0.1	26	4.6
50	0.2	24	5
100	0.4	20	5.4
200	0.8	18	6
300	1.2	16	

Alpha Wire
3464C
6328
2414C
2424C

- Reminder : there are 640 MPGD FEBs with tailored power cable Assemblies
- If possible, having DC/DC board next to FEB is preferred

Summary

- VTRX+ and its pigtail :
  - → Secured in FEB
  - → Connection to external world through MT – MPO adapter on FEBs front panel

- MPGD FEB low voltage power supply
  - → ASICs require on-board ultra LDO regulators
  - → 2 power supply inputs per FEB : high power 1.5V and week 2.8V
    - Respectively for 1.2V and 2.5V on-board voltages
  - → 8.5W per FEB with 25% safety margined
    - 33 mW / channel compared to 15 mV / channel assumed for Salsa

- Magnetic field tolerant compact DC/DC converters are crucial
  - → Placed close to FEBs
    - DC/DC to FEB LV cable diameter may vary from 4.5mm to 6.5mm depending on length
      - Respectively 30 cm to 3 m
      - Accepting 0.5V voltage drop over cables 2.8 W dissipation (loss)
    - Privilege DC/DC converters on FEBs
      - Avoids extra 11 mW / ch due to cables
  - → Placed ~20 m away from LV power supply
    - LV cable assembly of 6 mm in diameter
      - Accepting 1V voltage drop over 20 m cables : 1.2W dissipation (loss)

- Low voltage power supply : 15 W per FEB
  - → 60 mW / channel compared to 15 mV / channel assumed for Salsa

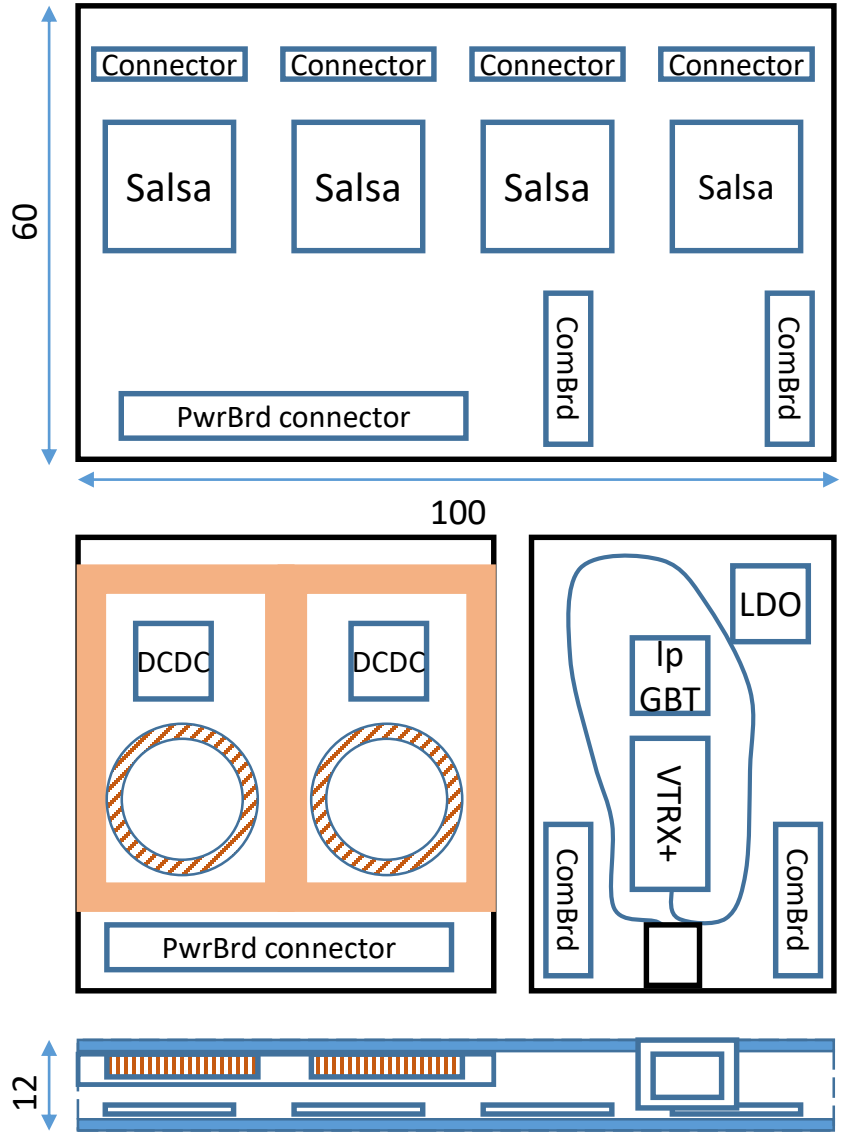
- Question: How others are doing, given that the consumption of ASICs and constriction of FEBs are very similar if not more complex ?

Backup

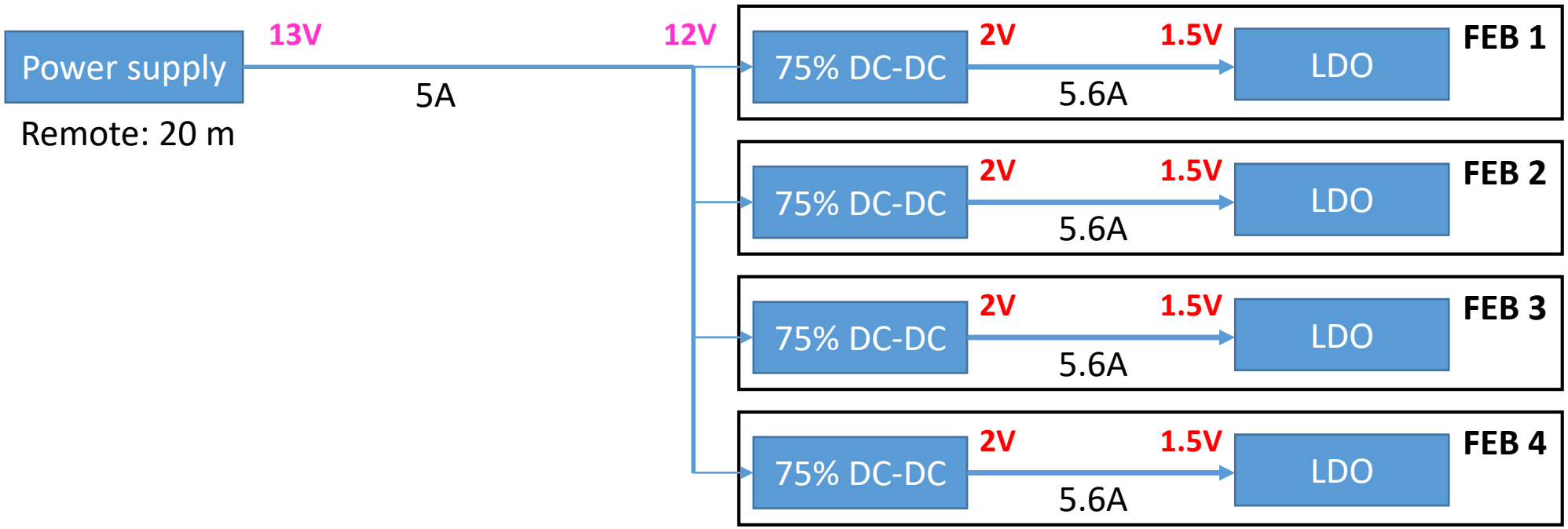
FEB organization ?

- Understand if a daughter card hosting lpGBT and VTRX+ can suite all MPGDs
  - → Placing lpGBT on FEB makes it high-density high-speed grade PCB
    - 10 Gbit/s link speed
    - 0.5 mm pitch 289-ball (17x17) BGA
  - → Pros
    - Production of a large number communication cards common to MPGDs
    - Form-factor adapted low complexity “cheap” FEBs
  - → Cons
    - More types of PCBs to produce and maintain

- Understand if a DC/DC power mezzanine can fit all MPGDs
  - → Pros
    - Avoids LV cables, ground loops, improves regulation
  - → Cons
    - Extra material due to air core and shield



A power harness per CyMBaL detector module : 4 FEBs



- Reasonable assumption for LVPS power cable cross-section : 12 AWG or 3.3 mm^2
  → Cable harness with two power cables and two 0.5 mm^2 sense wires
- Reminder : 32 LV power harnesses for 32 CyMBaL detector modules