POWER REGULATOR OPTIONS & POWER DISTRIBUTION FOR ePIC

Tim Camarda OCT 24 2024

-Testing with CERN bPOL DC-DC Buck converters

-Power board development for powering ASICs (LGAD service hybrids)

-Rad tested linear regulator options

-power distribution

DC|DC performance testing bPOL48V @ bPOL12V (BUCK POINT OF LOAD CONVERTERS)

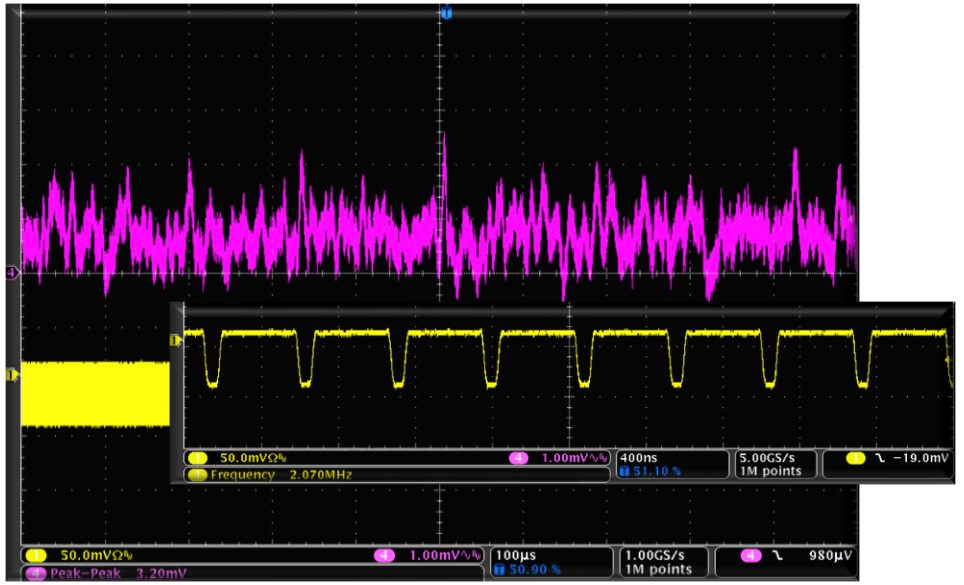
bPOL48V w/ bottom mount heat-sink, 300nH @ 1.5MHz
Inductor dimensions: 10 x 12.0 x 7.5mm (LxWxH)

Vout Noise/ ripple ~3mV (1mV/div) h. 100us

V_{OUT}	1.2V
I_{OUT}	8.2A *MAX 10A
I_{IN}	870mA
V_{IN}	15V
P_{IN}	13.0W
P_{OUT}	9.84W
P_{EFF}	> 75%
Noise 1gHz	< 0.3%
Ripple 25MHz	< 0.3%
On-time	~60ns
Fsw	1.5MHz

EMI (near field) 82.0mV p-p
Measured from bottom of the PCB
50mv/div h.400ns

bPOL12V NO heat-sink, 220nH @ 2.0 MHz
Inductor dimensions: 10.3 x 6.5 x 3.5mm



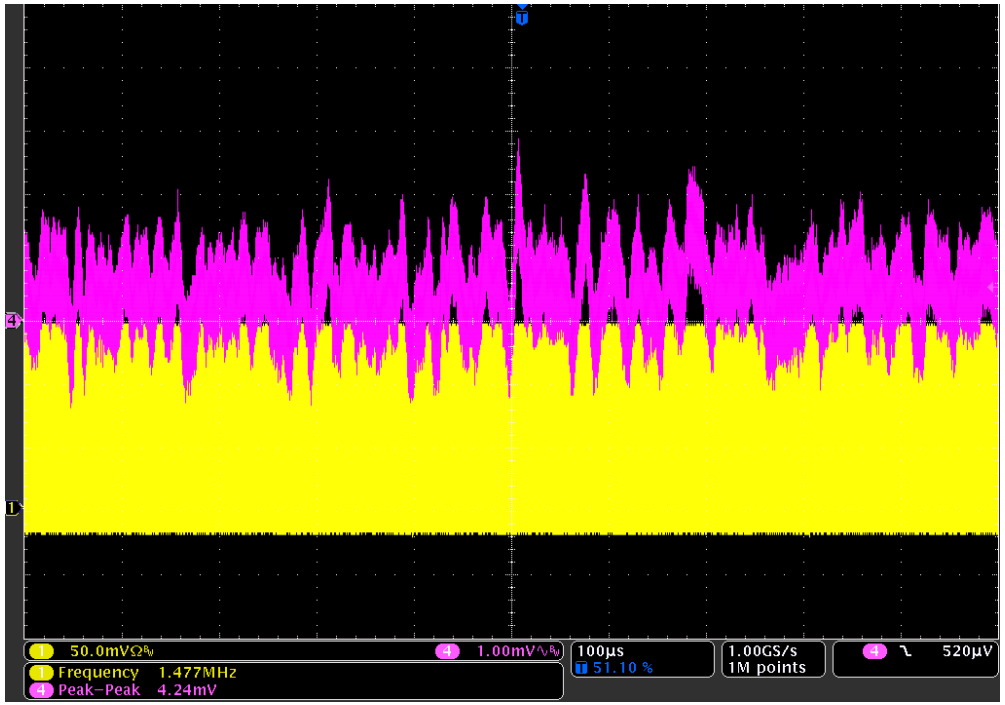
Vout Noise/ ripple ~3.2mV (1mV/div) h. 100us

V_{OUT}	1.2V
I_{OUT}	2.4A *MAX 4A
I_{IN}	410mA
V_{IN}	10V
P_{IN}	4.1W
P_{OUT}	2.9W
P_{EFF}	70.0%
Noise 1gHz	< 0.3%
Ripple 25MHz	< 0.3%
On-time	~70ns
Fsw	2.0 MHz

EMI (near field) 82.0mV p-p
Measured from bottom of the PCB
50mv/div h.400ns

*Manufacturers maximum rating

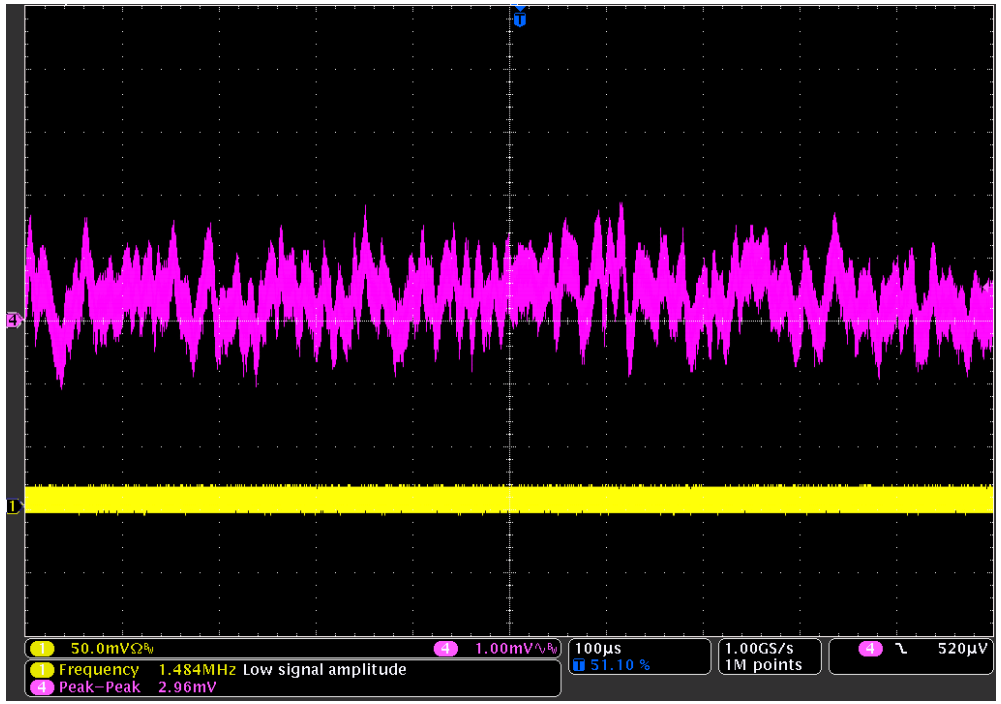
bPOL48V EMI shielding (top PCB)



Condition: No EMI shield on top of PCB

VLT: NOISE @ 1GHz$_{BW}$ (4.24mV$_{p-p}$) < 0.4%

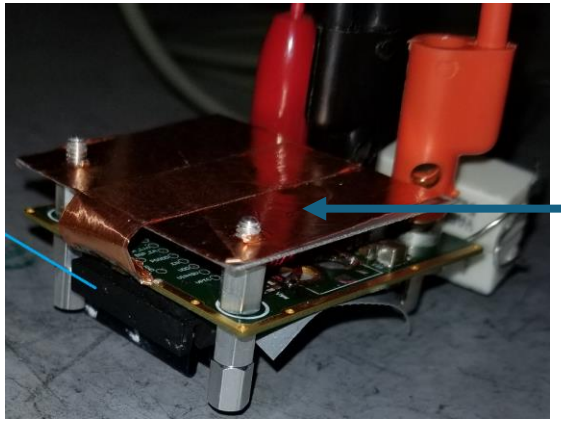
YLW: EMI PROBE$_{NEAR}$ @1GHz$_{BW}$ (150mV$_{p-p}$)



Condition: EMI shield placed on top of PCB

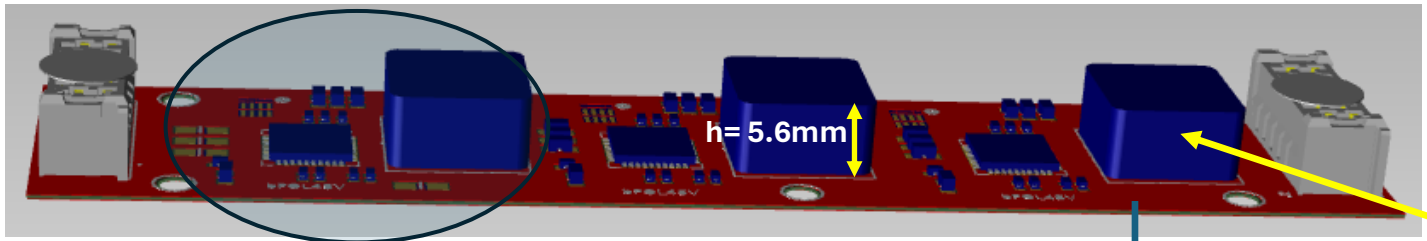
VLT: NOISE @ 1GHz$_{BW}$ (3.0 mV$_{p-p}$)

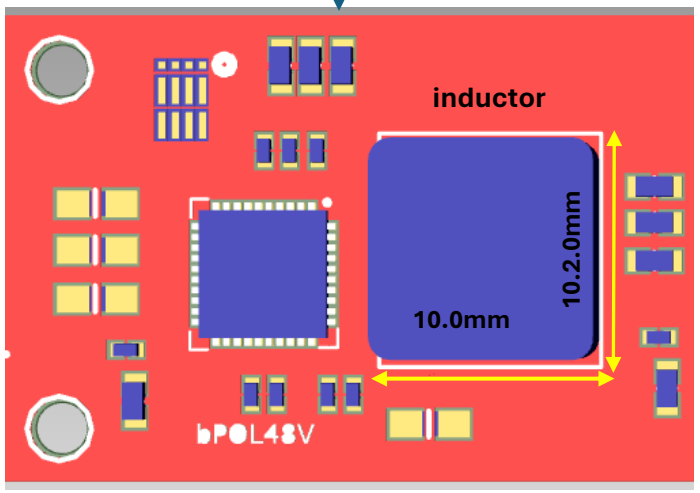
YLW: EMI PROBE$_{NEAR}$ @1GHz$_{BW}$ (25mV$_{p-p}$)



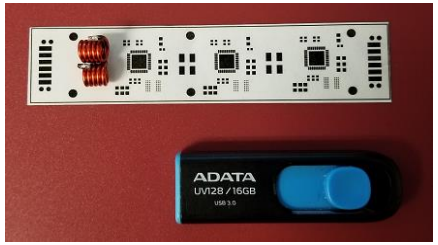
EMI Probe placed on top of shield
Over switching inductor

bPOL48V power regulator board: 25W total (10W/ ch)
1.2V_{OUT} @ 8A



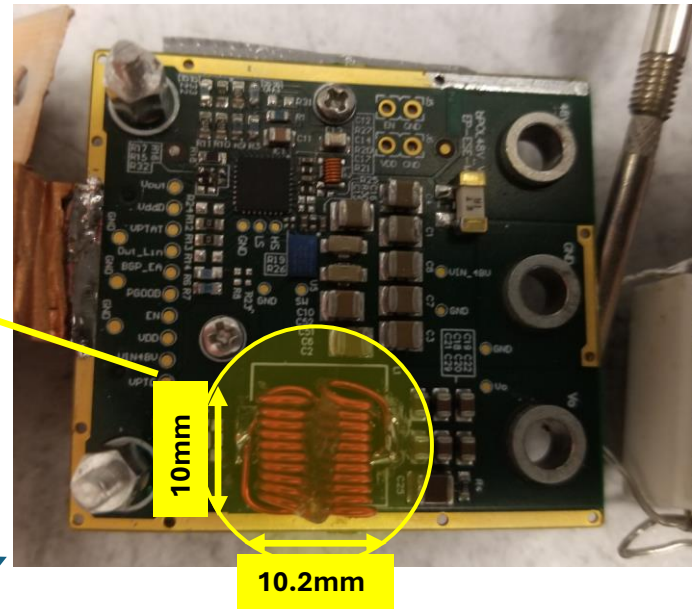


6.82cm^2 circuit footprint size / converter



Proposed fTOF Power Board shown as example
PCB dimensions: 100mm x 22mm x 2.3mm

Cooling:
PCB is requires mounting to cooling plate w/ thermal grease



CERN bPOL48V evaluation board
Modified for 1.2V_{OUT} 8A, ~10W
Heat-sink attached w/ thermal pad at bottom

- Custom switching inductor: 300nH, 8A air-core, solenoid wound in anti-parallel
- DC loss: 66.0mW
- Input LC filter (need for LC output filter will be evaluated)
- Inductor dimensions (mm) lxWxH => 10 x 10.2 x 5.6 => allow ~ *8mm clearance height*
- PCB board stack-up height: 2.4mm (93mil)
- 2.0oz outer copper, 4-6 layers
- Possibility to add shield…but bottom ground plane of RDO may act as shield

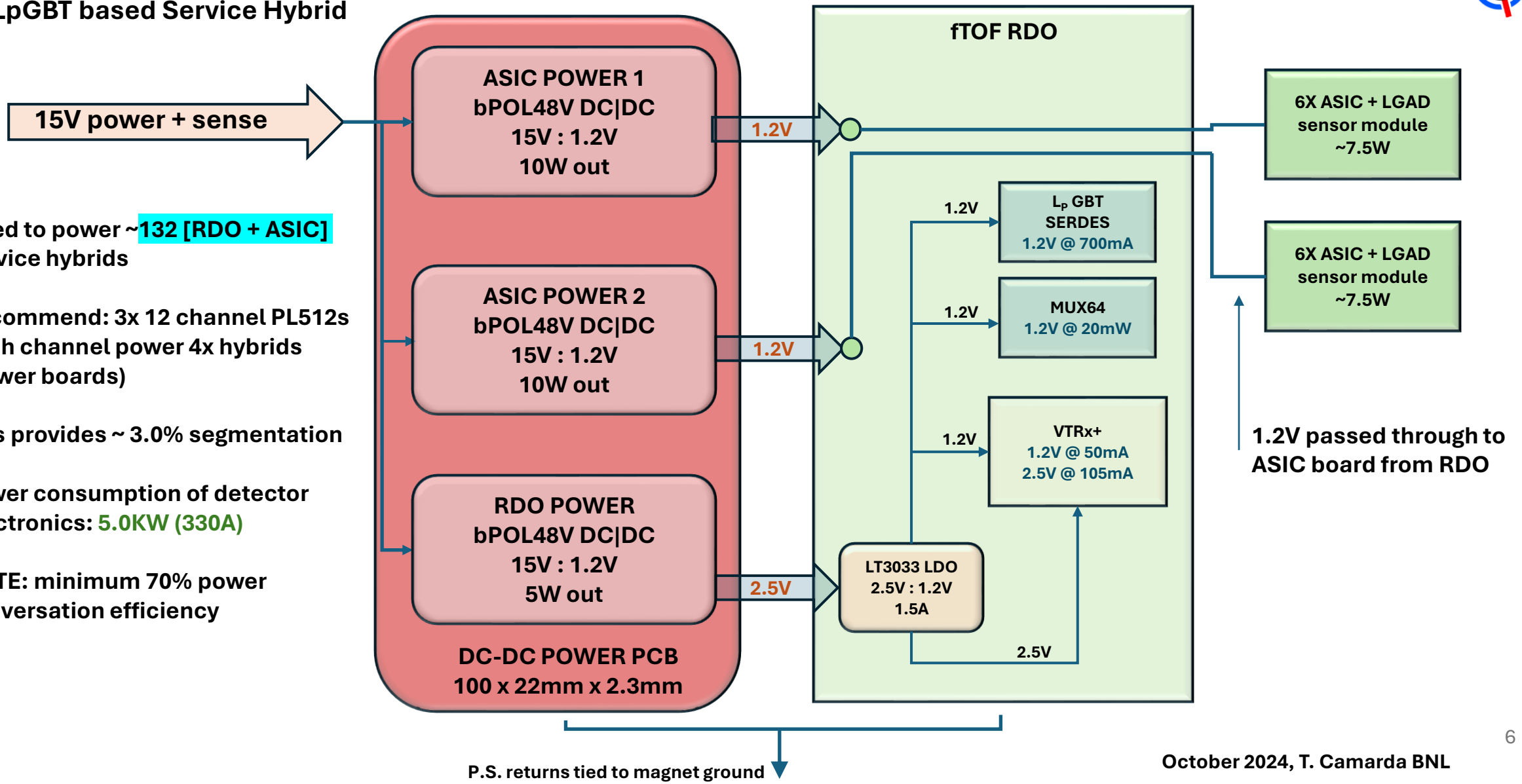
Tim Camarda for ePIC project, OCT 2024

Linear LV regulators: CERN rad hardened Vs COTS rad tested

Device	V_{IN} (V)	V_{OUT} (V)	I_{OUT} (Amps)	V_{DROP}	Pin Functions	Package(mm)	Rad Tested	output noise	Comments
LinPOL12V	5 – 11	0.9 – 3.3	25mA @ 3.3Vo 80mA @ 1.4Vo	Not specified V_{IN} min = 5V	enable	2x2x0.9 DFN	Pending test as per data sheet	Not specified	2x channel Iout / ch
~~LinPOL48V_V2~~	~~0 – 48~~	~~1.2 - 13~~	~~200mA~~		~~enable~~	~~2x2x0.9 DFN~~	~~TID: 50Mrad 4.0E14 n/ cm^2~~	~~Not specified~~	
LT3042	1.8 - 20	0 - 15	200mA	350mV @ 50°C	enable I Lim power good	3x3x0.75 DFN 5x3x1.10 MSE	TID: 70K rad 4.0E12 n/cm^2	0.8uV RMS	MSE is a lead package
LT3045	1.8-2 0	0 – 15	500mA	450mV max	enable I Lim power good	5x4x1.1 MSE	TID: 18k rad 15E11 n/cm^2	0.8uV RMS	
LT3033	1.0 - 10	200mV – 9.7	3A	240mV max	enable I Lim power good	3x4x0.75 QFN	TID: 80k rad 4E12 n/cm^2	60uV RMS	
LT3021	0.9 - 10	200mV – 1.8V	500mA	300mV max	enable	5x5x0.75 DFN 6x5x1.7 SOIC	TID: 45k rads 3.1E12 n/cm^2	300mV RMS	

- Only single option available for rad hardened device
- COTS devices listed were tested by CERN controls & Electronics group. Neutron equivalent damage satisfies ePIC requirements in 3 of the devices
- BNL EE group can further evaluate TID for 100K rad at our cobalt 60 facility

fTOF POWER BOARD POWER DISTRIBUTION BLOCK
LpGBT based Service Hybrid



Need to power ~132 [RDO + ASIC] service hybrids

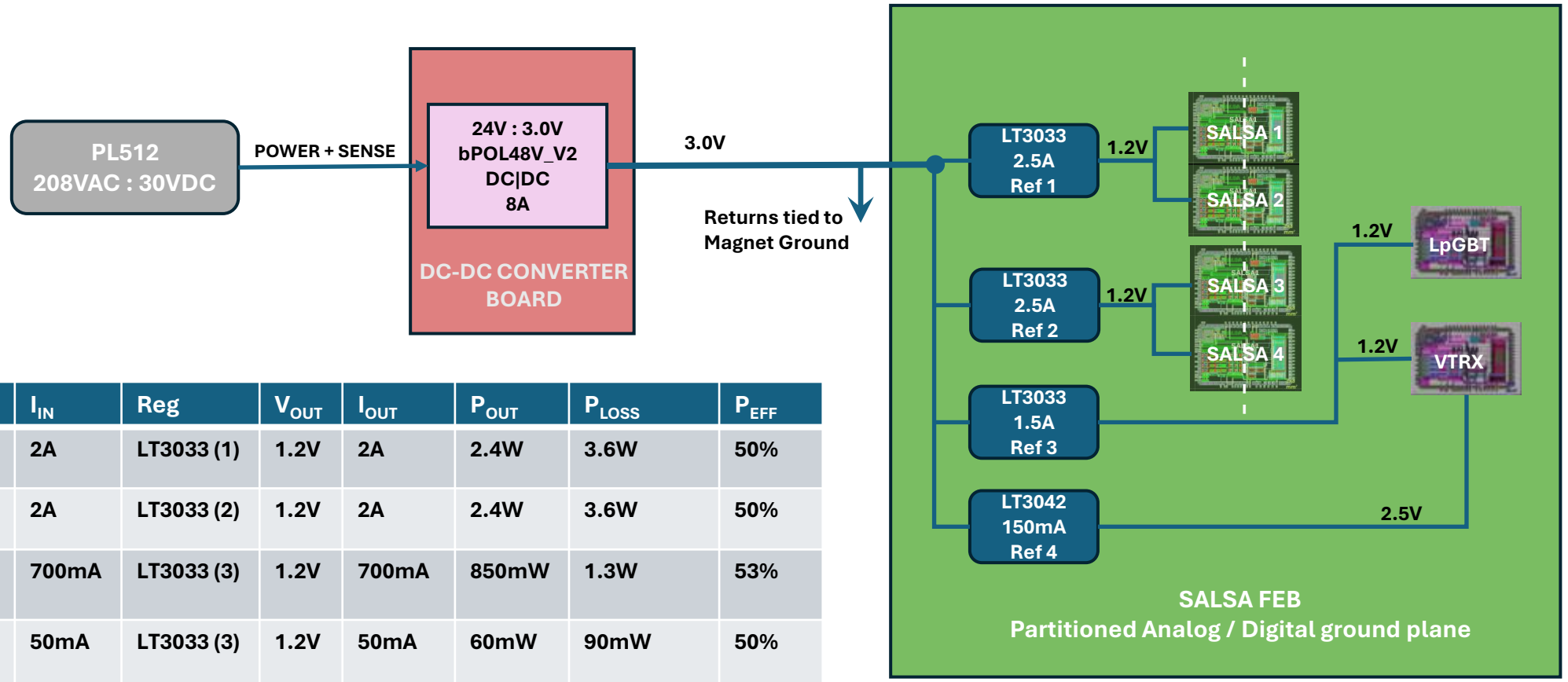
Recommend: 3x 12 channel PL512s
Each channel power 4x hybrids (power boards)

This provides ~ 3.0% segmentation

Power consumption of detector electronics: 5.0KW (330A)

NOTE: minimum 70% power conversation efficiency

Powering MPGD ASIC FEB (power budget)
Hybrid design w/ bulk input conversion & linear regulation on FEB



Circuit	V_{IN}	I_{IN}	Reg	V_{OUT}	I_{OUT}	P_{OUT}	P_{LOSS}	P_{EFF}
SALSA ASIC	3.0	2A	LT3033 (1)	1.2V	2A	2.4W	3.6W	50%
SALSA ASIC	3.0	2A	LT3033 (2)	1.2V	2A	2.4W	3.6W	50%
LpGBT	3.0	700mA	LT3033 (3)	1.2V	700mA	850mW	1.3W	53%
VTRX	3.0	50mA	LT3033 (3)	1.2V	50mA	60mW	90mW	50%
VTRX	3.0	105mA	LT3042 (4)	2.5V	105mA	275mW	60mW	78%
Input Reg	24V	870mA	bPOL48V	3.0V	4.86A	14.6W	4.38W	70%

Regulator circuit Voltage & Current Output
Current indicated is maximum load reg circuit is designed for.
See table for power budget

Need to re-tally number of bPOL48V and bPOL12V required for ePIC

System	Part No.	Quantity	Comments	No. of boards powered
Forward TOF	bPOL48V_V2	700	ASIC board + RDO power	212 ASIC modules + 212 RDOs
	bPOL12_V6	700	FPGA based ASIC Read Out Board	
Barrel TOF	bPOL48V_V2	900	ASIC board + RDO power	288 ASIC modules + 288 RDOs
	bPOL12_V6	900	FPGA based ASIC Read Out Board	
MPDG Disk	bPOL48_V2	100	Front End Board + RDO power	63 Front End Boards + 63 RDOs
	bPOL12_V6	210	Power for SALSA ASIC boards	
Inner Barrel MPDG	bPOL48_V2	50	Front End Board + RDO power	40 Front End Boards + 40 RDOs
	bPOL12_V6	150	Power for SALSA ASIC boards	
Outer Barrel	bPOL48_V2	170	Front End Board + RDO power	144 Front End Boards + 144 RDOs
	bPOL12_V6	500	Power for SALSA ASIC boards	
pfRICH	bPOL48_V2	100	Sensor Board	68 sensor boards + 17 RDOs
	bPOL12_V6	60	RDO	17 RDOs
	bPOL48_V2	2,020		
	bPOL12_V6	2,520		