RDO Concept

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Goals

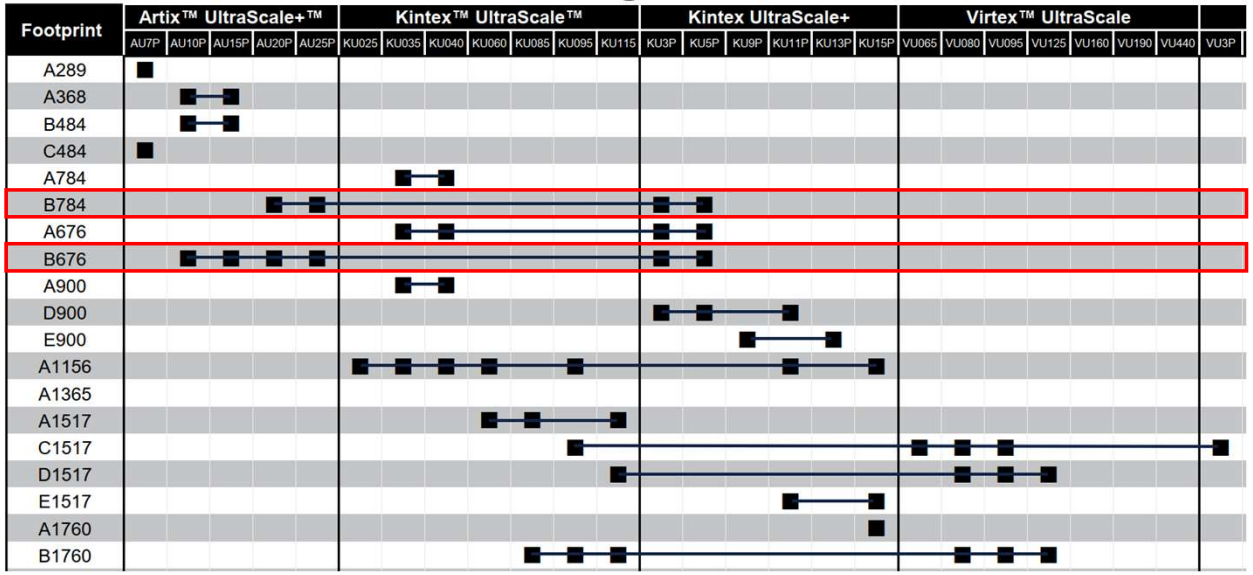
- Design of a reusable FPGA module suitable for a wide range of detectors
  - Not only calorimeters, but make a generic RDO
  - Suitable for data acquisition and aggregation
- Flexible and adaptable
- Scalable
- Available at a good price (for a long time)

FPGA

Baseline is to use Artix (Kintex) UltraScale+ from AMD (Xilinx)

- Relatively well-priced FPGAs to consider
- Long-term availability is important
- The scalability is also very important

UltraScale Architecture Migration Table



The pin count point of view two footprint can give a big range of flexibility:

- B676 1mm pitch
- B784 0.8mm pitch

(The Spartan series is not pin compatible and its complexity is very low.)

https://www.amd.com/en/products/adaptive-socs-and-fpgas/fpga/artix-ultrascale-plus.html
https://www.amd.com/en/products/adaptive-socs-and-fpgas/fpga/kintex-ultrascale-plus.html

FPGA complexity - Comparison criterias

B676 Package, 1mm pitch

#	Part Number	Unit Price $	Logic Cells	DSP	36K	HP	HD	GTH GTY	PCIe Gen/Lane
11	XCAU10P-1FFVB676E	185	96 250	400	100	156	72	12	4/4, 3/8
13	XCAU10P-2FFVB676E	259	96 250	400	100	156	72	12	4/4, 3/8
15	XCAU15P-1FFVB676E	231	170 100	576	144	156	72	12	4/4, 3/8
17	XCAU15P-2FFVB676E	324	170 100	576	144	156	72	12	4/4, 3/8
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21	XCAU20P-2FFVB676E	467	238 437	900	200	156	72	12	4/8
23	XCAU25P-1FFVB676E	398	308 437	1200	300	208	72	12	4/8
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27	XCKU3P-1FFVB676E	1 405	355 950	1368	360	208	72	16	4/8
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31	XCKU5P-1FFVB676E	2 055	474 600	1824	480	208	72	16	4/8
33	XCKU5P-2FFVB676E	2 731	474 600	1824	480	208	72	16	4/8

B784 Package, 0.8mm pitch

#	Part Number	Unit Price $	Logic Cells	DSP	36K	HP	HD	GTY	PCIe Gen/Lane
19	XCAU20P-1SFVB784E	305	238 437	900	200	156	72	12	4/8
21	XCAU20P-2SFVB784E	428	238 437	900	200	156	72	12	4/8
23	XCAU25P-1SFVB784E	388	308 437	1200	300	208	96	12	4/8
25	XCAU25P-2SFVB784E	543	308 437	1200	300	208	96	12	4/8
27	XCKU3P-1SFVB784E	1 466	355 950	1368	360	208	96	16	4/8
29	XCKU3P-2SFVB784E	2 054	355 950	1368	360	208	96	16	4/8
31	XCKU5P-1SFVB784E	1 976	474 600	1824	480	208	96	16	4/8
33	XCKU5P-2SFVB784E	2 768	474 600	1824	480	208	96	16	4/8

- Of course, the number of Logic Cells
- DSP capabilities
- Buffering, Clocking
- Pin Count and Type
  - High Performance IO-s
  - High Density IO-s
- Speed Grade
- GTH/GTY
  - GTH: 16.3 Gbps Max.
  - GTY: 32.75 Gbps Max.

- AMD UltraScale+ GTH (16.3Gb/s): Low power & high performance for the toughest backplanes
- AMD UltraScale+ GTY (32.75Gb/s): Maximum NRZ performance for the fastest optical and backplane applications; 33G transceivers for chip-to-chip, chip-to-optics, and 28G backplanes
- https://www.amd.com/en/products/adaptive-socs-and-fpgas/technologies/high-speed-serial.html

V_{CCO}[4, 5]	Supply voltage for HD I/O banks	1.140	3.400	V
	Supply voltage for HP I/O banks and configuration bank 0	0.950	1.900	V

Table 23: **LVDS Component Mode Performance**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages						Units
		0.85V				0.72V		
		-2		-1		-1		
		Min	Max	Min	Max	Min	Max	
LVDS TX DDR (OSERDES 4:1, 8:1)	HP	0	1250	0	1250	0	1250	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	HP	0	625	0	625	0	625	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8)[1]	HP	0	1250	0	1250	0	1250	Mb/s
LVDS RX DDR	HD	0	250	0	250	0	250	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4)[1]	HP	0	625	0	625	0	625	Mb/s
LVDS RX SDR	HD	0	125	0	125	0	125	Mb/s

Table 24: **LVDS Native Mode Performance**

Description[1, 2]	DATA_WIDTH	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages						Units
			0.85V				0.72V		
			-2[3]		-1[3]		-1[3]		
			Min	Max	Min	Max	Min	Max	
LVDS TX DDR (TX_BITSLICE)	4	HP	375	1600	375	1600	375	1260	Mb/s
	8		375	1600	375	1600	375	1600	Mb/s
LVDS TX SDR (TX_BITSLICE)	4	HP	187.5	800	187.5	800	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	800	Mb/s
LVDS RX DDR (RX_BITSLICE)[4]	4	HP	375	1600[5]	375	1600[5]	375	1260[5]	Mb/s
	8		375	1600[5]	375	1600[5]	375	1600[5]	Mb/s
LVDS RX SDR (RX_BITSLICE)[4]	4	HP	187.5	800	187.5	800	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	800	Mb/s

Clock Buffers and Networks

Table 36: **Clock Buffers Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
Global Clock Switching Characteristics (Including BUFGCTRL)					
F_{MAX}	Maximum frequency of a global clock tree (BUFG)	775	667	667	MHz
Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)					
F_{MAX}	Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV)	775	667	667	MHz
Global Clock Buffer with Clock Enable (BUFGCE)					
F_{MAX}	Maximum frequency of a global clock buffer with clock enable (BUFGCE)	775	667	667	MHz
Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)					
F_{MAX}	Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF)	775	667	667	MHz
GTH or GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)					
F_{MAX}	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability	512	512	512	MHz

FPGA complexity - Comparison criterias - Economic aspects

B676 Package, 1mm pitch

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B784 Package, 0.8mm pitch

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- Price

- Long-term availability
  - Tried. Trusted. Long Lasting. With typical lifespans extending well past 15 years, you can depend on AMD devices being around for the life of your design
  - AMD 7 Series FPGAs and adaptive SoCs extended through 2040*
  - AMD UltraScale+™ FPGAs and adaptive SoCs extended through 2045*

https://www.amd.com/en/products/adaptive-socs-and-fpgas/fpga/artix-ultrascale-plus.html

FPGA selection - Conclusion

B676 Package, 1mm pitch

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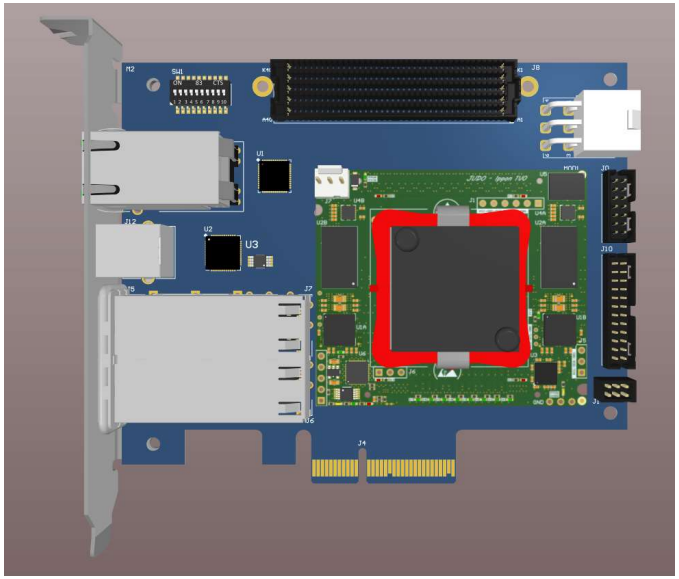
- The Artix US+ seems to be a really good option
- The bigger package does not give any advantage in terms of pin count, but reduces scalability
- 100+ HP and HD pins enable interfacing many (even different) types and many chips
- With the available GTx pins (12, maybe 16 in Kintex), aggregator functions are also available and can be implemented
- Consequently, the B676 footprint was proposed due to the wider chip choice and the mentioned facts before

Basic idea – Mother and Daughter boards

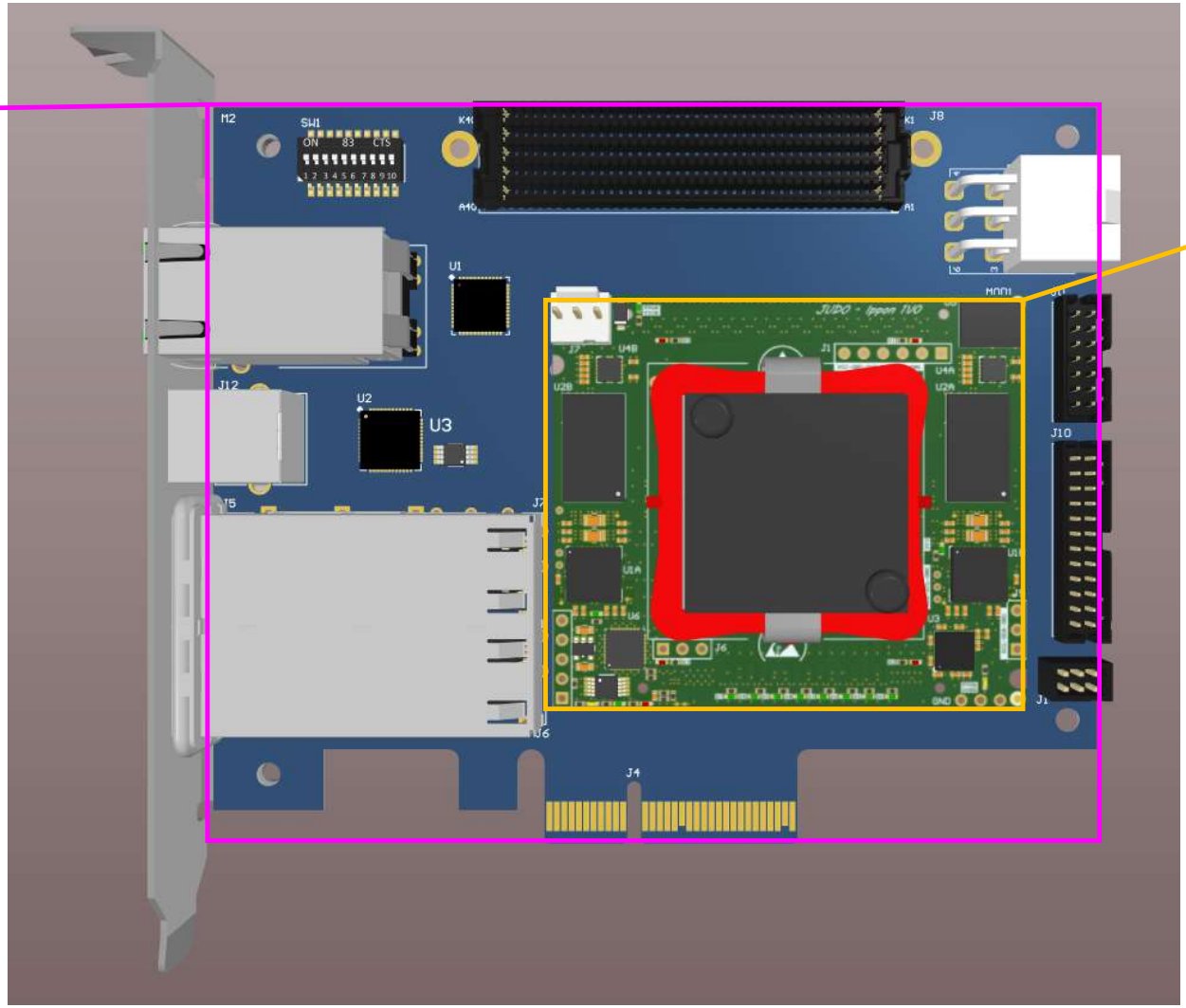
- Daughter Board (DB):
  - FPGA (Artix UltraScale+ or Kintex UltraScale+ FPGA)
  - 676 pin package
  - 12 Maybe 16 GTx
  - 50+ Differential pair, HP
  - 20+ Single ended wire, HD
  - OnBoard Memory DDR4 (optional, 0, 1 or 2)
  - System controller on the board
  - Low complexity clock signal distribution
  - DCDC-s with 12V input

- Mother Board (MB):
  - All connections to FEB
  - All connections to DAM (SFP+ or FMC)
  - Power distribution
  - Low or High complexity clock signal distribution
  - Compatible with all daughter cards
  - Can be highly application dependent
  - This board is ‚cheap', can be different for each detector
    - PCIe compatibility for testbeams
    - 10G, SFP+
    - 1 or 2 FMC connector



Basic idea – Design Example

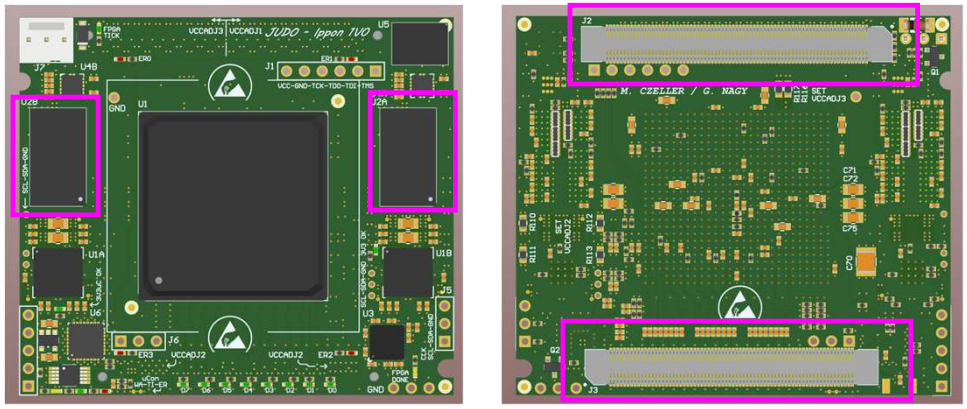
Mother Board (MB)



Daughter Board (DB)

Proposed versions for Daughter Board (DB)

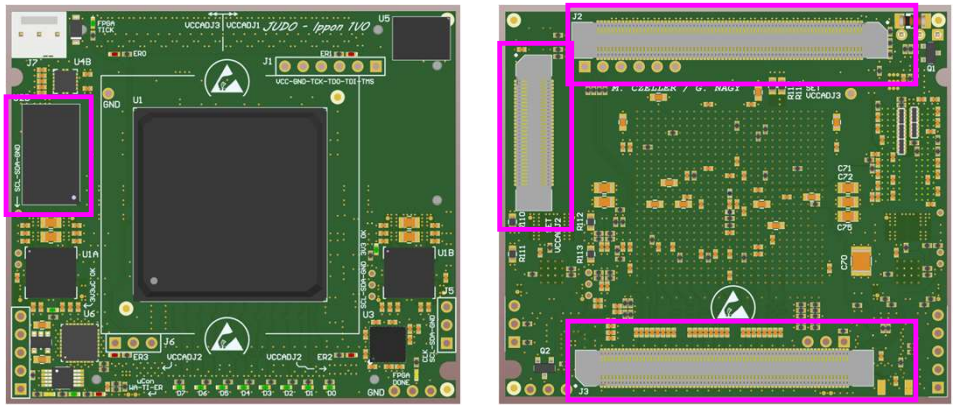
Version A – 62x54mm



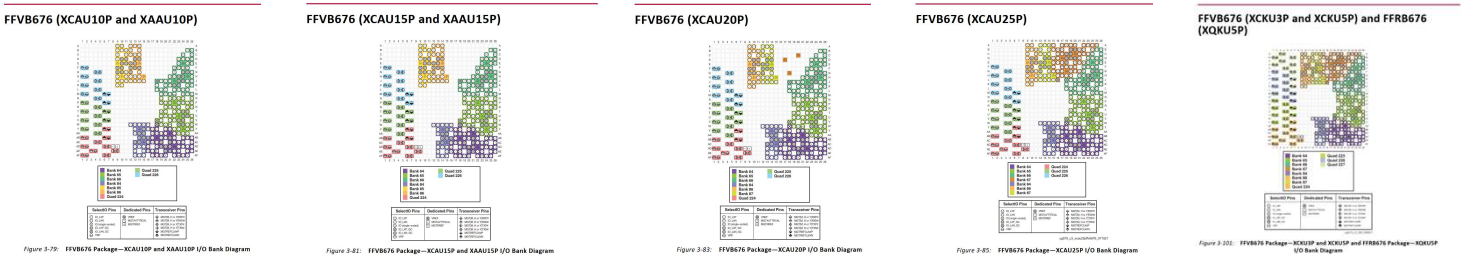
- 2 connector version, contains 2x independent DDR4 Memory chip, MT40A512M16TB, (DDR4-3200 or DDR4-2666)

- 46 HP differential pair – 46 x Max. 1250Mbps (1600Mbps*)
- 12 MGT – 12x Max. 16.3 Gbps
- Ideal for aggregator tasks
- Proposed FPGA: XCAU25P (XCKU3P or XCKU5P)

Version B – 62x54mm

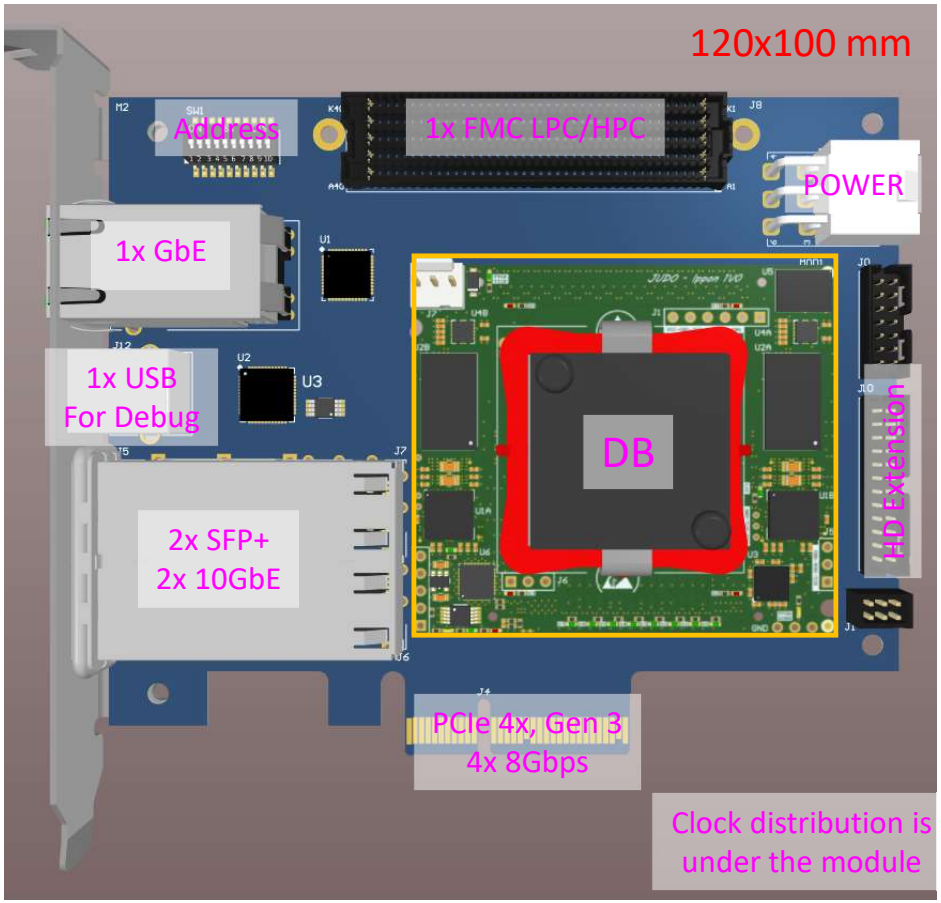


- 3 connector version, contains 1x DDR4 Memory chip, MT40A512M16TB, (DDR4-3200 or DDR4-2666) in case of XCAU25P (or all Kintex version) All other Artix version has no memory chip populated
- 46+24 HP differential pair – (46+24) x Max. 1250Mbps(1600Mbps*)
- 12 MGT – 12x Max. 16.3 Gbps
- Ideal for interfacing for chips
- Proposed FPGA: XCAU25P (XCKU3P or XCKU5P)



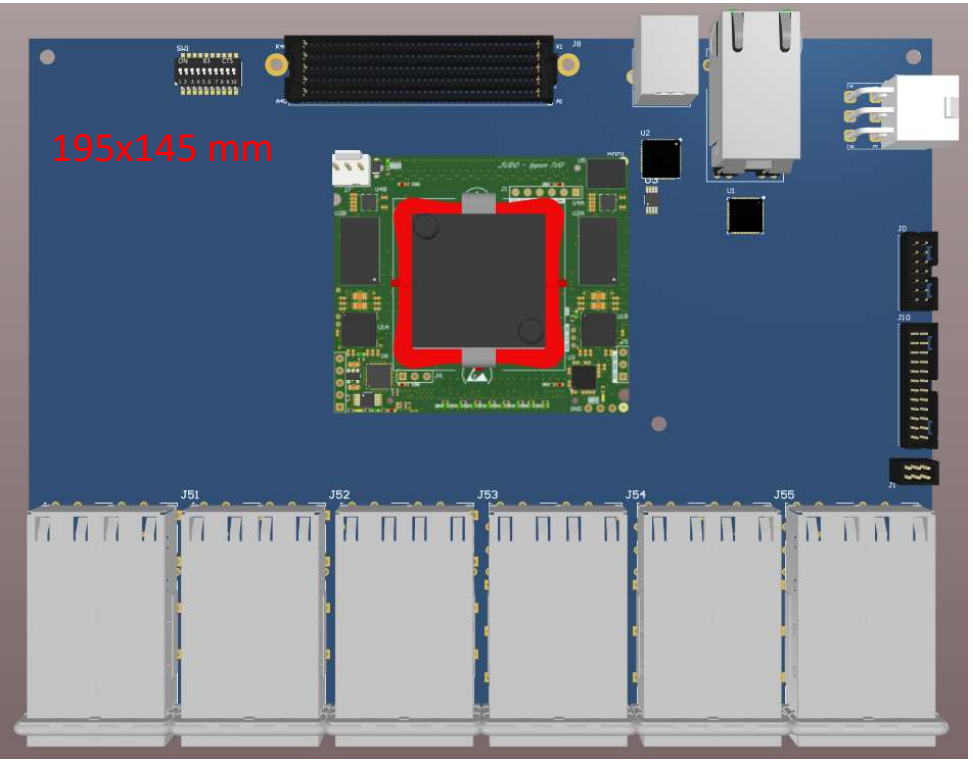
Proposed versions for Mother Board (MB)

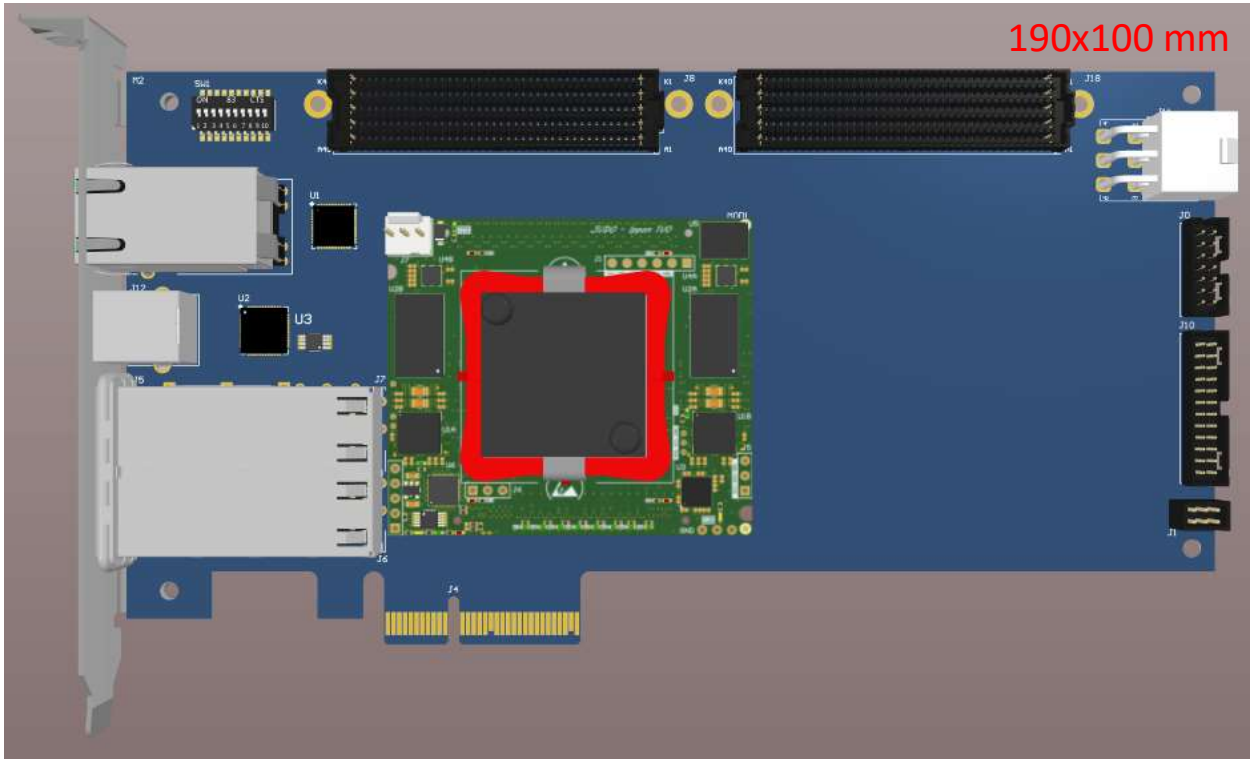
- This board can receive all the above mentiond DB
- You can develop and test mostly all basic IP-s on this board which are necesarry
- It is a ‚cheap' board and it can be strongly application dependenet



Another two exmample for Mother Board (MB)

Aggregator or 2x FMC



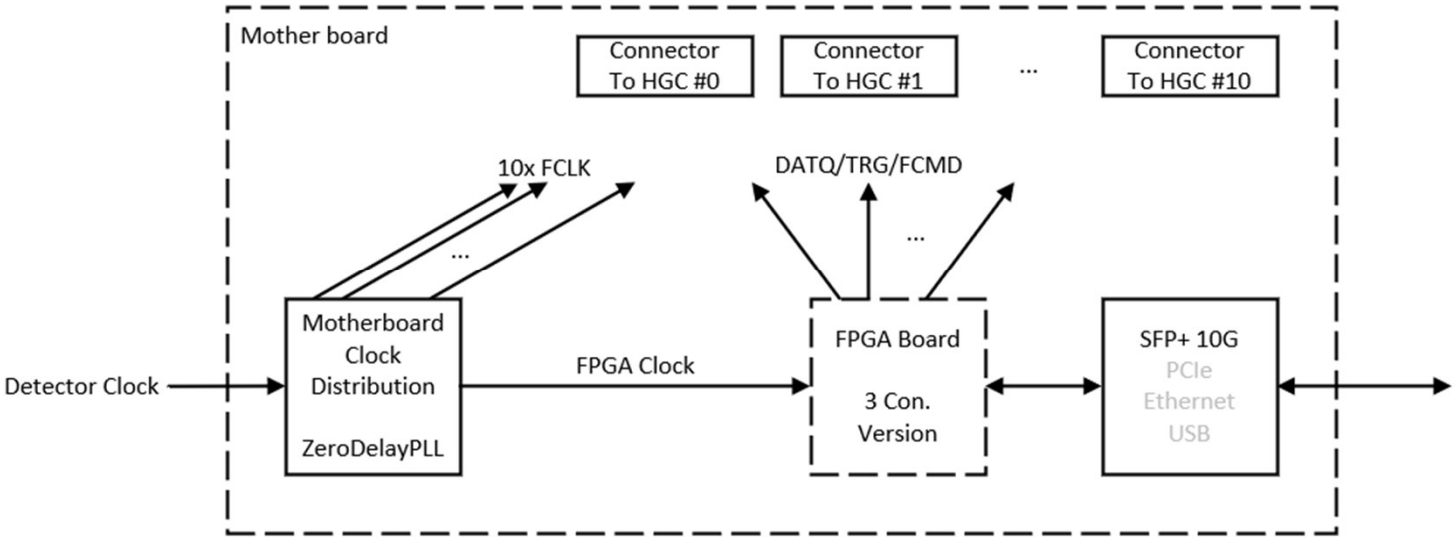


Specific implementation with H2GCROC/CALOROC

- Possibilities based on the available pins:

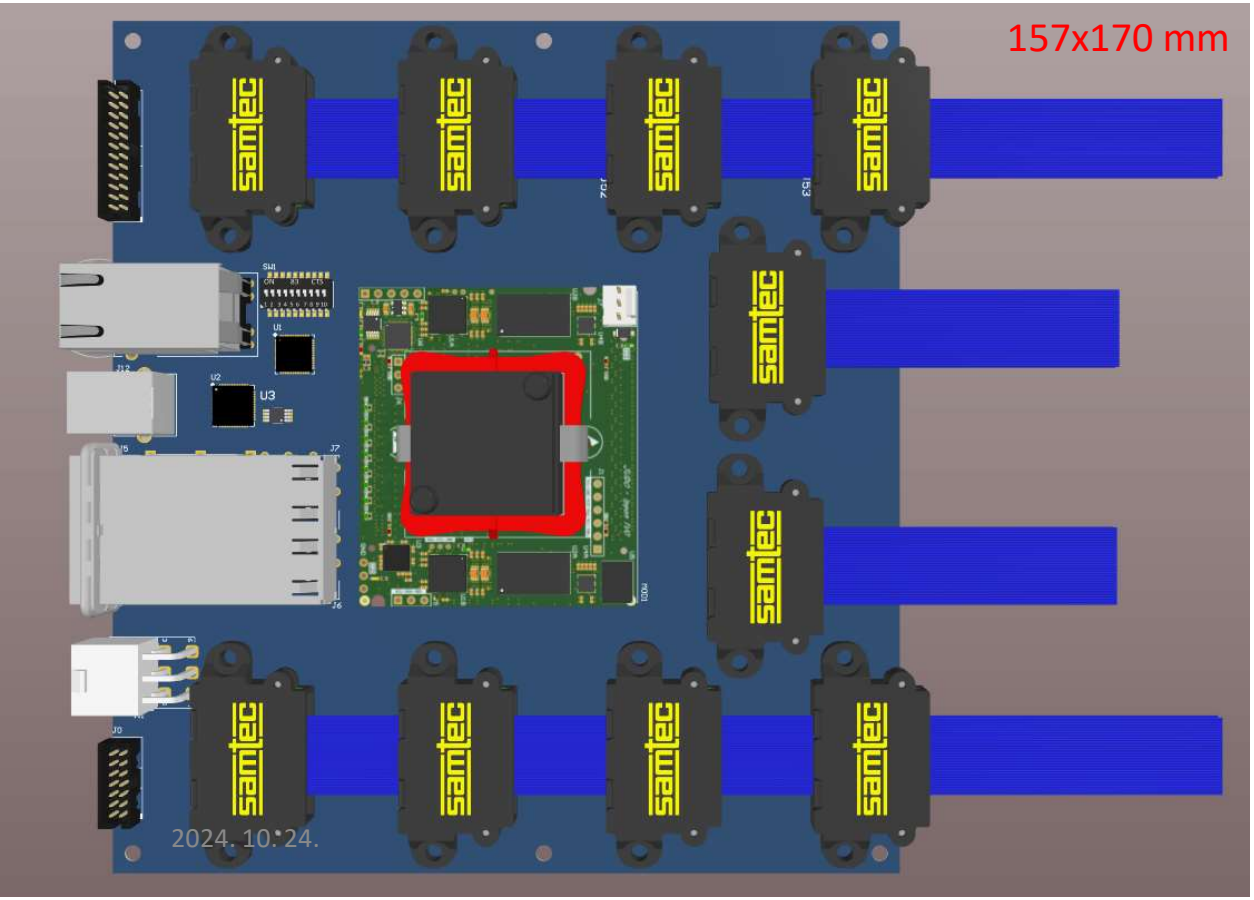
	Data 1.28Gbps	Trigger 1.28Gbps	FCLK 320MHz	FCMD 320MHz	I2C Reset(s)
H2GCROC	2	4	1	1	4
CALOROC (initial)	4	0	1*	1*	4
CALOROC (proposed)	4	0	1	1	4
* 200MHz					

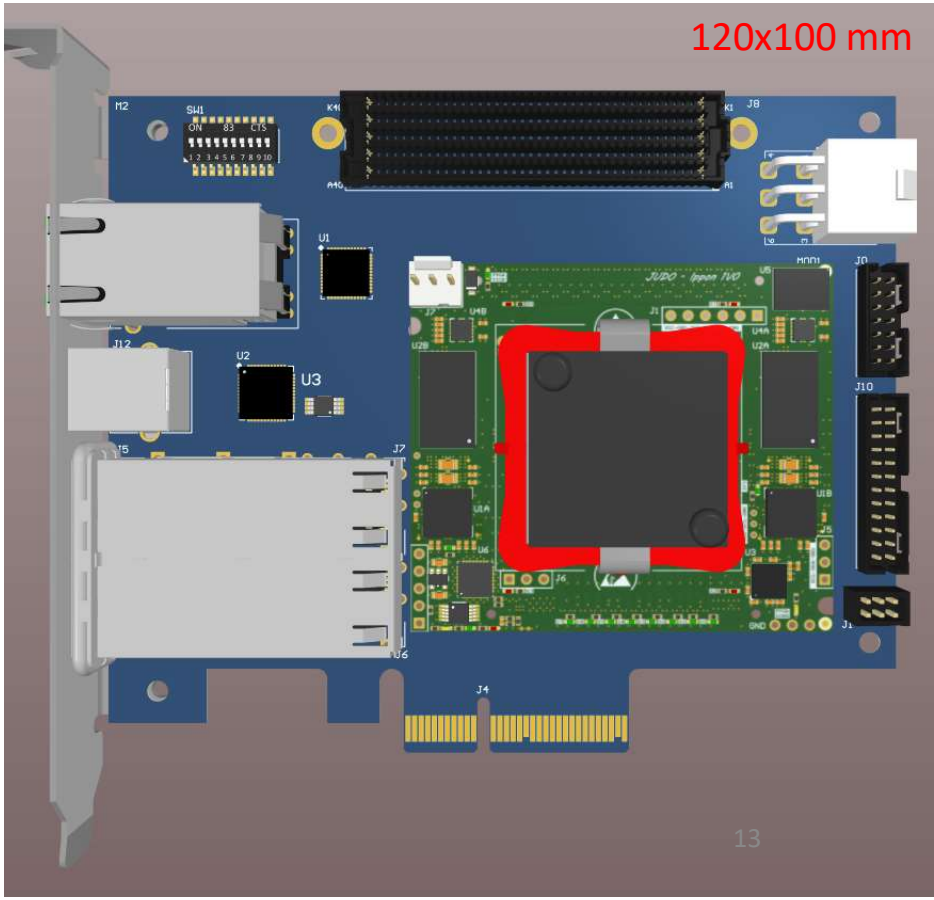
Configuration	2 Con. Version	3 Con. Version
-	46 HP Diff.	70 HP Diff.
H2GCROC (Full)	5	8
H2GCROC (Full), Ext CLK	6	10
H2GCROC (Full), TC9	7	11
H2GCROC (Full), Ext CLK, TC9	9	14



Specific implementation with H2GCROC/CALOROC cont.

- These needs can be met with the Proposed Motherboard + Version A or B in case of FMC connector
- Or with a special motherboard with HQDP cables from Samtec (10m)





Fill up form for each detector types

This is an attempt to collect all the needs from different detectors to optimize the motherboard for broader usage

	Detector name (CALOROC)	RDO I/O pins used
FEB connections	4x1.28 Gbps (LVDS/CML)	
	320 MHz clock (LVDS/CML)	
	Fast Command (320 MHz)	
	Soft Reset	
	Hard Reset	
FEB/RDO ratio	8	
DAM connection	1x10 Gbps fiber	1xMGT
...		
...		
...		


Thanks!