EICROC and lpGBT

- Discussion with the EICROC developers 10/8/2024
  - Christophe, Frederic, TL, also Norbert
- It should be no problem (even easier!) to move to lpGBT-required readout and clocking scheme
  - current clock: 200 MHz ⇒ 320 MHz
  - “Fast command” becomes ⇒ 320 Mbs
    - 8bit command is issued at the 40 MHz frequency
    - we especially need the “clear counters” command
  - data from EICROC becomes ⇒ 160 Mbs or 320 Mbs and up to 1280 … (programmable)
- they will implement this using the existing cores from the current lpGBT-compatible & vetted HGCROC (low risk)
- however, they need a confirmation ASAP!

Request from the DAQ Group

DAQ & the Project are asking for clear readout scheme diagrams from all detectors. Jeff started it showing FTOF as an example ⇒

TL volunteered to provide it for FTOF, BTOF, Roman Pots, B0

The goal is also to clarify the location of patch panels (fiber, power, etc): on vs off detector.

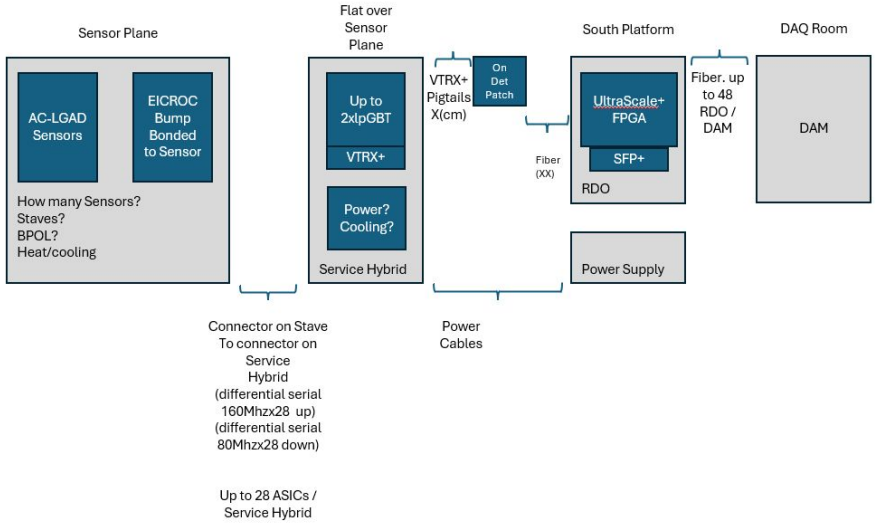
I think this is going to be very useful.

We'll start with the known stuff and put "?" where we don't know yet.

Once I'm done I will first present it to the TOF Group before sending it off to DAQ.

C) Readout Cartoons

ETOF



Come up with a format

- A Powerpoint Slide for each detector
- An excel sheet with the total number of each component
- An excel tab for each component / spec etc...
- DSCs should supply info – but either Electronics and DAQ or TIC should organize it.
- X,Y,Z positions of each type of electronics (or a specified range of values)

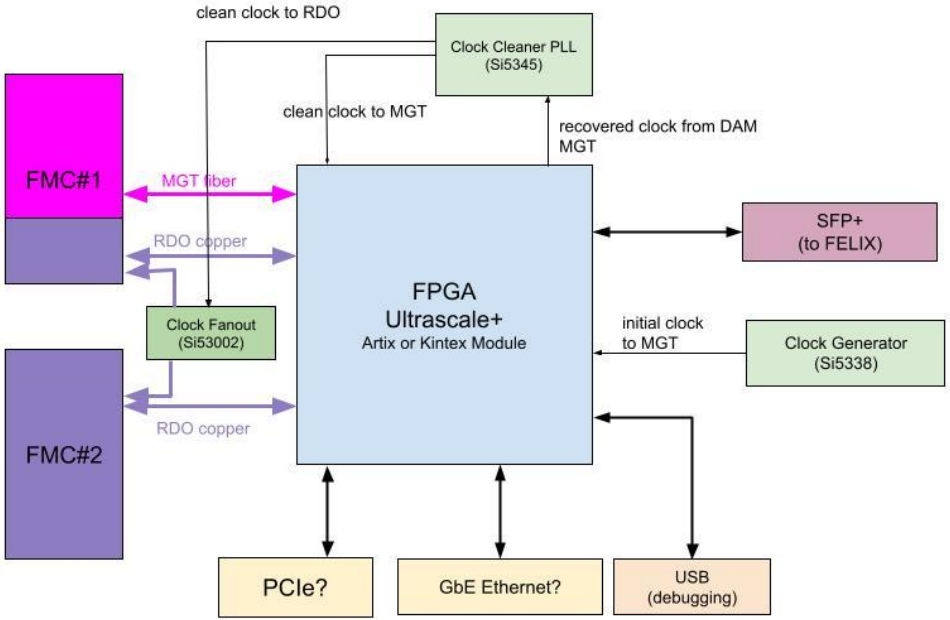
“Combined” RDO

Either a “Normal” FPGA-based RDO

or

Fiber Aggregator RDO

Tonko Ljubicic, Rice University
Oct 7, 2024



Commercial FPGA SOM examples:

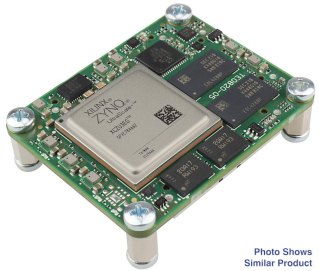
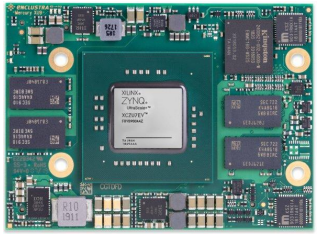


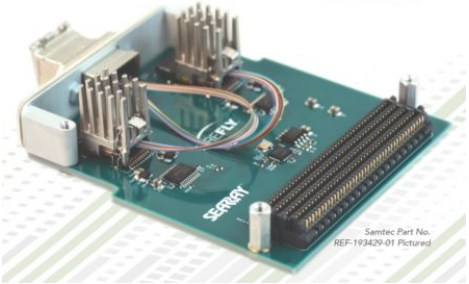
Photo Shows
Similar Product



Combined RDO Main Points

- FPGA based (Xilinx Ultrascale+)
  - we should aim for a FPGA SOM module e.g. 4x5 inches
    - Commercial: Trenz, Enclustra, etc
    - Our own: Miklos et al (EPIC Calorimeters) are already in the design phase with a very interesting module
- connects to “the FEB” either via fiber **OR** via copper cable
  - 2x FMC HPC connectors
    - 1 for commercial FMC fiber cards OR for custom, copper based RDOs
    - 1 only for custom, copper based RDOs
  - same board can be either a “fiber aggregator” OR a “standard” copper-based RDO
    - thus “combined”
  - supports either
    - 8-10 fibers (see on the right) OR
    - 32 copper FEBs/ASICs
- will be located away from the beam/detector (to be discussed!)
  - easily accessible
  - in low radiation area
  - no magnetic field
  - can be installed in cheap racks for convenience
  - NOTE that this is true for TOF and friends
- 1 SFP fiber link to DAM board
  - IMPORTANT: clock is recovered from the DAM link ala TCLink
- clock handling should be pristine with very low jitter
  - includes clock cleaner and general low jitter handling throughout the board ala ppRDO
- external interfaces
  - GbE for standalone operation (?)
  - PCIe for direct readout of the data ala FELIX (?)
    - becomes a low cost FELIX-equivalent for prototyping and standalone operation
- cheap
- simple to design and maintain
  - uses commercial components: FMC cards, FPGA pre-made swappable modules, SFP+ modules, power-management DC-DC converters etc

Commercial Optical FMC Transceivers



2-Port QSFP28 (2x100G) / QSFP+ (2x40G or 2x56G) FMC Module (Vita57

Prototyping, Phase I: ppRDO

- we plan to use our ppRDO as the first v0 prototype
  - Fiber Aggregator: it has 2 fibers: 1 to DAM, 1 aux to TOF lpGBT RDO (e.g.)
  - RDO: already designed for it with the FMC connector (supports 8 FEBs/ASICs)
  - IMPORTANT: it is the only board which has the clock recovery and precise clock distribution electronics (development kits don't)
- Step 1: local clock only (no recovered clock from DAM)
  - **Main Goal:** learn how to talk to lpGBT using CMS ETL RB (obtained from Rice!)
    - note that we also have a CERN ETROC ASIC board available from Rice
  - engineering: who? Zhenyu et al? TL?
- Step 2: recovered clock from the DAM
  - make a full chain: "DAM"->ppRDO->lpGBT ETL RB
  - **Goals:** clock recovery from DAM fiber, protocol development, fast readout, etc…
  - NOTE: we need a DAM candidate
    - preferably an FPGA board with PCIe interface → commercial → which one?
      - ALINX has a nice candidate
    - and we need engineering for DAM firmware: who? TL?

Prototyping, Phase II: Combined RDO V0 (“cRDO”)

- design & produce a Combined RDO prototype, version 0
  - set the requirements by discussion with
    - TOF & FF friends: lpGBT fiber based
    - copper or fiber(?) based: FPGA
      - Calorimeters (Norbert; CALOROC), MPGD (Irakli; SALSA), Forward ECAL (Gerard; off-the shelf ADC)
      - they are also considering lpGBT… TBD.
    - SVT: lpGBT fiber based aggregator (Jo)
    - others?
  - design a V0 prototype board
    - engineering – who? where?
  - produce it…
  - program it…
  - evaluate it… use it…
- Also note that the Calorimeter group (Norbert & Miklos et al) are already designing cards that might fit our needs
  - met with Miklos, Norbert on 10/9 to discuss this… Under consideration.
- I also discussed this with Jo for SVT (lpGBT aggregator)
- I will also discuss this with Irakli for MPGD, Gerard for FECAL → next week
- And then re-discuss with all proponents to see if we can make an agreement “soon”