



# DAQ Demonstrator

Atanu Modak

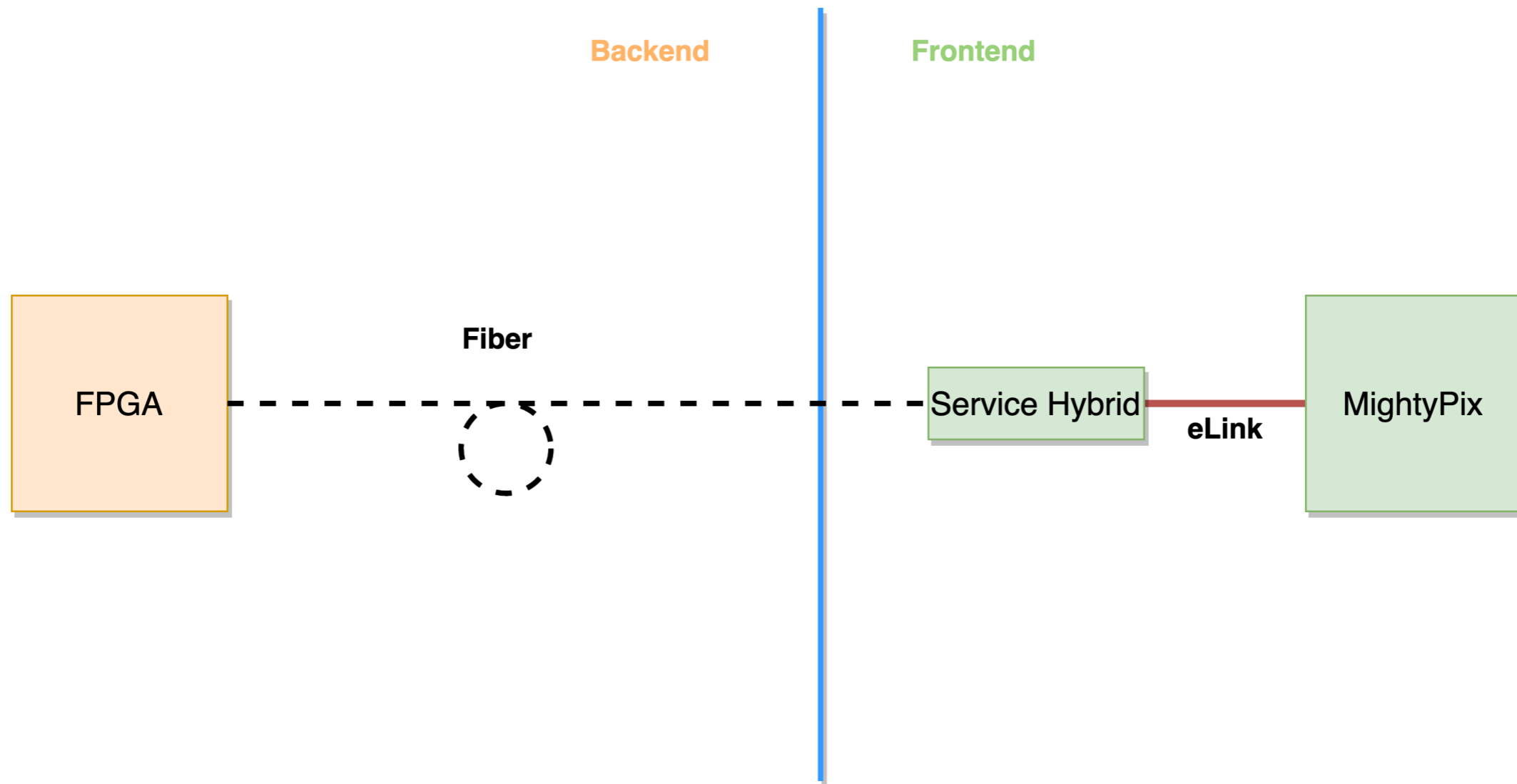


Science and  
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Facilities Council

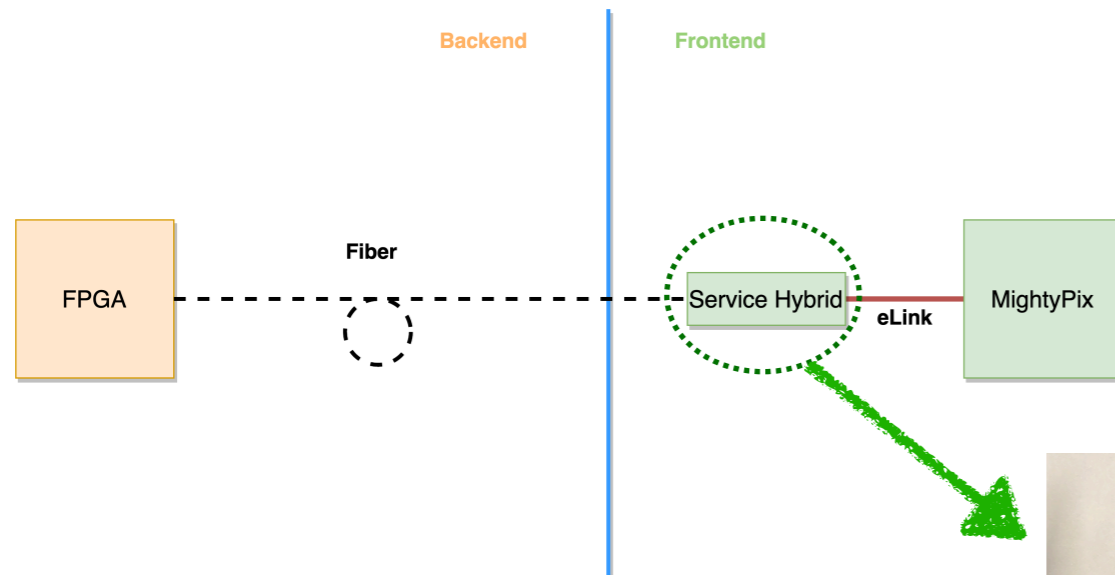
Particle Physics

# Motivation

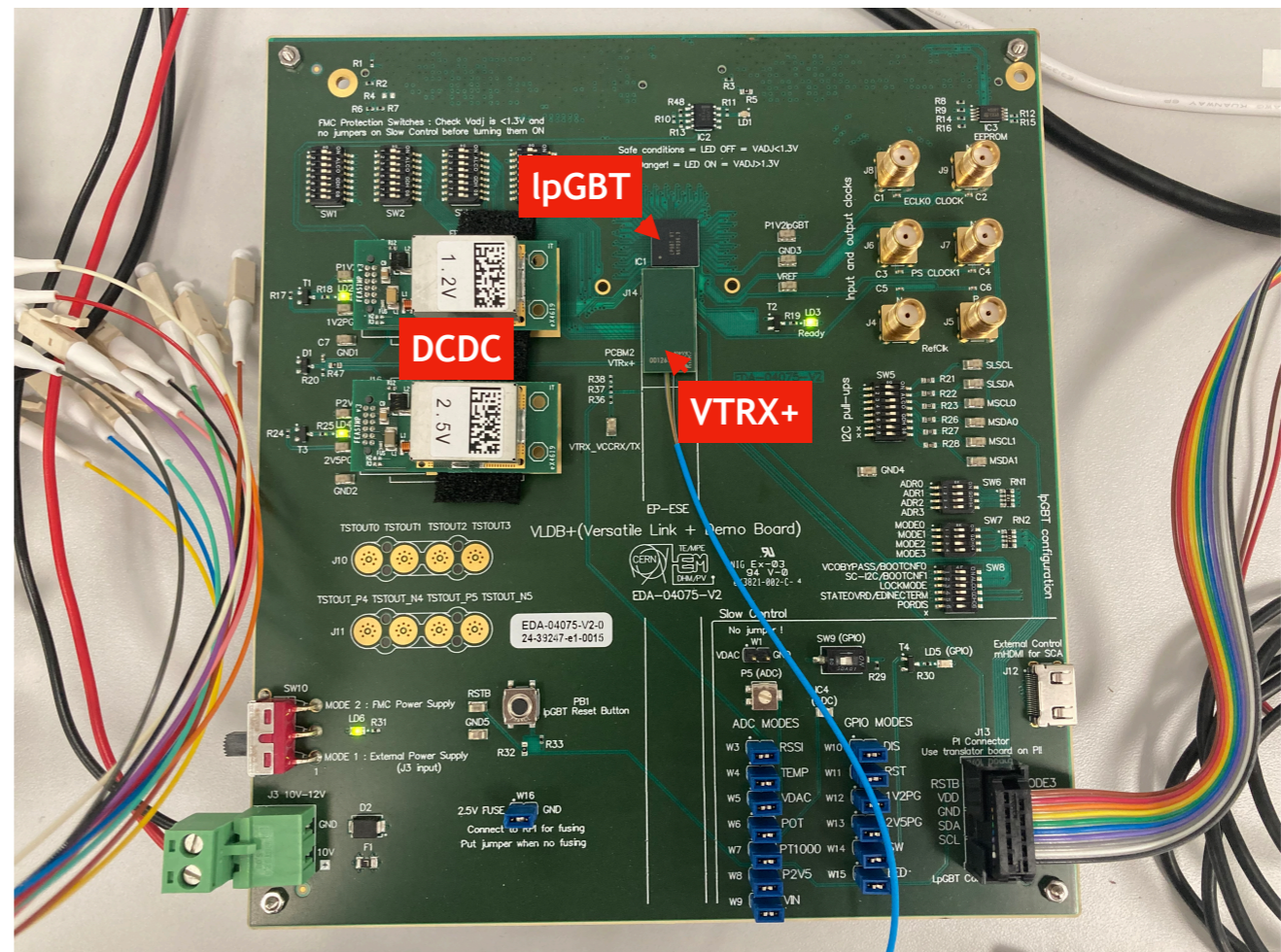
Demonstrate a full DAQ chain with final system like components for LHCb tracker upgrade in LS4 (2033-34)



# Available Hardware

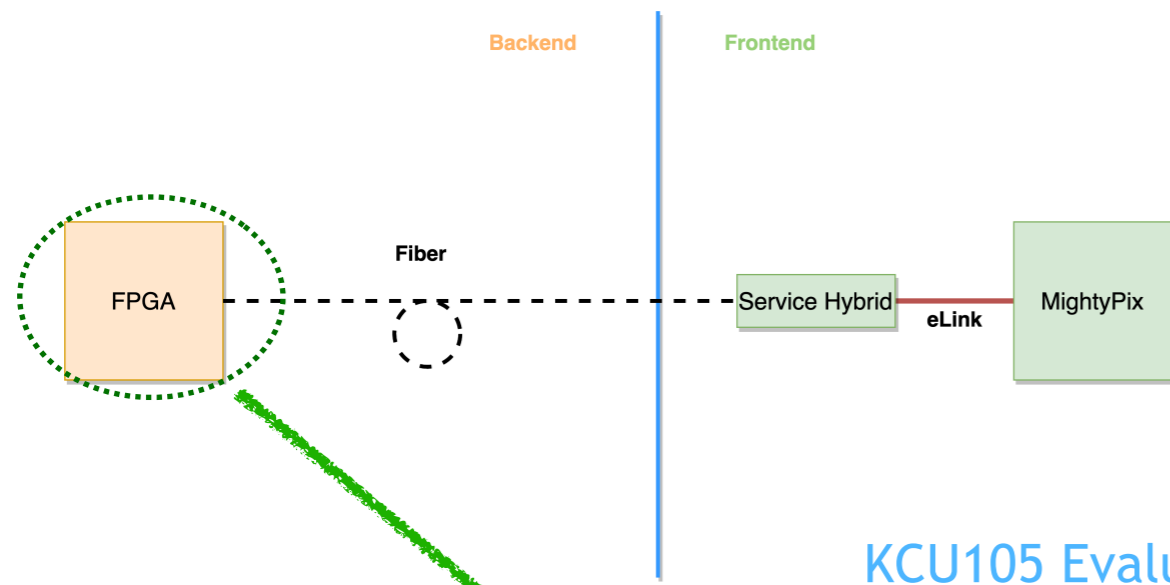


Versatile Link Demo Board (VLDB+)



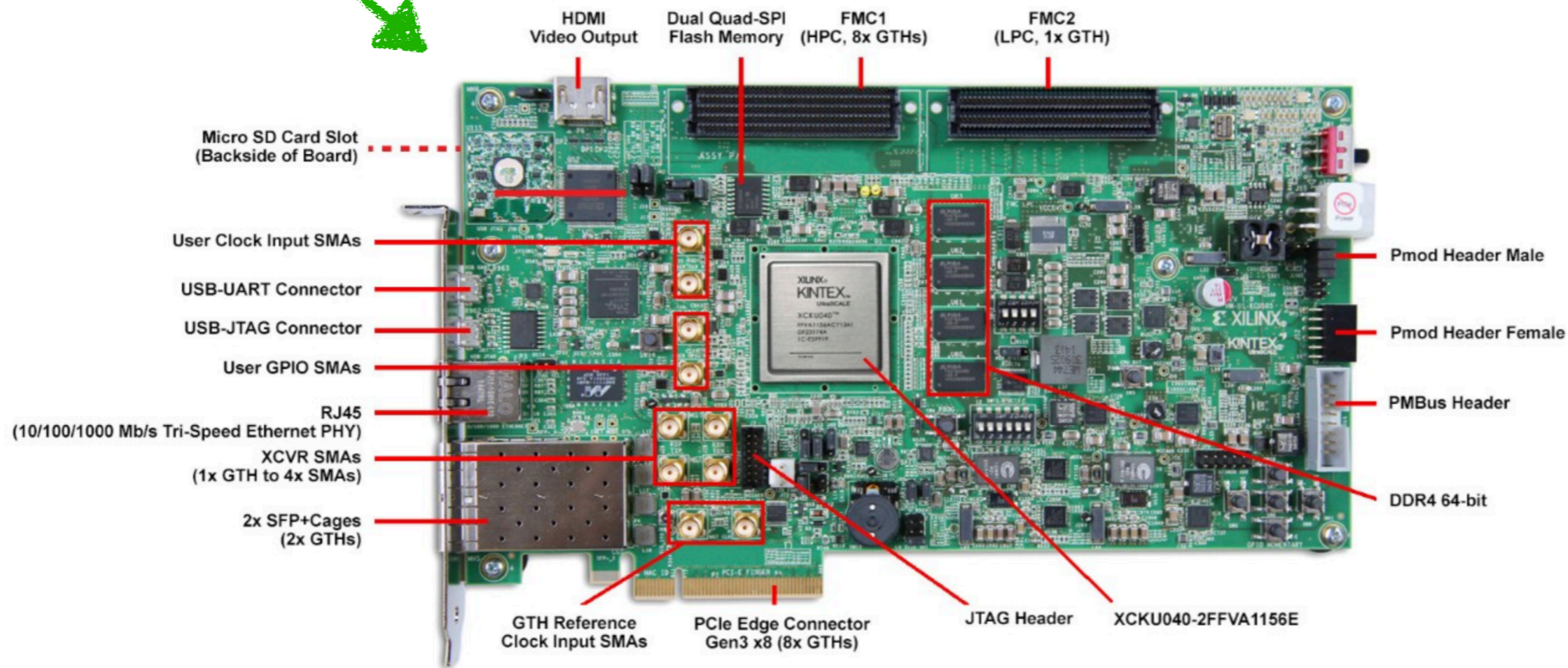


# Available Hardware



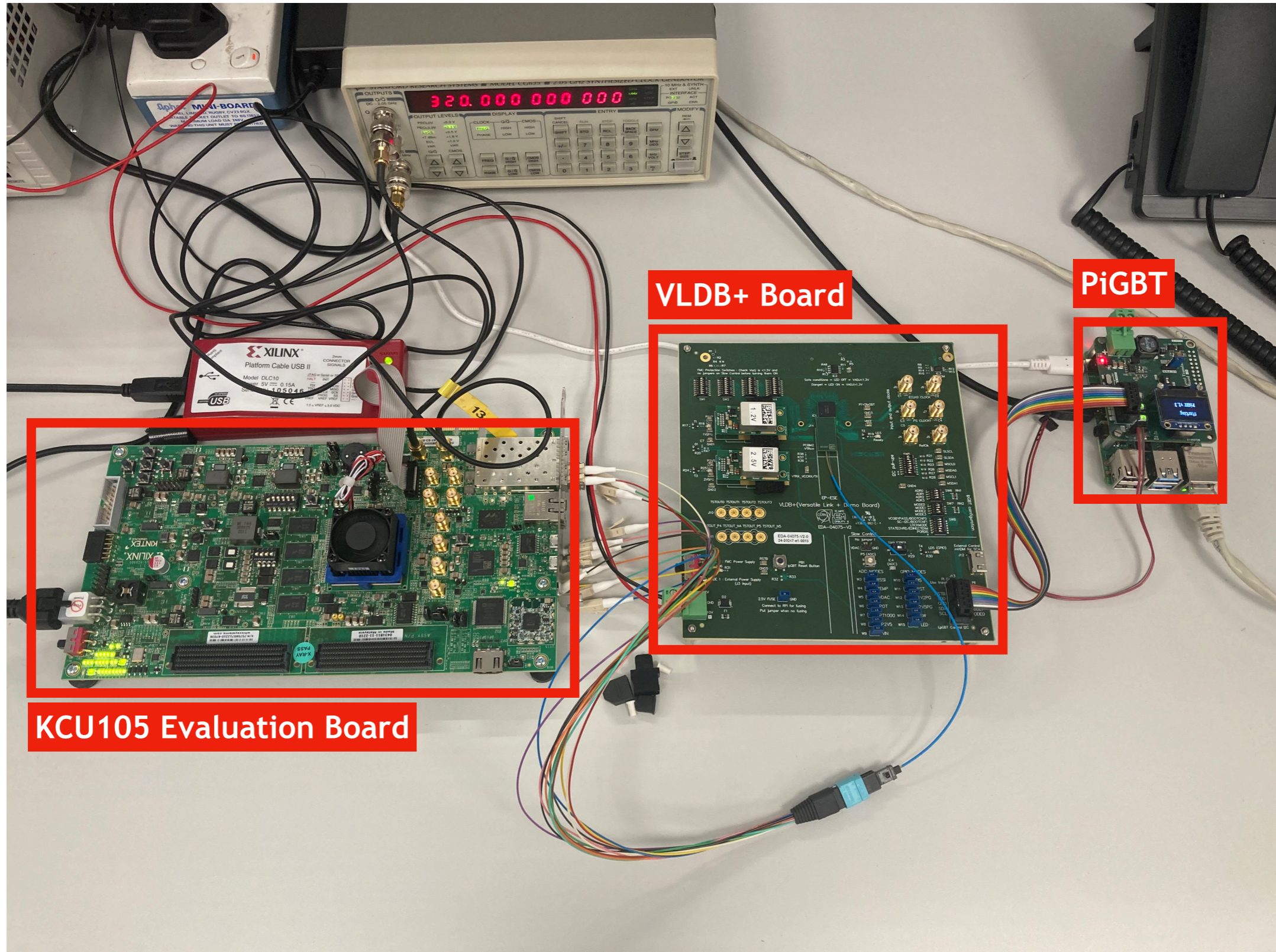
KCU105 Evaluation Board

Chosen because of firmware support and availability, other options were: vc707, vcu108, vcu118





# Hardware Setup



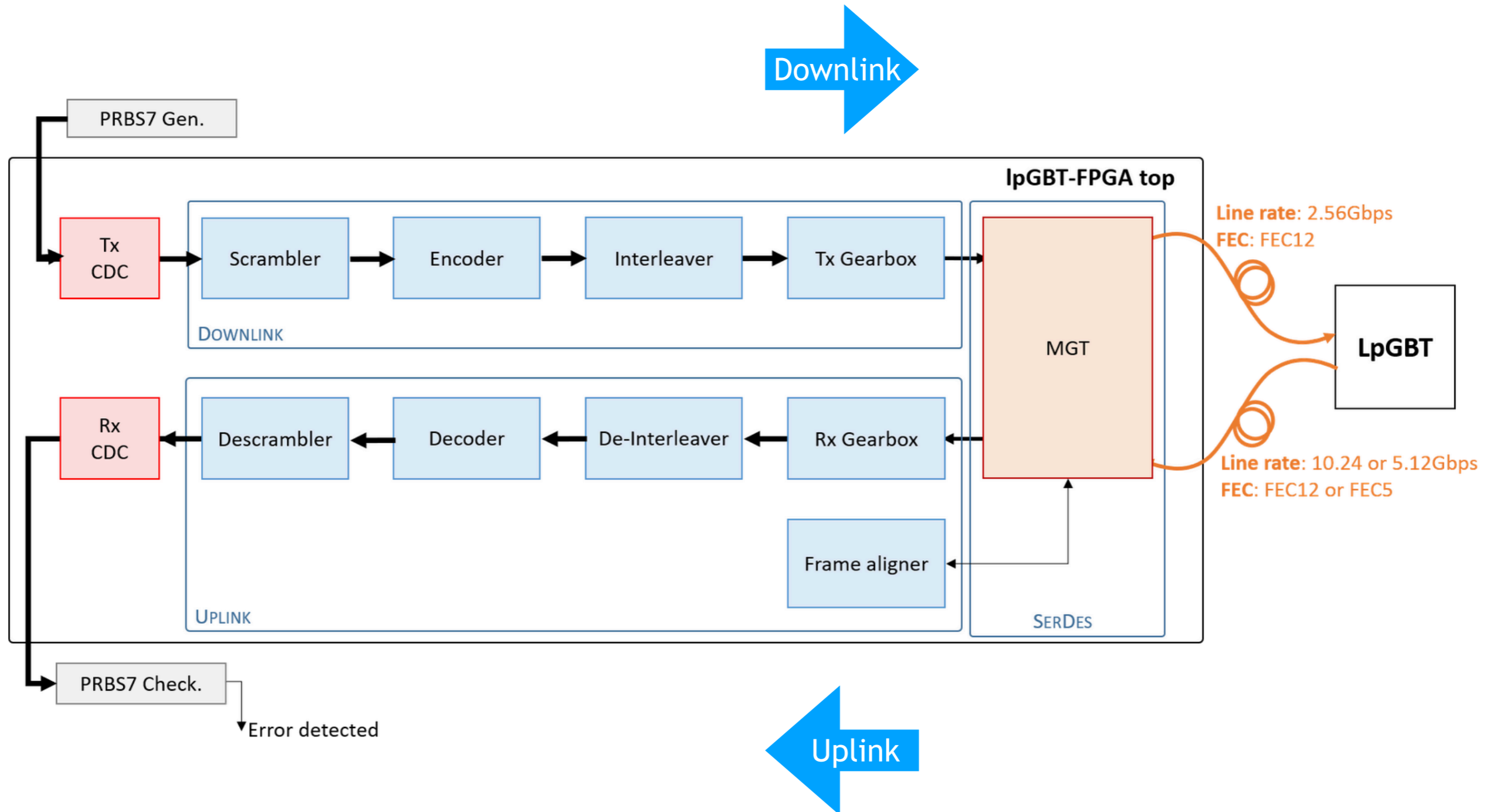
VLDB+ Board

PiGBT

KCU105 Evaluation Board



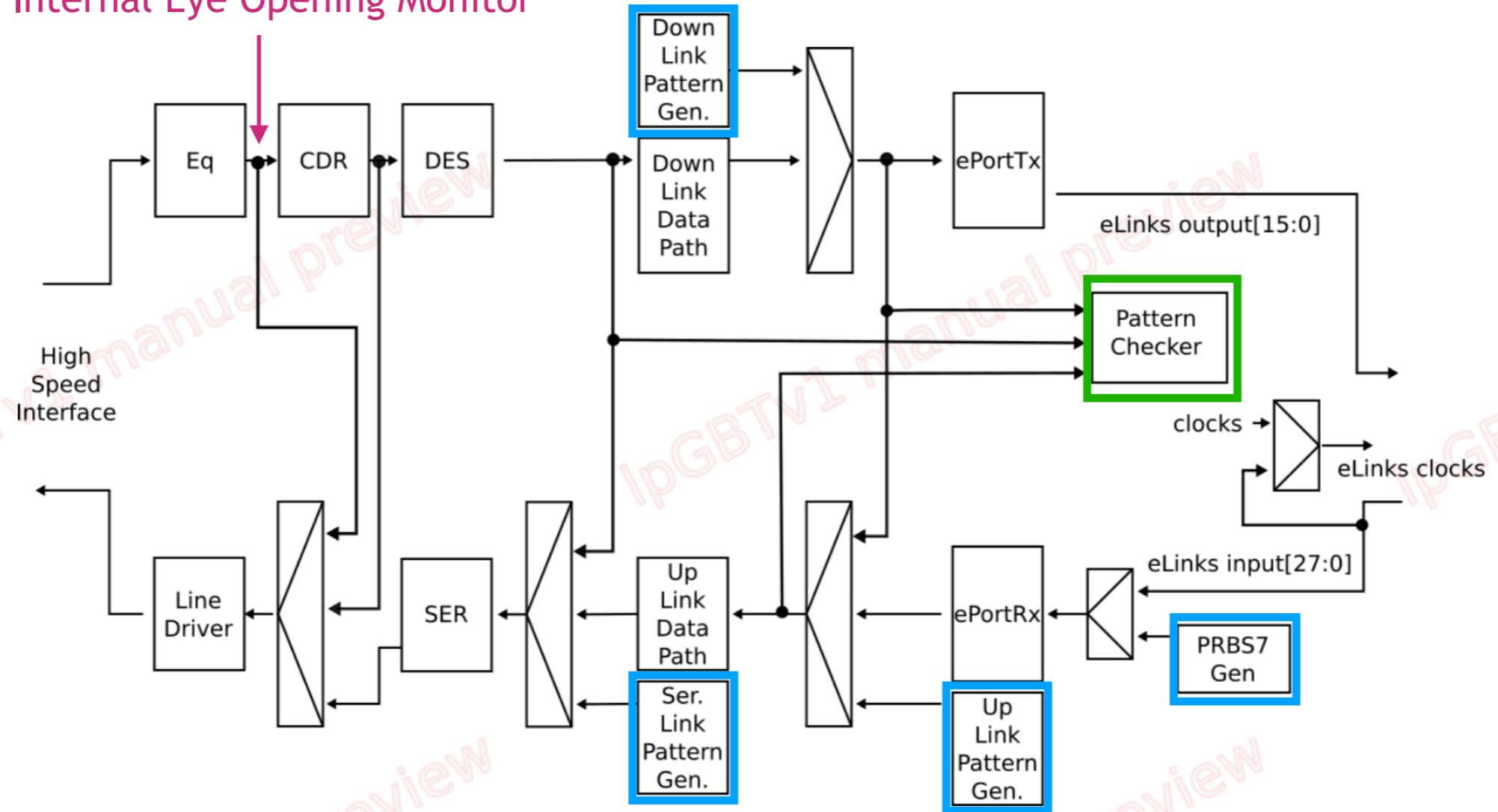
# Firmware Block



# IpGBT test features

## IpGBT architecture

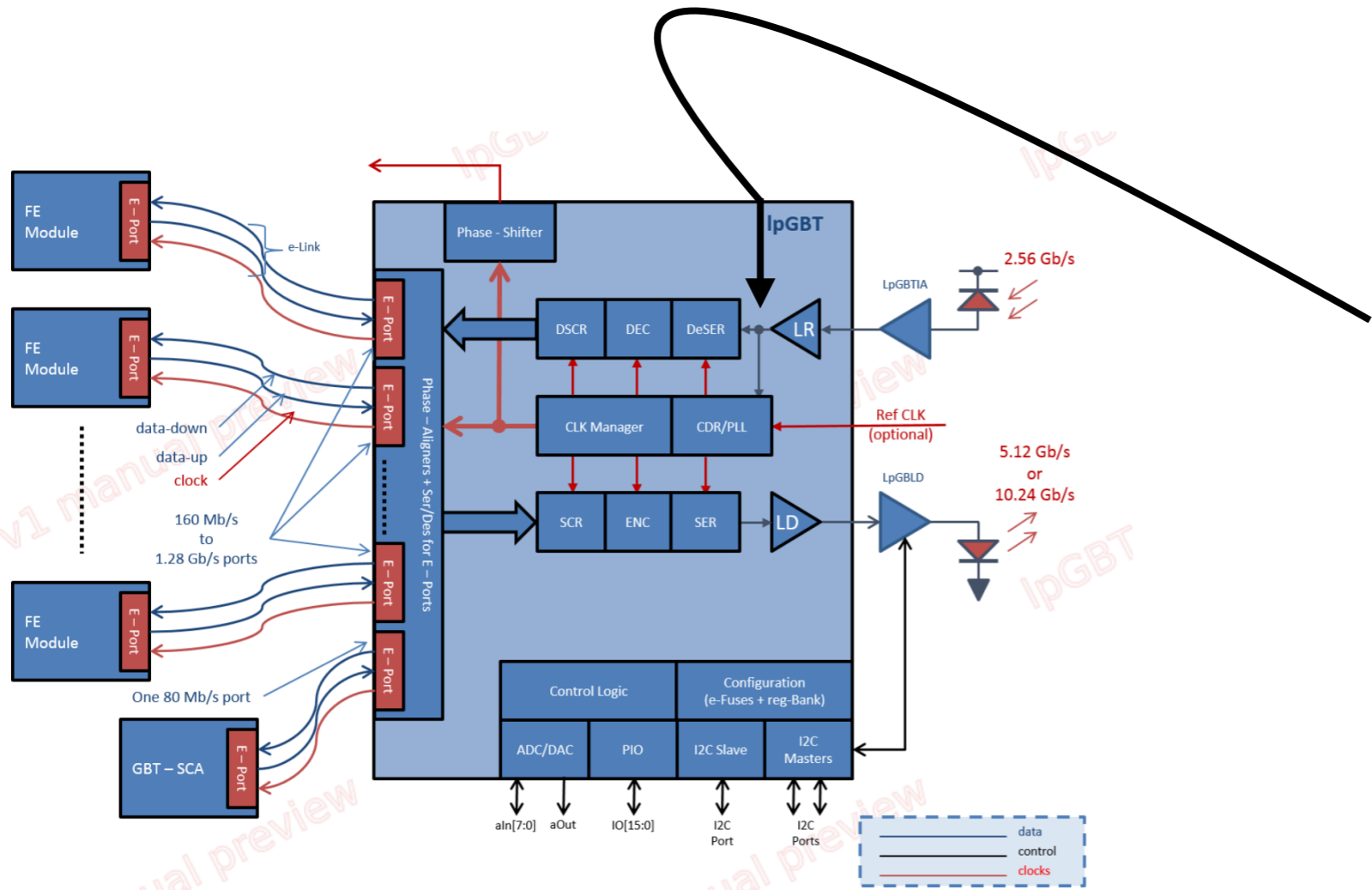
Internal Eye Opening Monitor



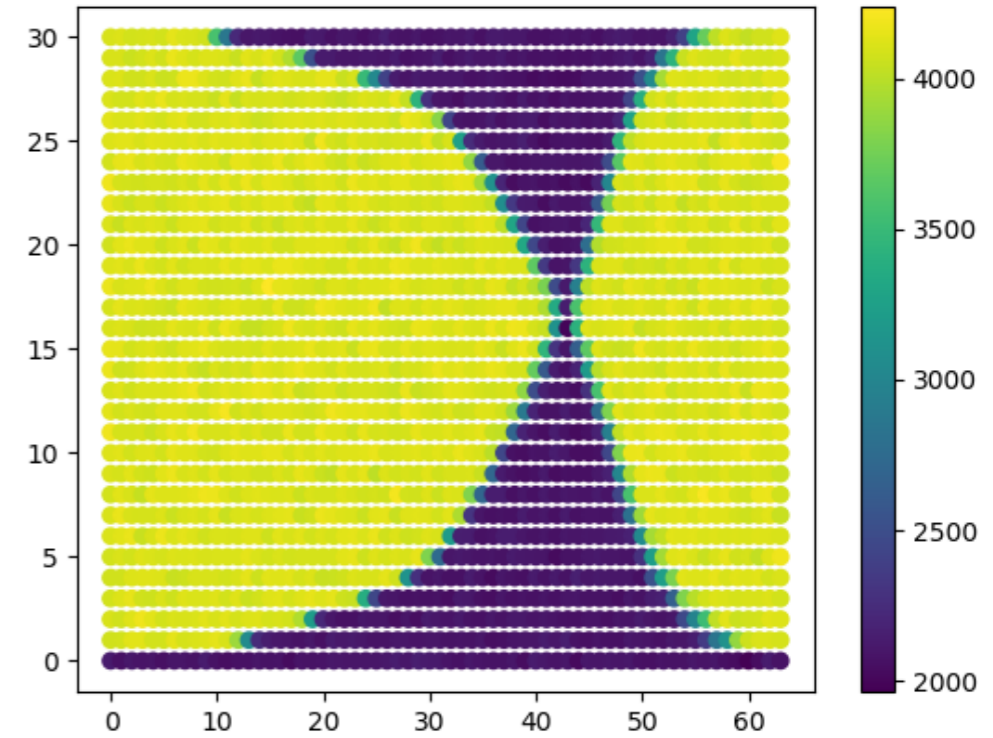
Internal **Pattern Generators** and **Pattern Checkers**



# Downlink signal quality

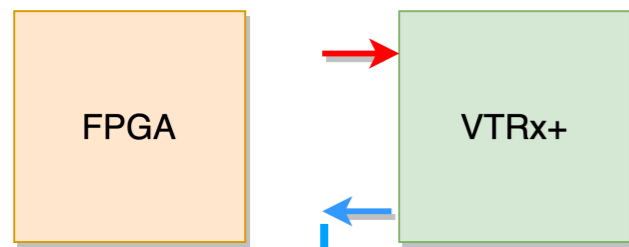


lpGBT architecture

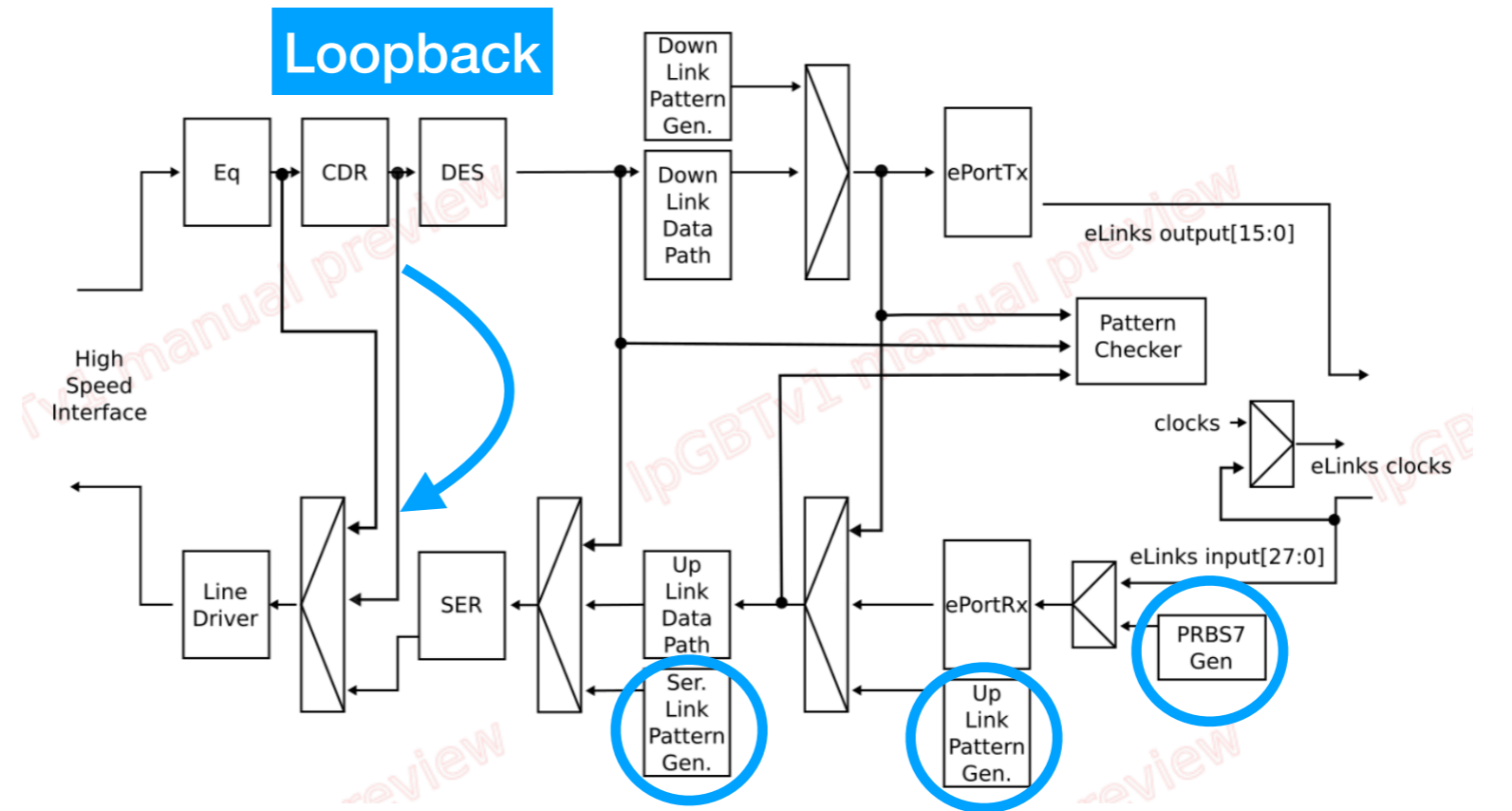




# Uplink Optical Eye: Setup



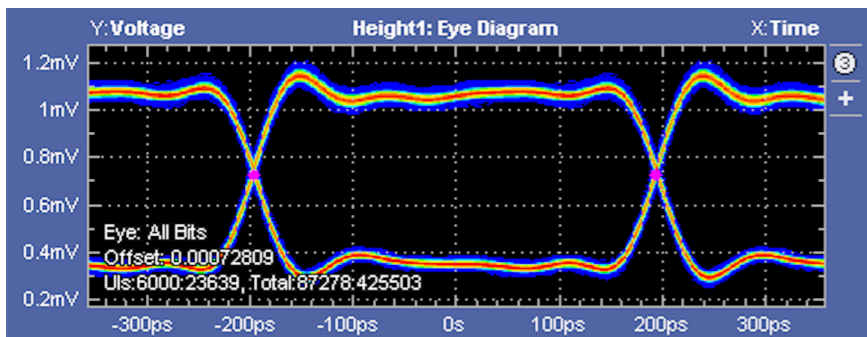
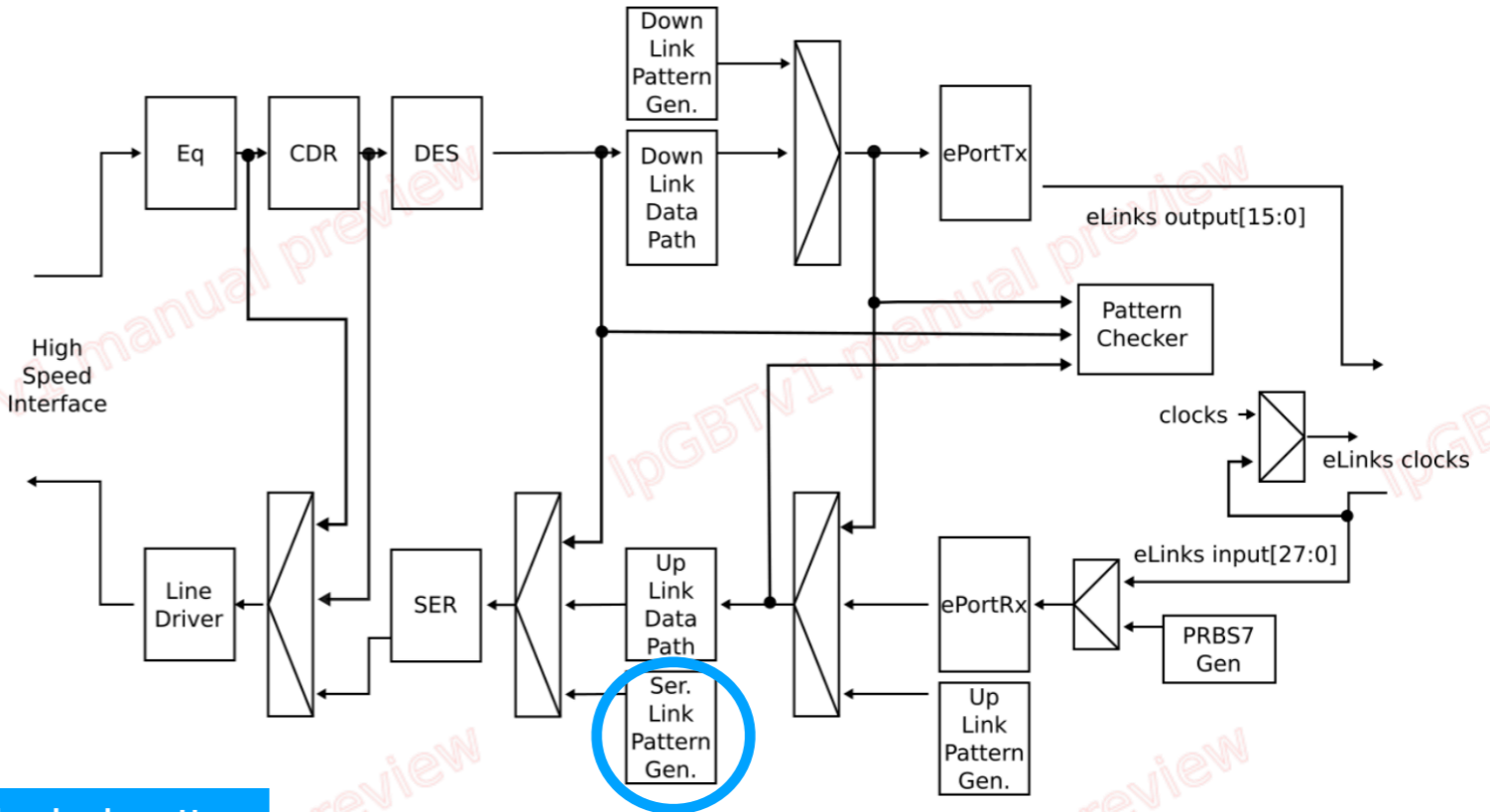
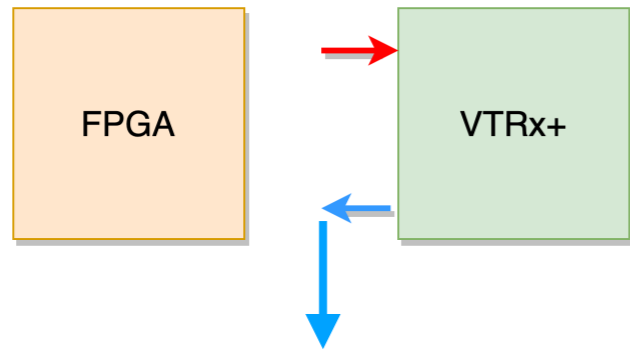
VTRx+ MT pigtail  
+  
MPO to LC fanout (40 cm)  
+  
LC to FC (30 m)



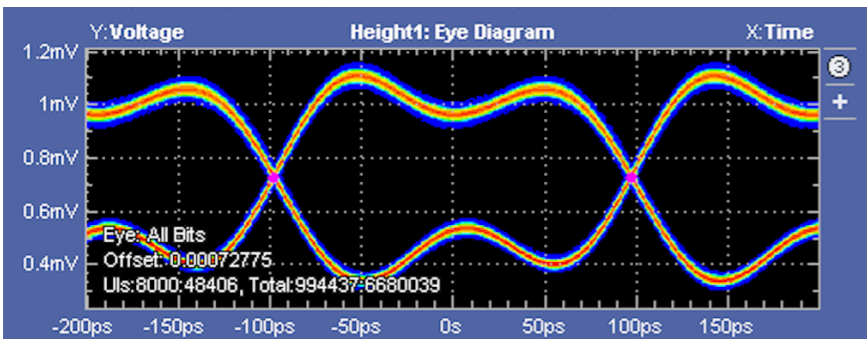
33 GHz Scope



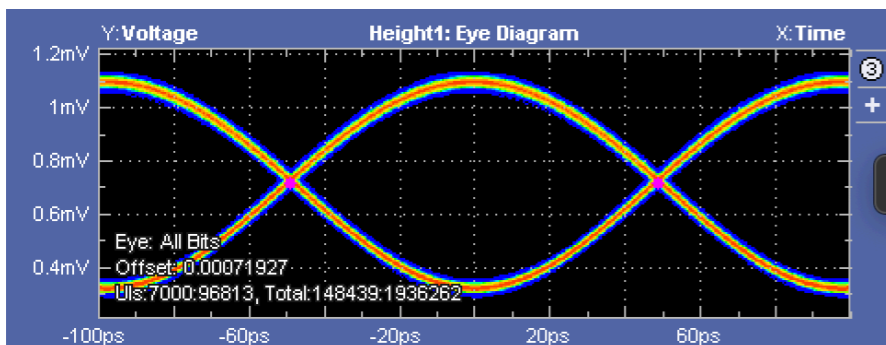
# Uplink Optical Eye



1.28 GHz clock pattern



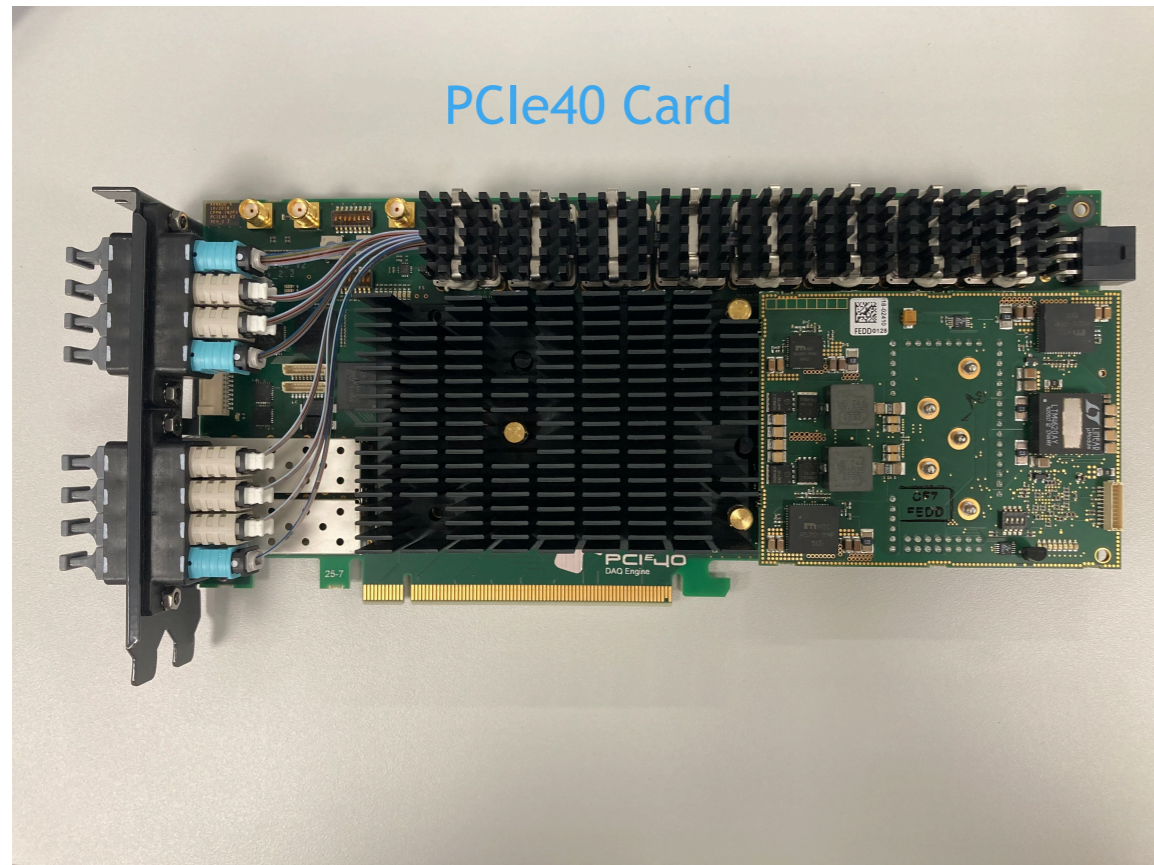
2.56 GHz clock pattern



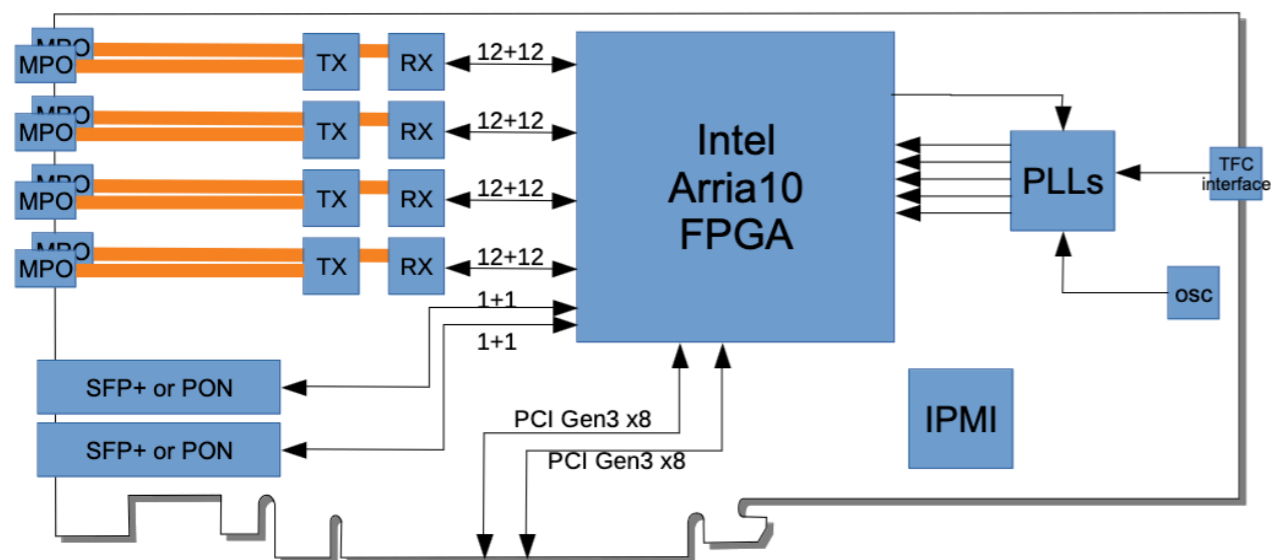
5.12 GHz clock pattern

ULSerTestPattern[3:0]	Name	Description
4'd0	DATA	Normal mode of operation
4'd1	PRBS7	PRBS7 test pattern (x7 + x6 + 1)
4'd2	PRBS15	PRBS15 test pattern (x15 + x14 + 1)
4'd3	PRBS23	PRBS23 test pattern (x23 + x18 + 1)
4'd4	PRBS31	PRBS31 test pattern (x31 + x28 + 1)
4'd5	CLK5G12	5.12 GHz clock pattern (in 5Gbps mode it will produce only 2.56 GHz)
4'd6	CLK2G56	2.56 GHz clock pattern
4'd7	CLK1G28	1.28 GHz clock pattern
4'd8	CLK40M	40 MHz clock pattern
4'd9	DLFRAME_10G24	Loop back, downlink frame repeated 4 times
4'd10	DLFRAME_5G12	Loop back, downlink frame repeated 2 times, each bit repeated 2 times
4'd11	DLFRAME_2G56	Loop back, downlink frame repeated 1 times, each bit repeated 4 times
4'd12	CONST PATTERN	8 x DPDataPattern[31:0]

# LHCb miniDAQ

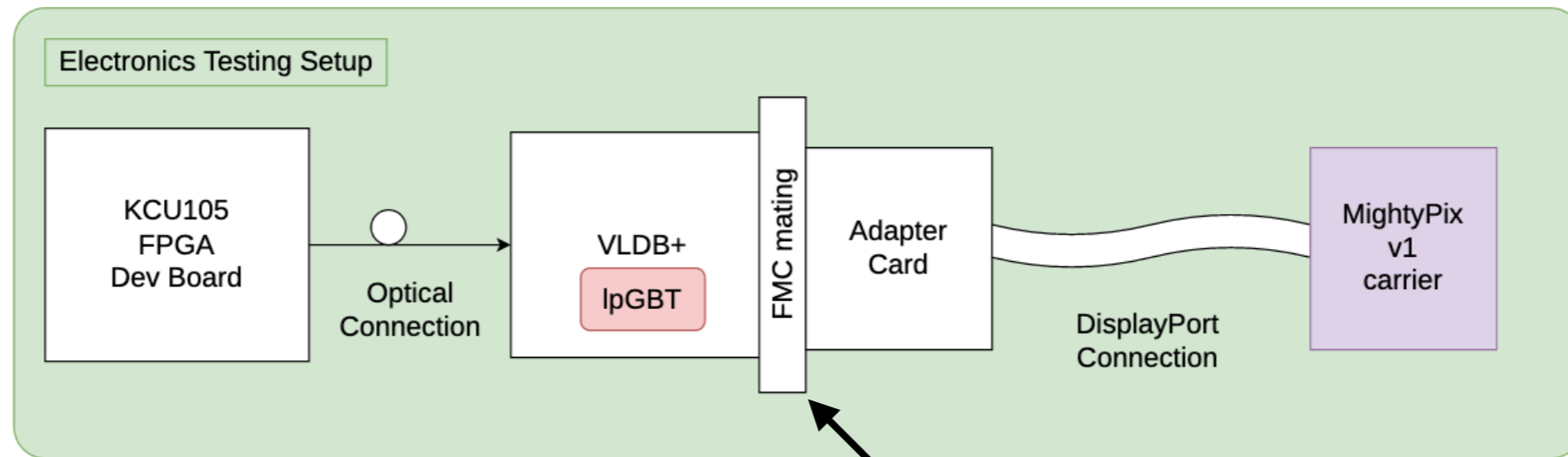


- PCIe40/PCIe400 based DAQ card will be used in the backend for the upgraded detector
- Developing a LHCb-like miniDAQ system using PCIe40: provides 48+48 bidirectional fibre connection
- lpGBT-FPGA core is under development

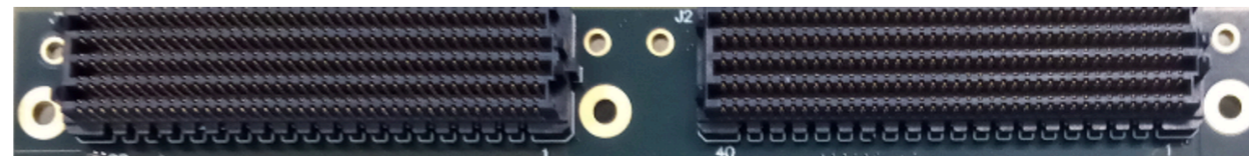


# DAQ Chain with FE attached

- Add MightyPix1 (our FE sensor) on the front-end to have a complete readout chain
  - This setup can also serve as a test bench for eLink (flat-flex) development, and off-chip component testing



eLink clock, data in/out, i2c signals available on the VLDB+ FMC

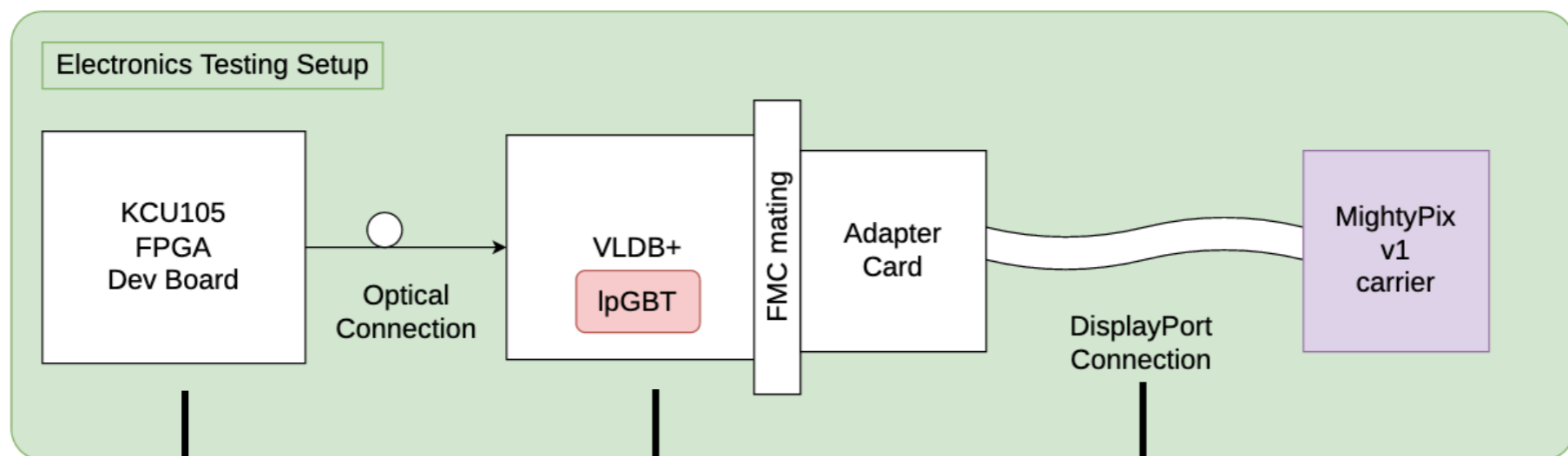


Presently I am checking if the FE data-lines are compatible with IpGBT input



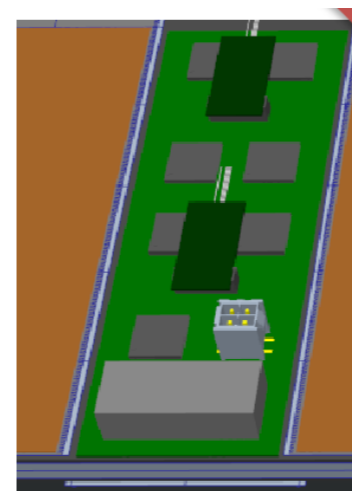
# Final DAQ chain

- Full system level DAQ chain



Replace this with proper flat flex

Replace this with proper service hybrid



This is an example service card being designed for LHCb tracker (using lpGBT, VTRx+, bPOL)

Replace this with LHCb style miniDAQ with PCIe40

***Thank You***