TOF Layers (BTOF & FTOF) pre-TDR (v0.1.2) review

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October 26, 2024

The current technical designs of the ePIC TOF detector systems, BTOF and FTOF, including their associated readout electronics and DAQ are presented in section 8.3.4.1 of pre-TDR version 0.1.2 (10/10/2024), p. 80 to 100.

From the pre-TDR overall table of contents (page v), the TOF layer section consists of 3 subsections:
- Requirements and Justifications
- Implementation
- Additional material

Instead the content of the TOF layer section (8.3.4.1) features multiple subsections:
- Requirements and Justifications
    - Requirements from physics
    - Requirements from Radiation Hardness
    - Requirements from Data Rates
        * BTOF
        * FTOF
        * Electronics noise
        * Data Rates
- Device concept and technological choice => AC-LGAD sensors
- Subsystem description:
    - General device description
    - Sensors
    - Front-End Electronics
    - Flexible Printed Circuit boards
    - BTOF stave design
    - FTOF module design
- Performance

- Implementation
    - Services
    - Subsystem mechanics and integration
    - Calibration, alignment and monitoring
        * Monitoring
    - Status and remaining design effort: eRD112 and eRD109
        * eRD112: Sensor R&D effort
        * eRD109: readout R&D effort

- E&D status and outlook (E&D: Exploration & Development?)
- Environmental, Safety and Health (ES&H) aspects and Quality Assessment (QA planning)
- Construction and assembly planning
- Collaborators and their role, resources and workforce
- Schedule
- Risks and Mitigation strategy

- Additional Material
    - Low-voltage and High-voltage powersupplies
    - Schedule
    - Particle identification

General comments:

The proposed text demonstrates that the design of the TOF detector systems benefits from simulation works, prototype testing and advanced thinking to meet the constraints of physics in terms of particle identification, supplementing other ePIC detector systems. An important part concerns the developments of AC-LGADs readout systems, from Front-end electronics to Back-end and DAQ. Modules assembly schemes, quality assessments and tentative schedules are also presented.

To my opinion, the TOF layer section could gain in clarity by rearranging subsections (avoiding multiple repetitions) and by more clearly separating the BTOF and the FTOF specificities, rather to mix them in each sub-sections, which makes the reading very difficult to follow.

From my point of view, to help the readers it should be stated from the beginning that the BTOF relies on strip AC-LGADs and FTOF on pixelated AC-LGADs. The difference between the 2 species of AC-LGADs in terms of specifications/requirements (input capacitance, …) should also be introduced. As an illustration, the 1st time BTOF and FTOF are described, table 8.12, there is no mention to strip nor pixelated sensors.
Be assured that the points I am addressing are only to contribute to improve the text.
Overall I regret that the proposed text does not reflect the authors' high level of detail clarity of the systems.
The subsections "Requirements from Radiation Hardness" and "Requirements from Data Rates" seems to me more statements from needs rather than requirements. Furthermore the paragraph, page 92 (lines 2344 to 2356) + figure 8.41), discussing irradiated sensors might be integrated to the "Radiation Hardness" subsection.
The subsections "Requirements from Data Rates" and "Low-voltage and High-voltage power supplies" are particularly difficult to follow/understand.
Some figures are really too small: 8.41, 8.46, 8.48 (schedules).
Some figures lack clarity, e.g. 8.32: (left) BTOF geometries and charge sharing distribution => no dimensions and hard to see what an insert looks like, can't see the charge sharing distribution + no scale; (right) "layout of sensor modules and service hybrids of FTOF" => a more exhaustive legend (to what correspond the different colors) could help. Furthermore, one can find a part of the missing caption of fig. 8.32 page 85, lines 2195 – 2196).
Some figure/table captions should be more explicit, e.g. Fig. 8.34 and Table 8.13 => from simulation?
Some acronyms are not defined: BV (line 2185): Biased Voltage? AWG (Table 8.14)? CV (line 2422)?
erd112 and erd109 => **eRD**112/109 for each occurrence.

"Requirements and Justifications":

- Table 8.12:
  * FTOF: channel count **3.2 M** but page 83, line 2095, it is written **5.8 M**…
- Figure 8.33: no labels, nor particle IDs for "Barrel TOF PID" left figure. Difference between Fig. 8.33 & Fig. 8.49 (Additional Material)?
- "Requirements from Radiation Hardness": to my opinion, this subsection should appear after the detailed description of the 2 subsystems and should include the paragraph page 92 (lines 2344 to 2356) + figure 8.41.
- Sentence/statement not clear to me: "The leakage current increase due to radiation damage for the fluence in ePIC has to be low enough not to trigger a thermal run away combined with the power dissipation from the readout chip, especially for the forward and end-cap region where the chips are bump bonded on top of the sensors", lines 2070-2073. Cooling system?
- "Requirements from Data Rates": very difficult to follow/read/understand how the counts are made… Personnally, I got lost… A table might help.
- Concerning the "Electronics noise" (lines 2098-2099): "Noise measurements have consistently shown a rate of 30 Hz per channel. Such a noise rate is achieved with a 5-sigma cut ..." => From which measurements? To my opinion, this sentence calls for a more explicit explanation.

- "Device concept and technological choice" correspond to a description of the AC-LGAD and the motivation to implement them. A suggestion would be to include this part within the "Subsystem description".
- Lines 2126-2127: "The AC-LGAD technology has been chosen to **be** use**d** for particle identification, tracking, and far-forward detectors at EIC where precision timing and spatial measurements are needed.". "far-forward detectors", not the BTOF?

"Subsystem description":

- "General device description" & "FEE": the mixing of BTOF & FTOF from one sentence to the other is really confusing.
- It could be interesting to motivate the investigation of larger pitch and sensor thickness optimization.
- Lines 2173-2175: "The prototype is currently under testing, **with noise issues being addressed for future iterations**. The next version, EICROC1 (expected in 2025), will feature a **16x8** channel configuration, followed by the final 32x32 channel version for full-scale implementation." FYI, the EICROC0 noise issue was solved by firmware adjustment end of June 2024. EICROC1 will feature 8x32 (possibly 32x32, but no digital on top design).
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- Line 2185: BV? Biased Voltage?
- Line 2186, "low voltage for ASIC". Even though EICROC0 operates at 1.2V, the LV applied to the PCB is ~3V.
- Fig. 8.35 shows service hybrids for FTOF, why no equivalent for BTOF? Idem consideration for Fig. 8.36
- "BTOF stave design" (line 2215): 64 sensors and 128 ASICs on each side of the half-staves => 2 ASICs per strip sensor??

"Performance":

- Lines 2247-2253: "Assemblies … were developed by BNL, IJCLab, OMEGA, and Hiroshima group" ???=> To my knowedge, only the BNL team wire-bonded EICROC0 + 4x4 pixelated AC-LGAD to test boards designed by OMEGA. Some others were wire-bonded in by IPHC Strasbourg (France).
- Lines 2249-2253: "Testing includ**ed** scans of the analog and **digital components using charge injection and beta particles from a Sr-90 source**, resulting in a measured jitter of 8-9 ps for charges above 20 fC. Both wire-bonded and flip-chip assemblies were developed for various characterizations. Additional tests using Transient Current Technique (TCT) laser scans **were conducted** to map out charge distribution, and various tests are still ongoing.". I am surprised by the past tense of the sentences above in bold. The jitter associated to EICROC0 presented in Fig. 8.42 shows rather 10 to 15 ps above 20 fC… Updated plots should be presented.

"Implementation":

- Lines 2271-2273: "For FTOF, several types of SHs are used, covering 12, 24, or 28 sets of sensors and ASICs. The SH is distributed on the mechanical and support disk, together with sensor modules." => Ref. to Fig. 8.32?
- Table 8.14: AWG?, HV replaces BV used before? Different colors for BTOF and FTOF cells could help to distangle the 2 systems.

- "Subsystem mechanics and integration": this part could be group with the subsystem description, as a whole.
- Lines 2290-2292: "Both detector subsystems have 7.5cm space in radial direction for BTOF and in the beam direction for FTOF." => not clear for non TOF experts.
- Lines 2300: "**Calibration, alignment and monitoring:** ~~**Calibration and alignment:"**~~
- Lines 2311-2313: "The distribution of the reconstructed time at the vertex of these tracks – assuming they are pions – **should an rms spread** of approximately 50 ps, including the time spread of the luminous region and detector resolution."

"Status and remaining design effort":

- Line 2323: "HPK sensors from the latest production have been tested at the Fermilab test beam facility." => Strips? When have they been tested?
- Fig. 8.40: What was the readout system associated to pixelated AC-LGADs?
- Line 2334: "The new HPK production (expected by the end of this year)." => Clearer to specify 2024.
- Fig. 8.41: really too small. The whole paragraph should be gather with other "radiation hardness" topics.
- Line 2367: "input capacitance ~3.5 pF" => mimicking strip AC-LGAD capacitance?
- Line 2369-2371: "The **newly introduced amplitude readout** was found to function well, and results show 100% efficiency when combining neighboring strips." => More details on the newly introduced amplitude readout? "The time resolution measured from the beam test was around 50 ps." => Any plot available?
- Fig. 8.42 left: poor quality figure.
- Fig. 8.42 caption: "Left: FCFD Jitter measurements with 3.5 p**f (=> F)** input capacitance and charge injection. Right: EICROC Discriminator jitter versus the injected charge, determined from data on an oscilloscope. ~~Left: FCFD Jitter measurements with 3.5 pf input capacitance and charge injection~~. Plots from the **erd**112 and **erd**109 2024 reports."

"E&D status and outlook": ~~E&D activities~~

- Line 2393: "from the latest production will **be** glued to the stave"
- Fig. 8.44 => associated to BTOF.

"**Environmental, Safety and Health (ES&H) aspects and Quality Assessment (QA planning):**

- Line 2404: "The results were presented at IEEE conference…" => When? Reference?
- Line 2421: "The breakdown voltage of all devices has to be within **10%?**" => meaning of 10%'**?' ===> to be adjusted?**
- Line 2422: "CV" => meaning?
- Lines 2428-2429: "All channels have to be within **10%?** of homogeneity." => meaning of 10%'**?' ===> to be adjusted?**
- Fig. 8.45: a bit too small + colors should be adjusted to better read the text in black.

“Collaborators and their role, resources and workforce”:

- Table 8.47 caption: meaning of different colors? BTOF/FTOF teams? US/International contributions? LBNL (Zhenyu)? Why no mention to OMEGA for EICROC development, the same way as FermiLab for FCFD? OMEGA is an ePIC contributor.

“Schedule”:

- Fig. 8.48: impossible to read!
- “10% in 6 months” => specify the number of modules/staves it represents to give an idea for FTOF/BTOF, respectively.

“Risks and mitigation strategy”:

- Line 2504: “may be needed”

“Additional Material”:

- “Low-voltage and High-voltage power supplies”: not accessible for non experts. “Amps” => A ; KW => kW ; “500VDC” => 500 V DC
- Line 2537: “10 ma” => 10 mA
- Line 2549: “4 months from submission to delivery” => could last up to 6 months for the ASICs…
- Line 2554: “EICROC3” => It might be rather EICROC2_v1…