

# eRD109 Update - H2GCROC3A

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# Some future tests

## Finally starting to sum:

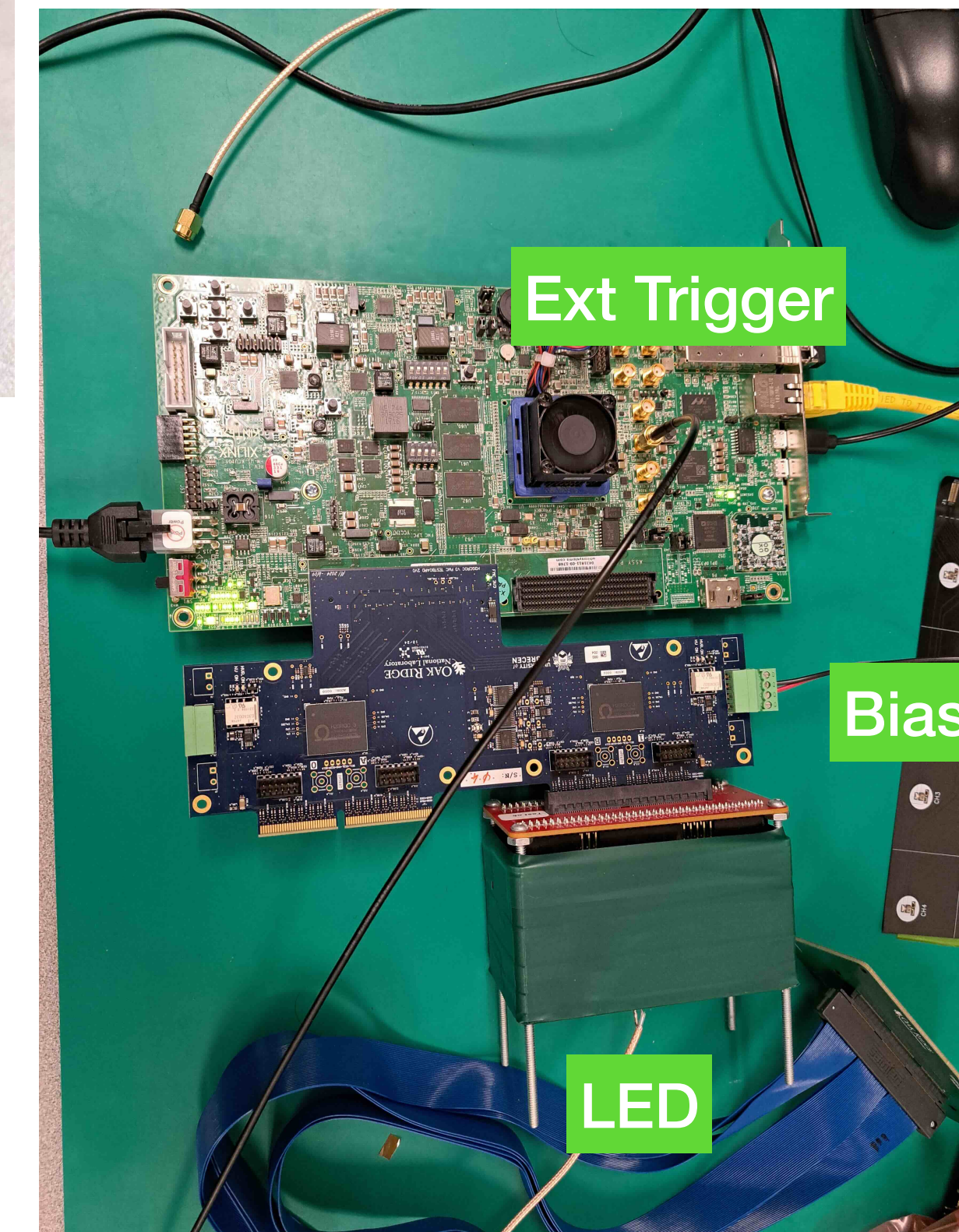
- The summing board is designed
  - There is a switch to 'sum' 1-8 SiPM's, using the BIC 4x4 SiPM array for this
  - We are starting the testing with the LED setup



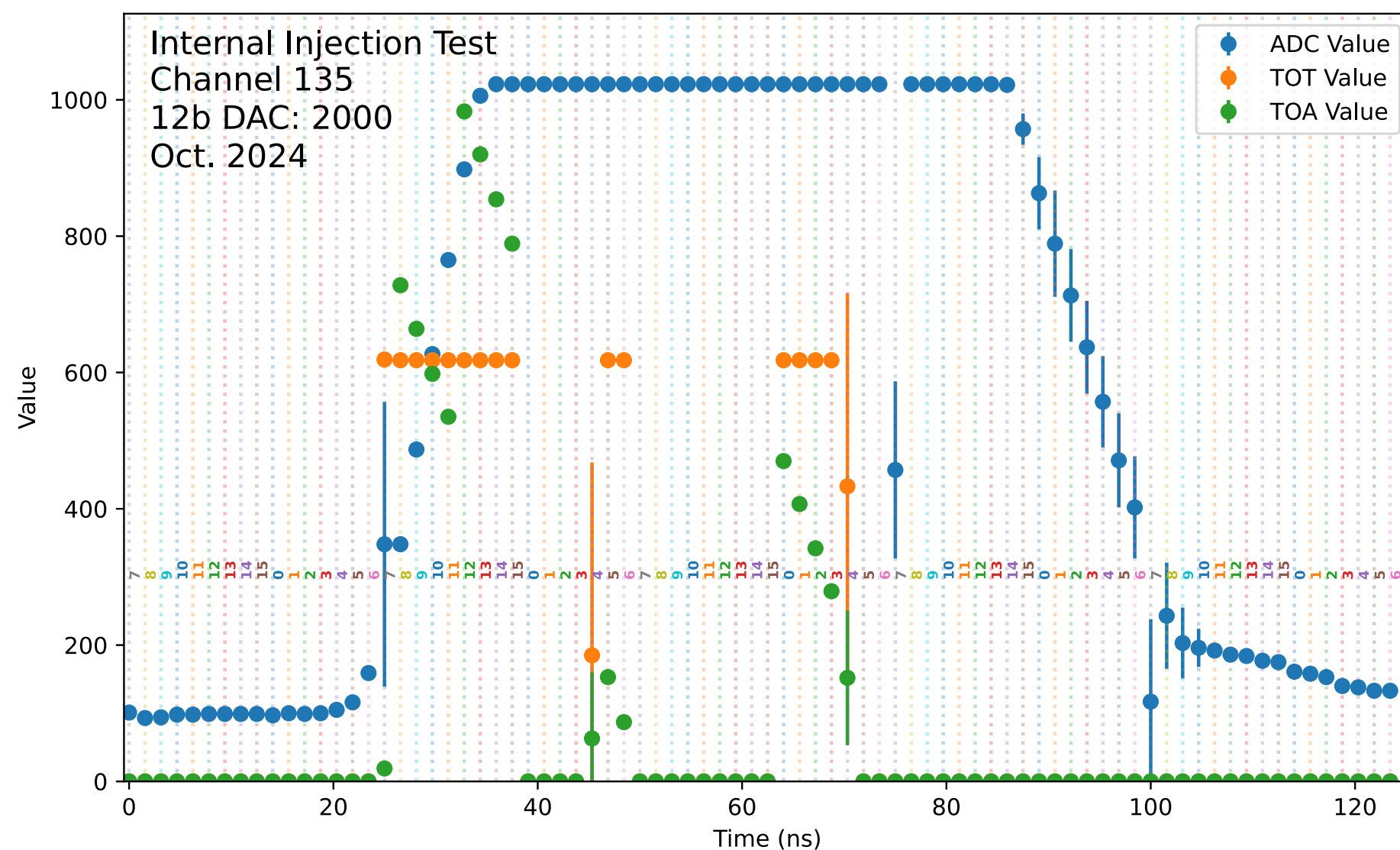
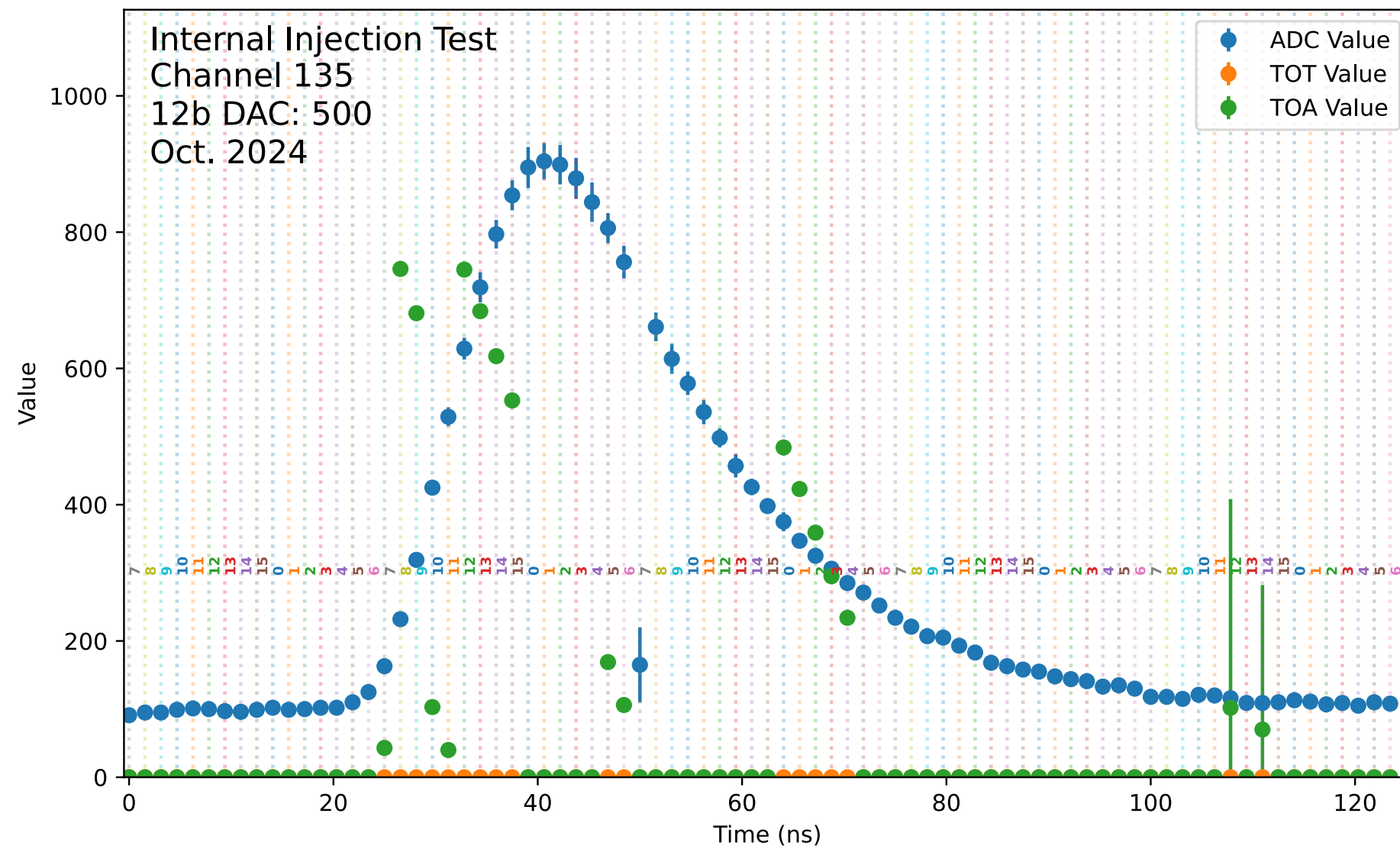
Switches for the summing

## LED calibration circuit:

- We saw a nice LED signal from the PWO4 tests
- Testing now with the BIC SiPM array and external function generator
- We rerouted the SiPM pulser from the H2GCROC to the FPGA



# Internal injection and TOA

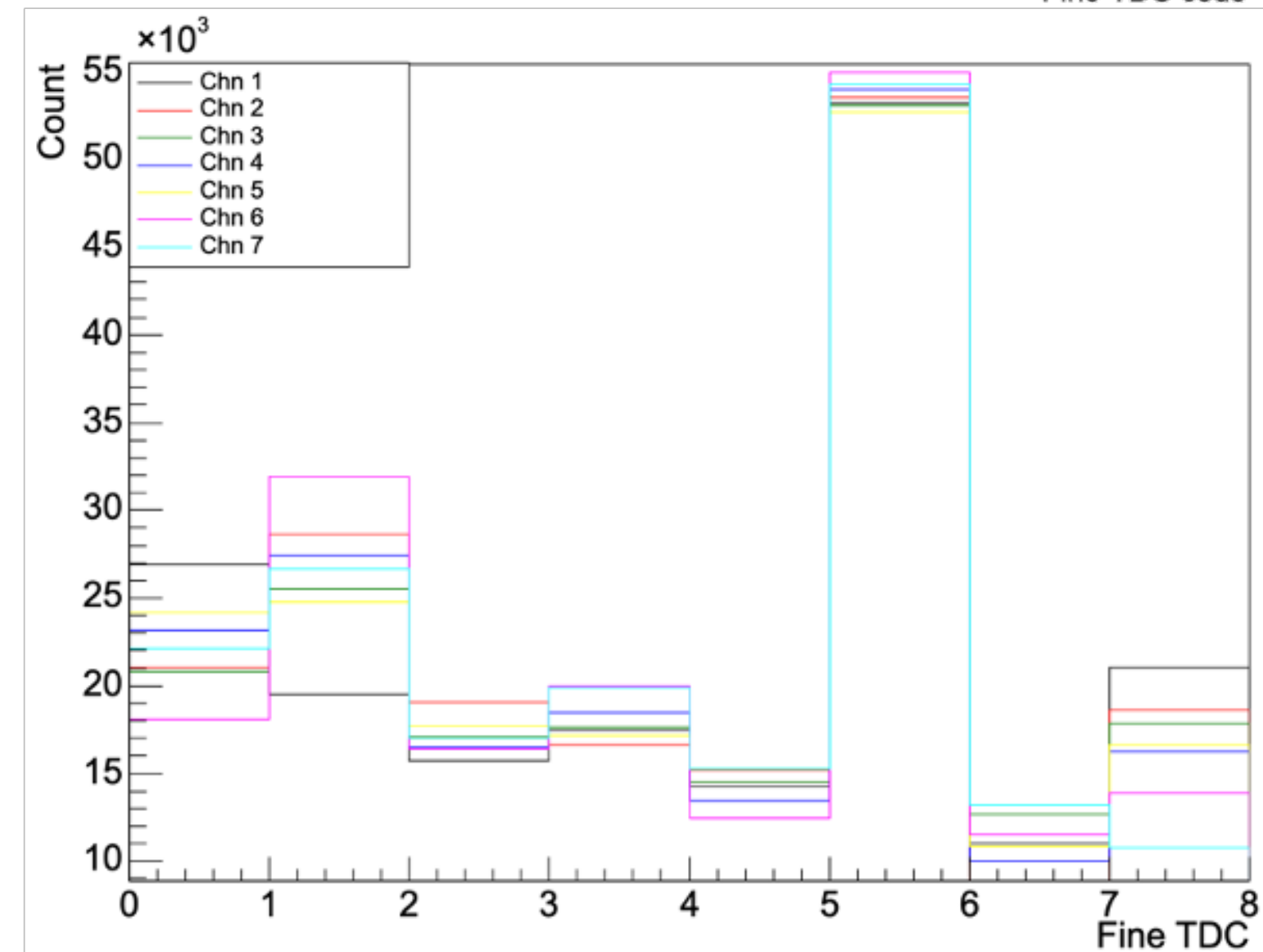
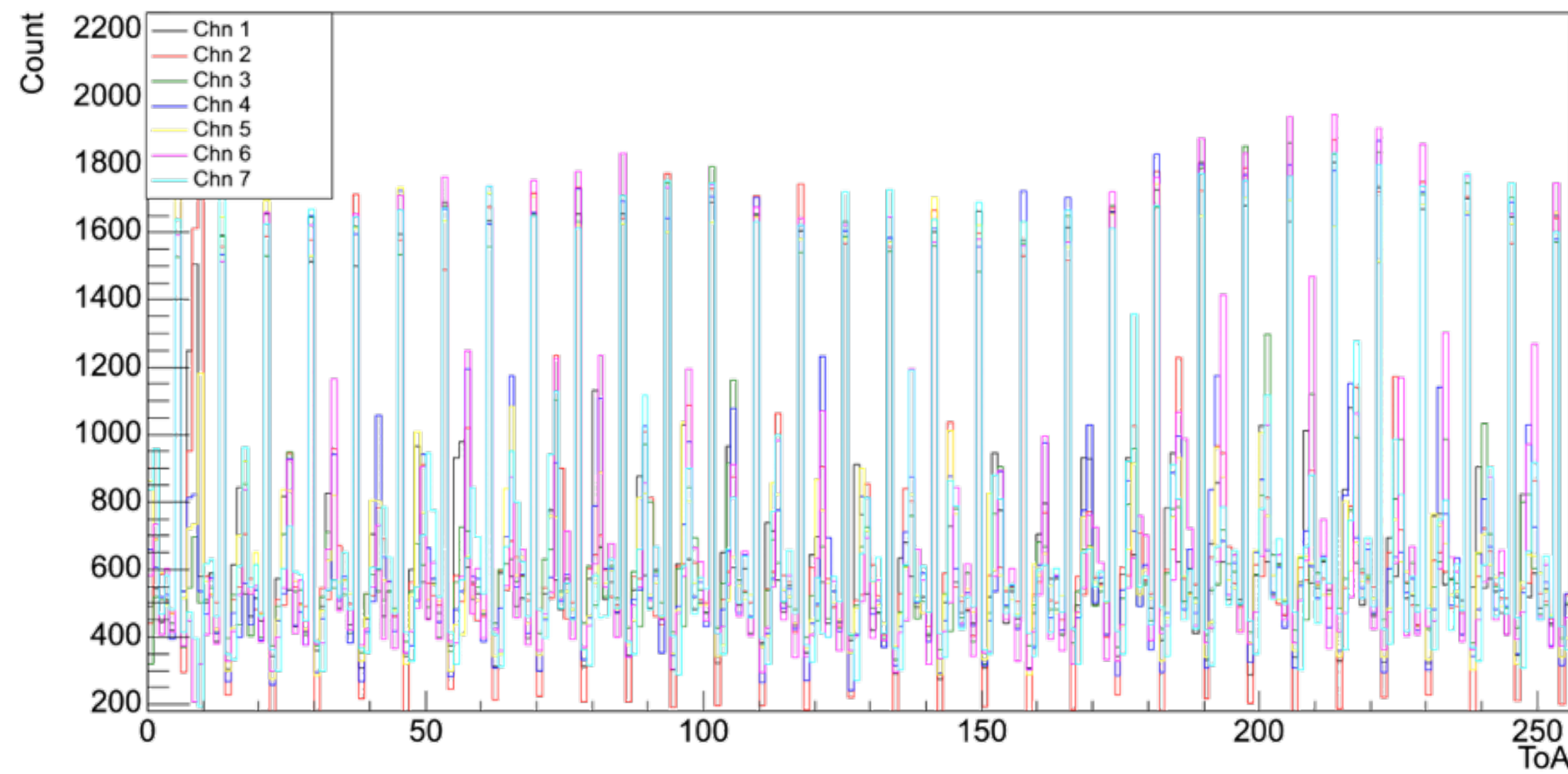
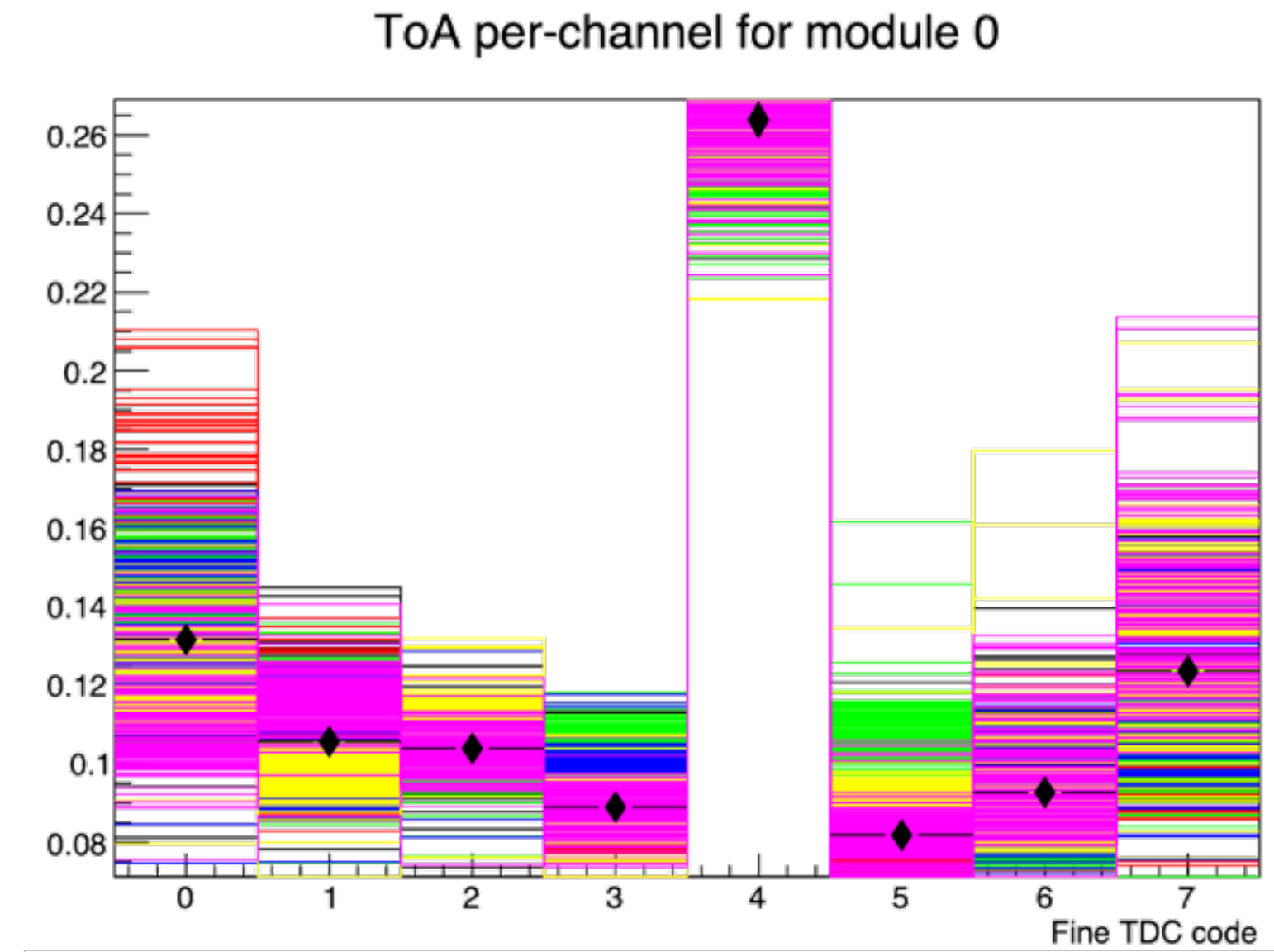
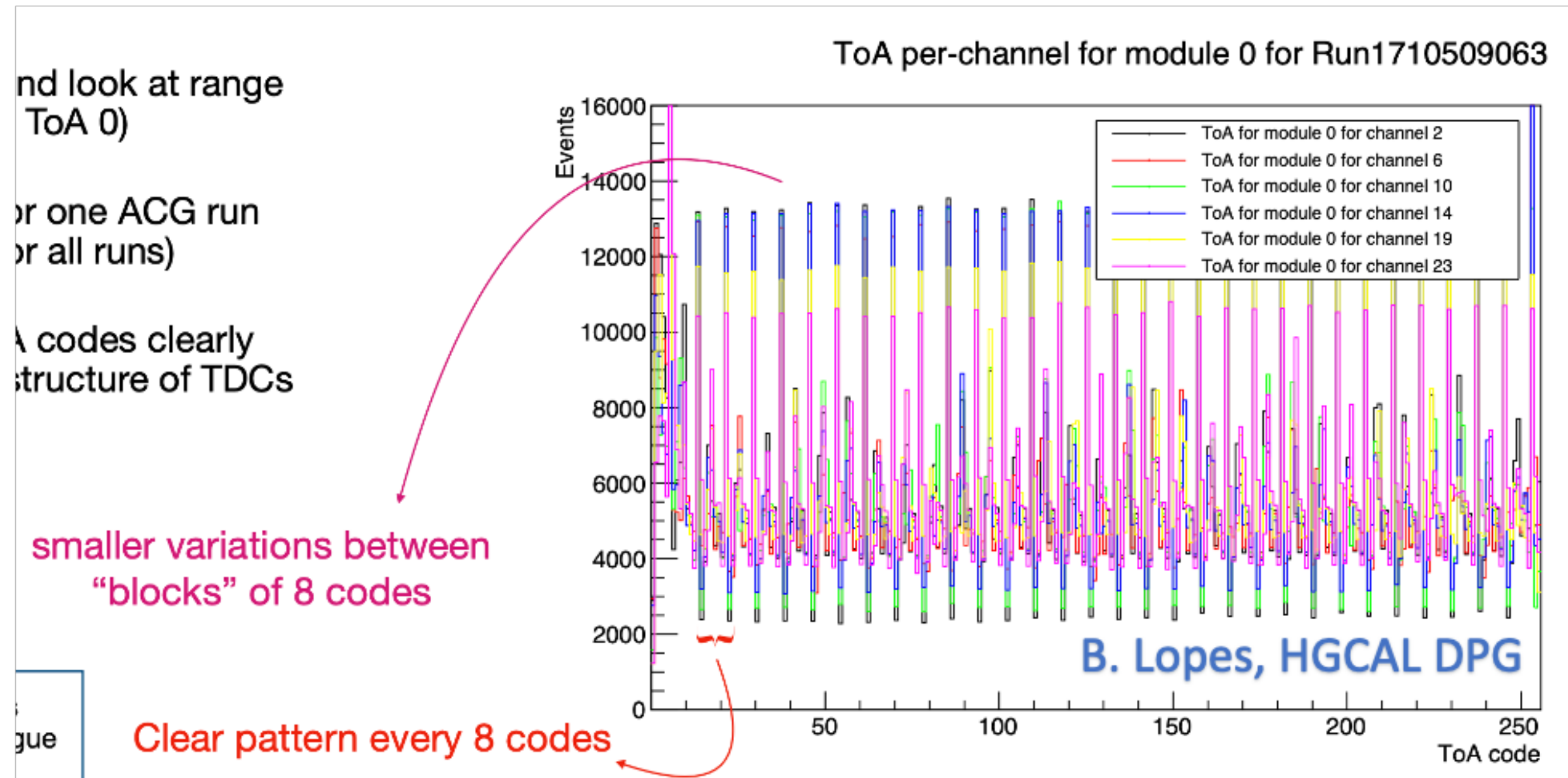


It appears for clock phases 0,1,2,3,4, the ToA and ToT values will shift by one bunch crossing

- Structure stems from each TDC being composed of 3 stages:
  - ◆ 2-bit grey counter LSB  $\approx 6.25$  ns
  - ◆ Coarse 5-bit TDC LSB  $\approx 200$  ps
  - ◆ Fine 3-bit TDC LSB  $\approx 25$  ps



# ToA calibration - fine TDC



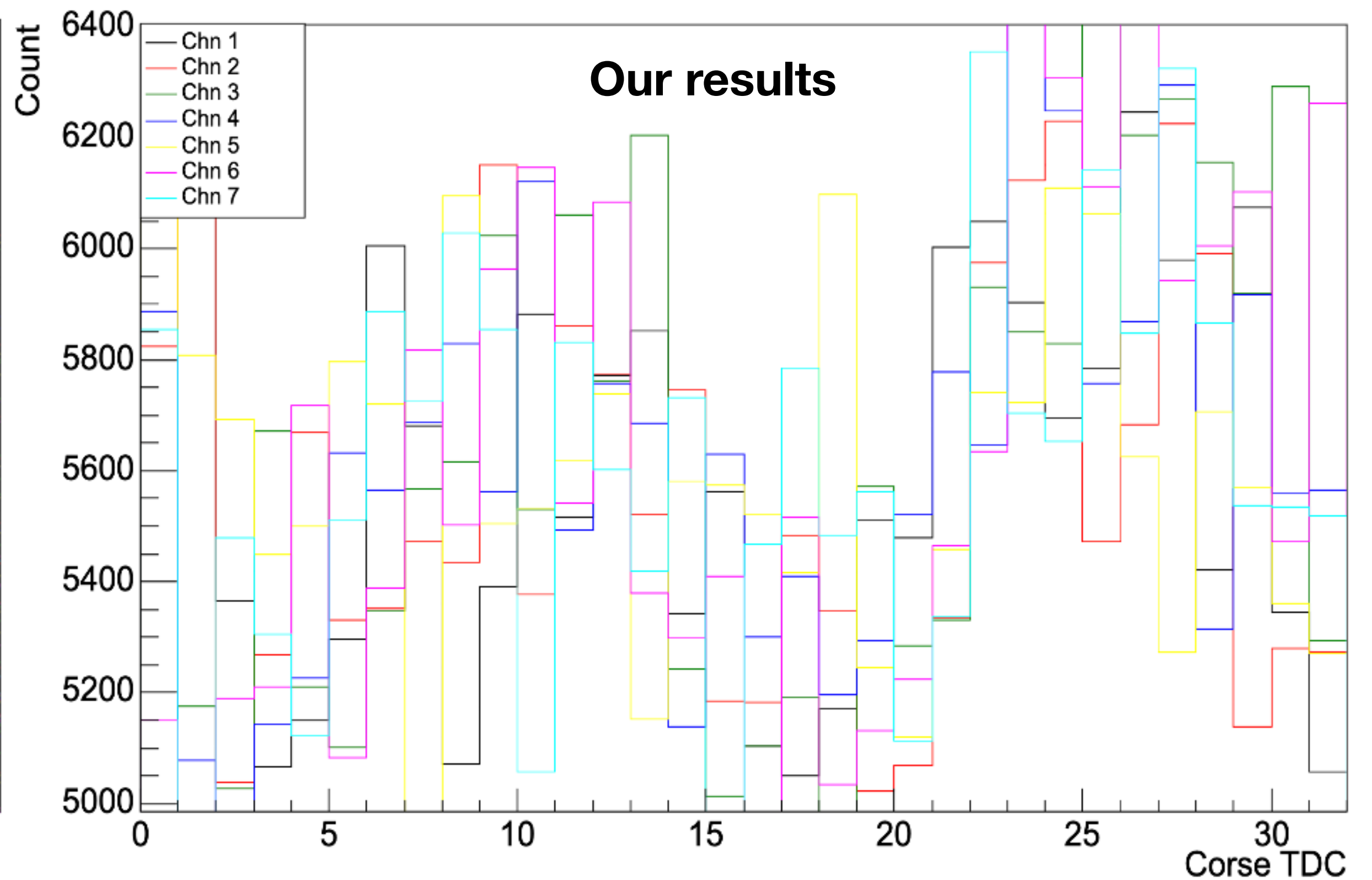
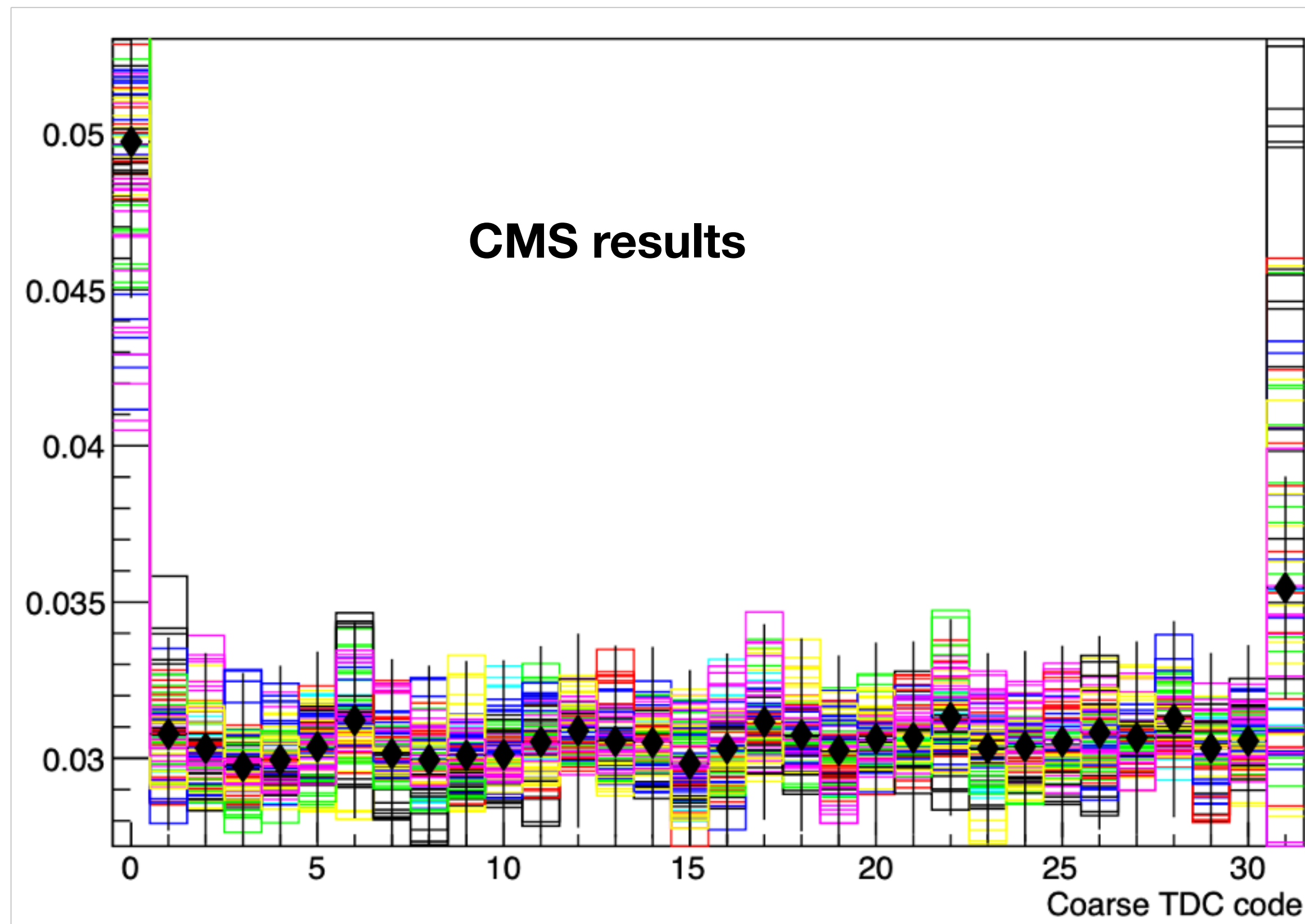
# ToA calibration - coarse TDC

Ideal fine TDC coverage:

000	001	010	011	100	101	110	111
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What it really looks like:

000	001	010	011	100	101	110	111
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*Thanks a lot for these studies from Shihai Jia!*