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Status report of the eRD109 project on SALSA chip development

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EPIC DAQ/electronics WG meeting

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SALSA CHIP TARGET SPECIFICATIONS

Versatile front-end characteristics

- Dedicated to MPGD detectors and beyond
- 64 channels
- Large input capacitance range, optimized for 50-200 pF, reasonable gain up to 1nF
- Large range of peaking times: 50-500 ns
- Large choice of gain ranges: 0-50, 0-250, 0-500 fC or 0-5 pC
- Large range of input rates, up to 100 kHz/ch with fast CSA reset (limit assumed for EPIC: 25 kHz/ch)
- Reversible polarity
- Front-end elements can be by-passed

Digital stage

- Fast sampling ADC for each channel on 12 bits (> 10 effective bits) at up to 50 MS/s
- Possibility under study to double rates by coupling pairs of channels
- Integrated DSP for internal data processing and size reduction, treatment processes to be selected according to user needs
- Continuous readout compatible with streaming DAQ foreseen at EIC, triggered mode also available
- Several 1 Gb/s output data links

General characteristics

- ~1 cm² die size, implemented on modern TSMC 65nm technology
- Low power consumption ~ 15 mW/channel at 1.2V
- Radiation hardened (SEU, TID)

LAST UPDATES ON SALSA PROTOTYPES

PRISME updates (PLL test chip)

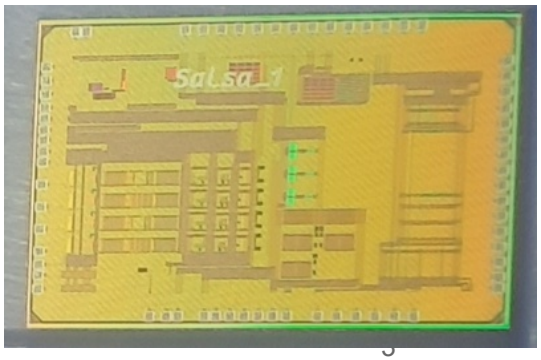
- Further tests on noise components, and on input frequency range (in case of lpGBT input)
- Several updates done on PLL and chip design
  - correction of large deterministic noise
  - improvements in case of lpGBT input frequency
  - inclusion of CDR inside PLL for clock detection and digital signal extraction from unified input signal combining clock, fast commands and slow-control input
- Submission of PRISMEb prototype based on new design December 11th

PRISME radiation tests

- TID radiation tests November 18-22 at CERN
- Preparation of radiation tests ongoing
- Caps removed from packages to allow direct radiation exposure of the chips
- SEU radiation tests beginning of 2025 at Sao Paulo

SALSA1 prototypes (front-end + ADC chip)

- Naked dies received beginning of October
- Packaging done, encapsulated chips received at Saclay
- Delays on test-boards due to some problems with the layout design, finally resolved
- PCB production ongoing, components ordered
- Test-boards available around end of November



LAST UPDATES ON SALSA PROTOTYPES

- **SALSA2** (fully featured prototype on up to 32 channels)
  - Main DSP modules and associated algorithms mostly defined, study still ongoing for peak finding and feature extraction algorithms
  - Work ongoing on HDL code of DSP modules
  - Updates done on the input interface definition to adapt it to lpGBT, in case it is selected for MPGD front-end boards; integration of the new PLL block version
  - Progresses on specification document describing DSP architecture and modules: 1st version of data format, selection of ADC samples to be recorded, generation of calibration data
  - Still a lot of development work ahead !

PROJECT MILESTONES AND NEXT STEPS

eRD109 FY23 project milestones

- Specifications of SALSA1 design → done
- Production of SALSA1 prototypes → done, packaged chips delivered to Saclay
- Test card production → in progress
- Performance evaluation → expected end of 2024 / beginning of 2025

Milestones of generic R&D program for EIC project (new 65nm PLL block)

- PRISME prototype submission → done July 19th 2023
- Packaging and test card production → done February 2024
- Radiation tests → November 2024

eRD109 FY24 project milestones

- SALSA2 specifications → July 2024, details in progress
- SALSA2 submission → March 2025
- Beginning of SALSA2 tests → September 2025

Very next steps

- Beginning of SALSA1 tests → December 2024
- Radiation tests on PRISME prototypes → TID tests in November
- Submission of new PRISMEb chip → December 2024
- SALSA2 HDL code → in progress