ppRDO eRD109 Status
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ppRDO Short Status

- Most parts of the Project are complete
  - ppRDO board itself
  - ETROC measurements (Zhenyu et al)
- Current efforts
  - precise jitter and clock stability measurements using on-board clock generators
    - Tim Camarda et al, BNL ⇒ almost complete
    - we would like to establish & characterize clock jitter using the specific on-board PLLs to possibly help other designs
- Future efforts
  - precise jitter measurements and clock characterization using the recovered clock from the fiber with the TCLink protocols
    - need a FELIX-equivalent and engineering
      - both are outside this eRD109 funding request so TBD
      - Note that due to the use of lpGBT this effort is under consideration
        - not needed for TOF and other high-precision AC-LGAD detectors
  - use of ppRDO to evaluate ASICs
    - waiting for EICROC1, possibly CALOROC as a similar ASIC to EICROC2