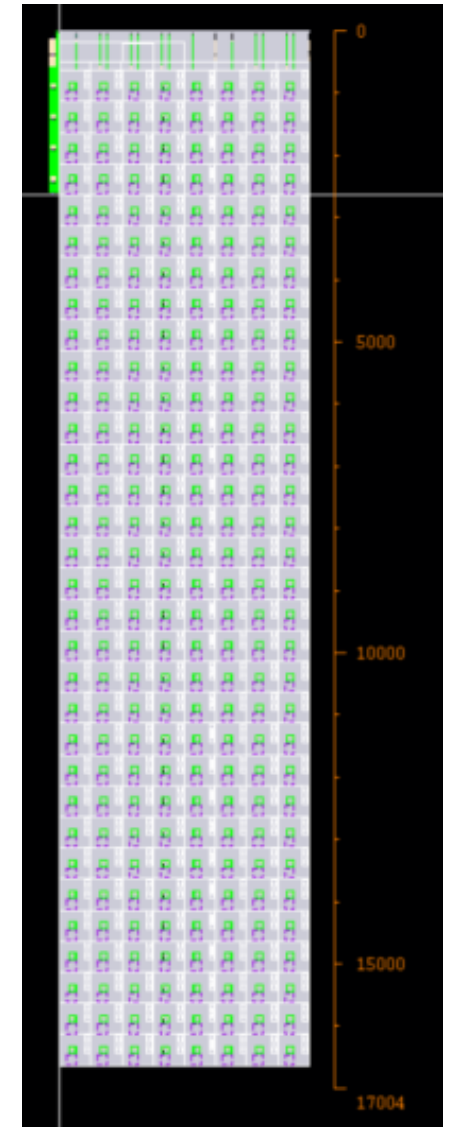


EICROC status and plans
eRD109 monthly meeting
7 nov 2024

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- EICROC1 : $8 \times 32 = 256$ pixels or $32 \times 32 = 1024$
 - Layout complete for 8×32 . DRC/LVS OK
 - Still EICROC0 digital architecture and Readout
 - 2/8 data outputs : 1 for 128 pixels (4×32)
 - Looking to increase R/O speed. Possibility to skip pixels by slow control
 - Looking to improve testability.
 - Verifications in progress (~2 months)
 - 32×32 would likely have 3-4 different flavours of 8×32
- EICROC1 addresses floorplan issues
 - Power drops along column, threshold uniformity
 - TDC uniformity and dependance on number of channels triggering
- Variants of EICROC0 will also be submitted
 - Lower power in the ADC branch ($100 \mu\text{W}$)



Chip	date	Techno	size	Analog	Digital	goal
EICROC0	Jun 2023	130n	4x4	Conservative	Simple	Study sensor
EICROC0A/B	beg 2025	130n	4x4	Low power	same	Study analog
EICROC1	beg 2025	130n	32x32	Conservative	Same	Study power distribution
EICROC0_65n	end 2025	65n	4x4	final	Simple	Study analog in 65n
EICROC2	End 2026	?	32x32	Low power	Final	First final prototype

Chip	date	Techno	size	Analog	Digital	goal
CALOROC1A	beg 2025	130n	36ch	Conservative	Final	Study sensor
CALOROC1B	beg 2025	130n	36ch	Low noise	final	Study analog
CALOROC2	End 2026	130n	36/72	final	final	First final prototype

- TSMC now requires to fully populate the reticle of 24x32
 - Cost ~300 k€
- For EIC we would have
 - EICROC1
 - 2 or 3 EICROC0/A/B
 - 2 CALOROC1A/1B
 - ~60% of reticle area
- Possible additionnal partners
 - ~20% of reticle area
 - Still space available (if ready in time !)

