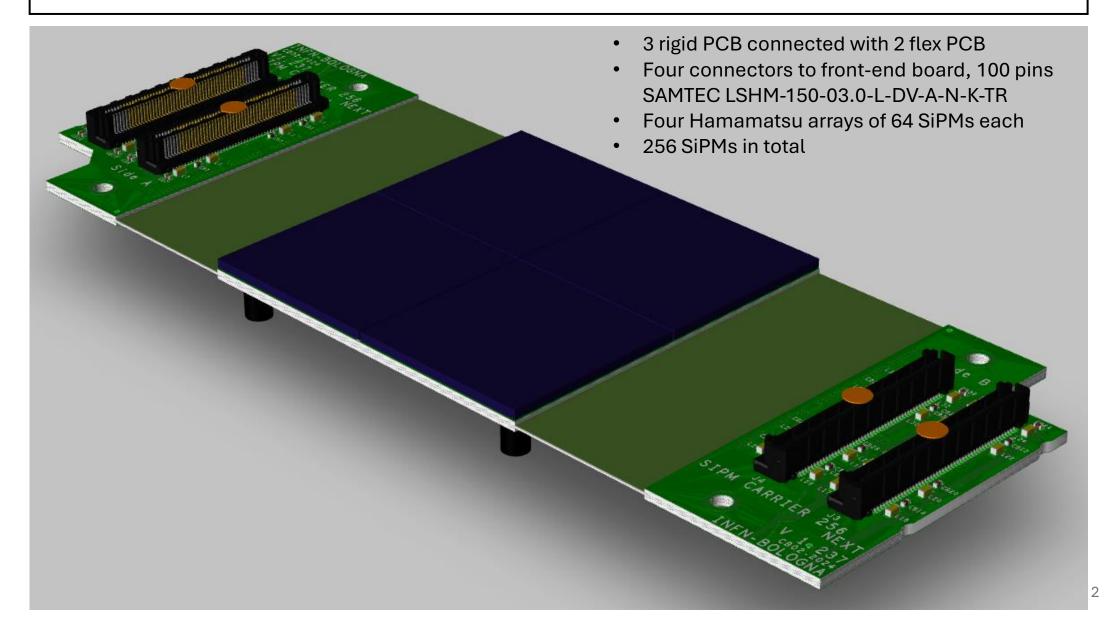
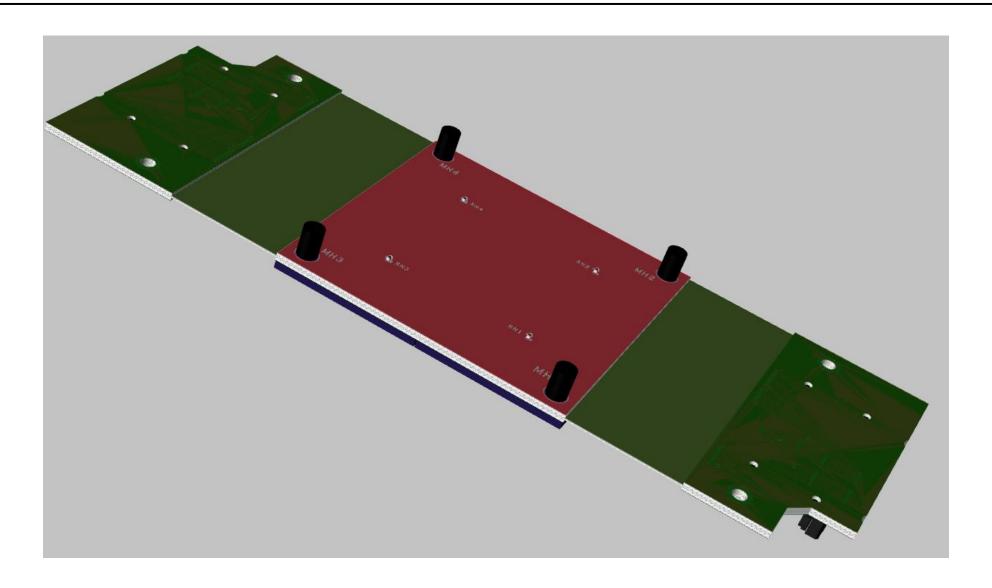


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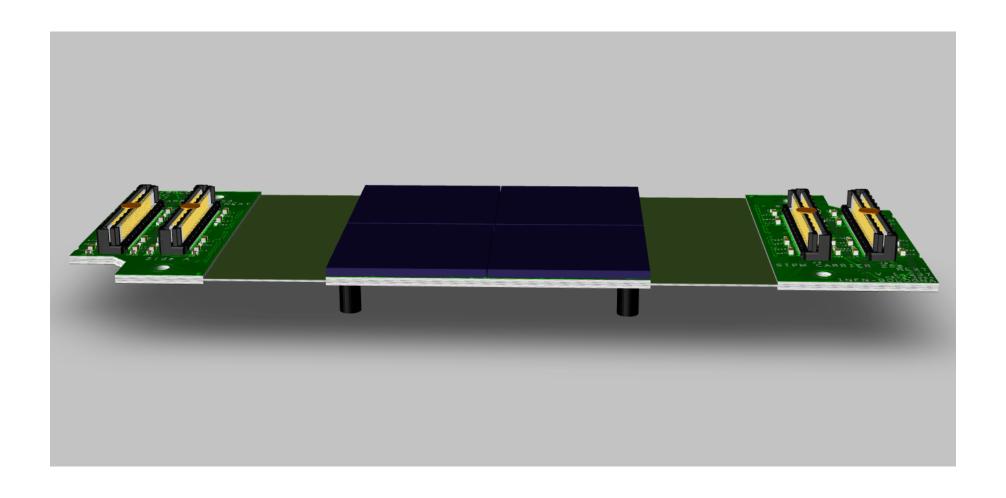




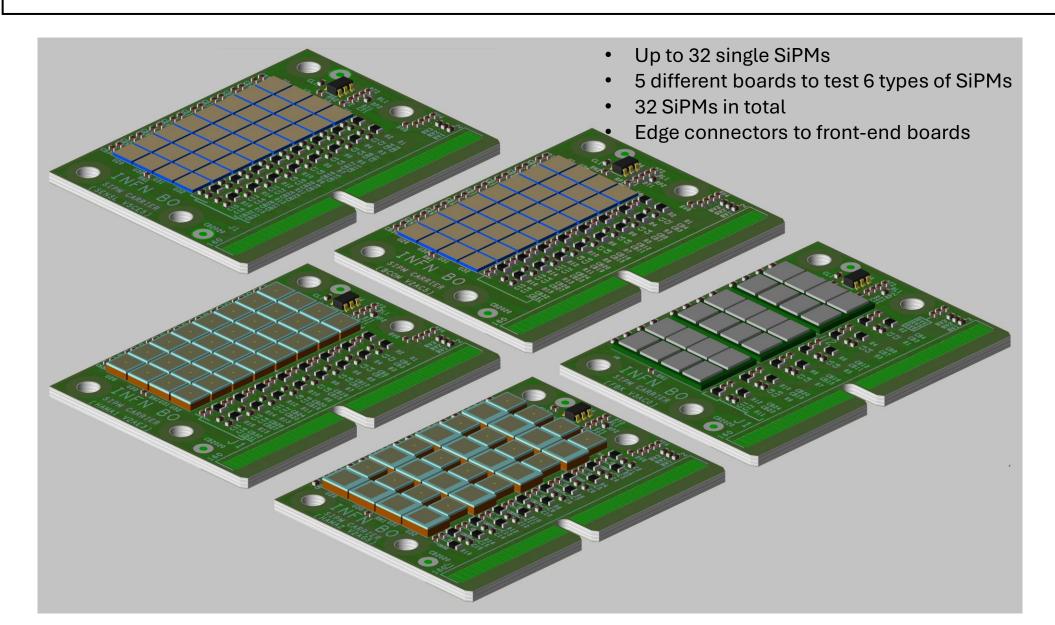




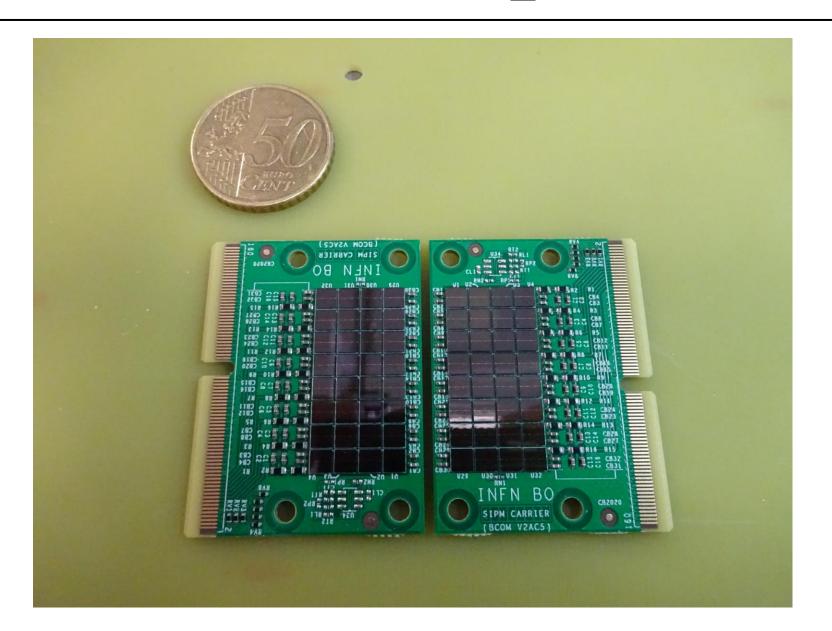




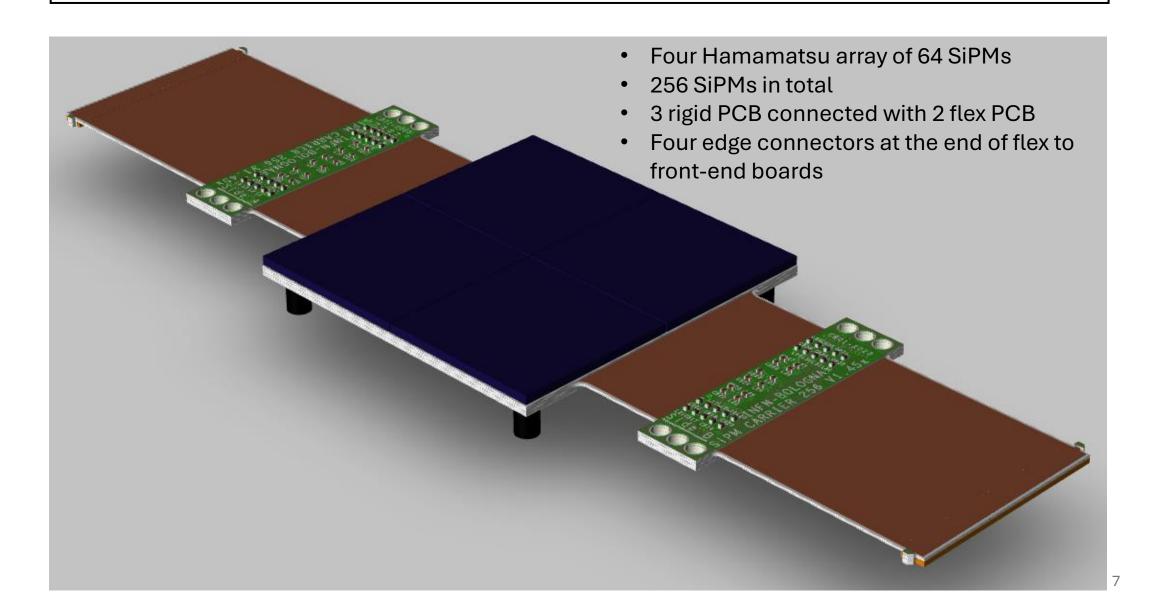




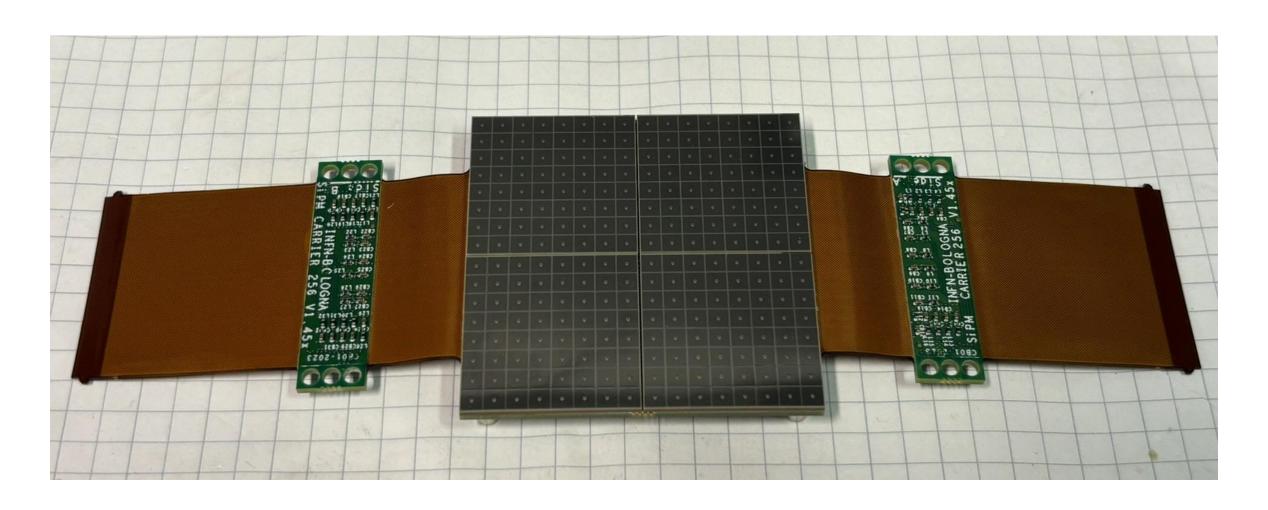






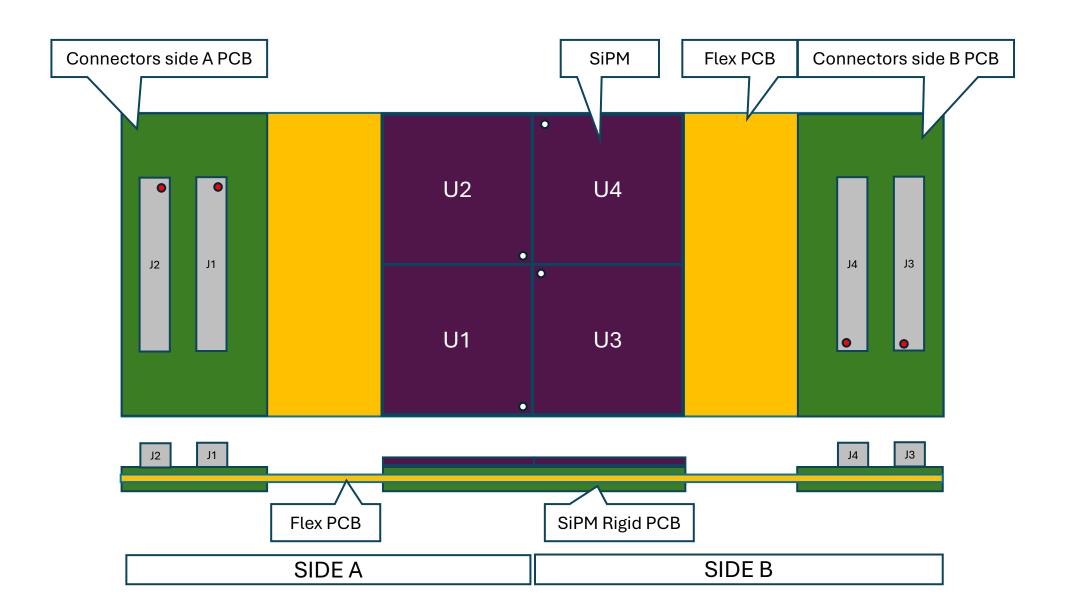






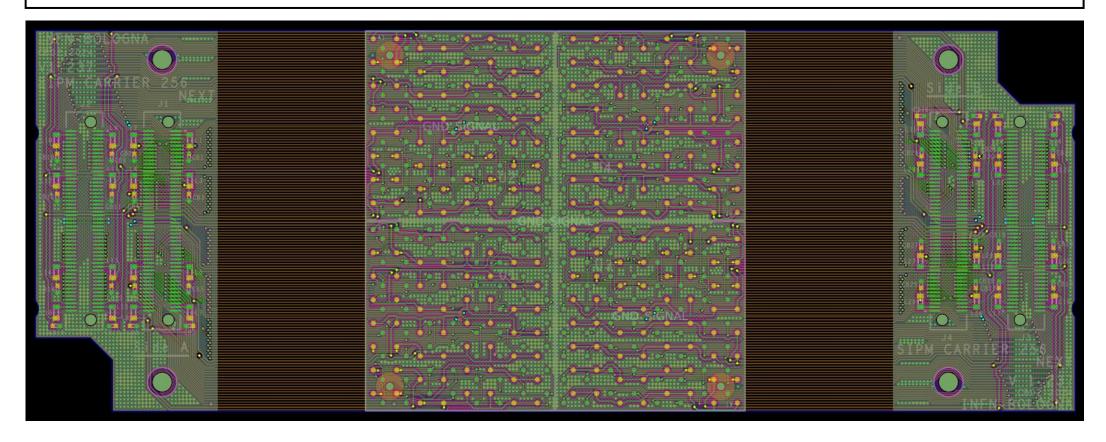


Carrier V3: Main components and PCB





PCB



- Dimensions: 142x52mm (5.59x2 inch)
- Three rigid PCBs connected together by two flex PCBs
- Rigid PCBs: 9 layers, minimum track width 0.127mm (5mils), minimum hole 0.15mm (5.9mils), minimum spacing 0.12mm (4.7mils), normal and blind vias
- Flex PCB: 3 layers, minimum track width 0.127mm (5mils), minimum spacing 0.12mm (4.7mils), no vias



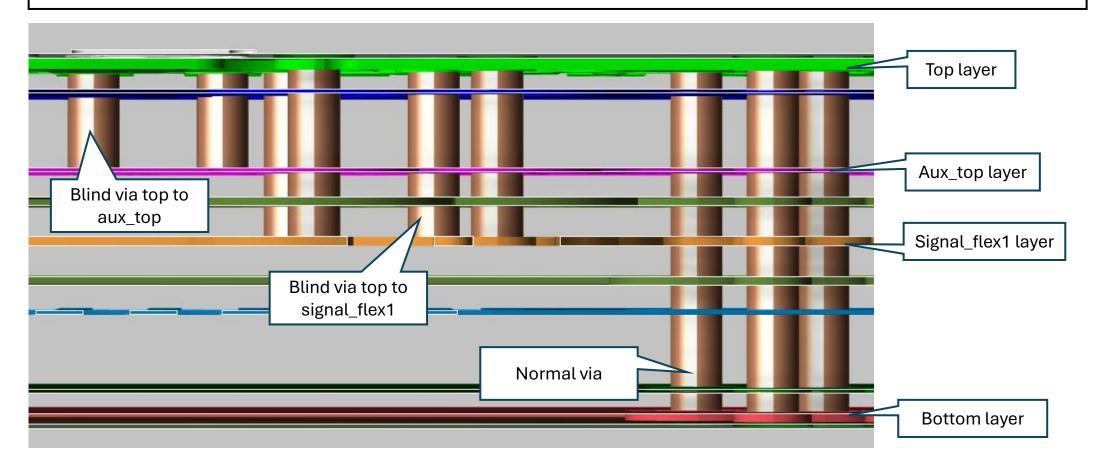
PCB: Stackup

Objects		Types	Thislenge				
	Name	Layer	Thickness	Material	Primary	Flex	Add Stackup
#			mm				
*	*	*	*	*	*	*	*
		Surface			✓	✓	
	SOLDERMASK_TOP	Mask	0.02	Soldermask	✓		
1	тор	Conductor	0.042	Copper	✓		
		Dielectric	0.08	Fr-4 No Flow Pre	✓		
2	GND_TOP	Plane	0.017	Copper	√		
		Dielectric	0.3	Fr-4	√		
3	AUX_TOP	Conductor	0.017	Copper	√		
		Dielectric	0.1	Fr-4 No Flow Pre	\checkmark		
	COVERLAY_TOP	Mask	0.04	Polyimide		✓	
4	GND_FLEX_EXT	Plane	0.035	Copper	\checkmark	✓	
		Dielectric	0.125	Polyimide Film	✓	\checkmark	
5	SIGNAL_FLEX1	Conductor	0.035	Copper	✓	✓	
		Dielectric	0.125	Polyimide Film	✓	\checkmark	
6	GND_FLEX_INT	Plane	0.035	Copper	\checkmark	\checkmark	
	COVERLAY_BOTTOM	Mask	0.04	Polyimide		✓	
		Dielectric	0.1	Fr-4 No Flow Pre	\checkmark		
7	AUX_BOTTOM	Conductor	0.017	Copper	✓		
		Dielectric	0.3	Fr-4	\checkmark		
8	GND_BOTTOM	Plane	0.017	Copper	✓		
		Dielectric	0.08	Fr-4 No Flow Pre	✓		
9	воттом	Conductor	0.042	Copper	✓		
	SOLDERMASK_BOTTOM	Mask	0.02	Soldermask	✓		
		Surface			✓	✓	

- 9 layers in total
- 5 layers for signals including one in the flex PCB
- 4 ground planes including two in the flex
- On the Flex PCB the signal layer is inserted between two ground plane layers
- The bottom layer of the central rigid PCB, in direct contact with the cooling plane, is not equipped with a solder mask to improve the thermal transmission.
- Blind vias have been used in this project to improve the tracks routing.
- The PCB core are currently between layer 2 and 3 and symmetrically 7 and 8
- Track impedence is 50Ω



PCB: vias

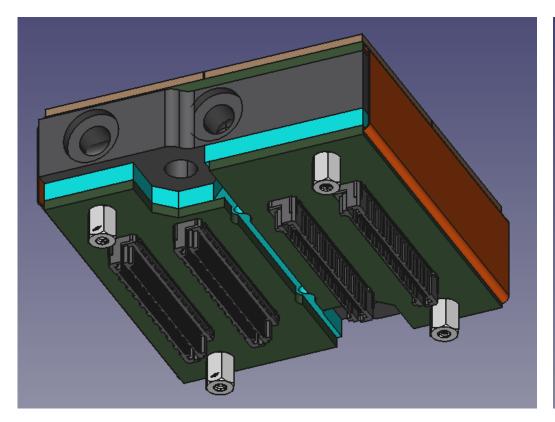


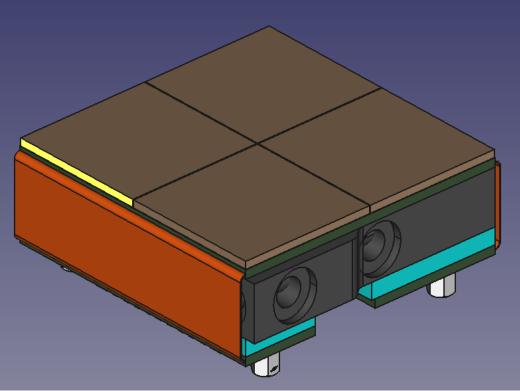
Three types of vias have been used for the routing:

- One from the top layer to the aux_top layer, the first internal conductors layer
- The second from the top layer to the signal_flex1 layer through the aux_top layer
- The third type are normal vias, for connection between the top layer and the bottom aux layer or the bottom layer, and for the ground plane connections.



PCB folding





- PCB folding around the cooling plate
- Cut-out for the cooling pipes

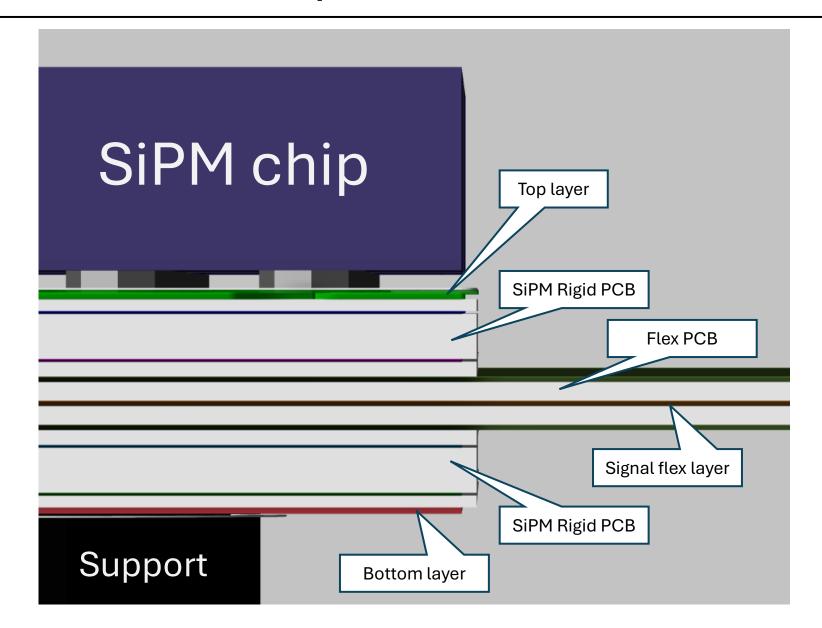


Conclusions

- The board schematic is complete
- The PCB layout is complete
- An offer has been requested from the PCB manufacturer for 8 boards
- Feedback was requested from the PCB manufacturer about the available materials, including the electrical and mechanical characteristics of:
 - Dielectrics (thickness, electrical permittivity ε_r)
 - The copper planes on FR4 associated with the cores (also thickness, electrical permittivity ε_r of the FR4 part)
 - Polymide sheets for the flex part (thickness, electrical permittivity ϵ_r) Once these parameters have been obtained, the stackup will then be checked and in case of changes, the new files will be sent for production

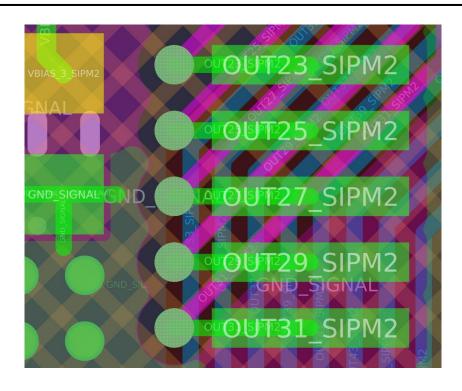


Backup: PCB stack



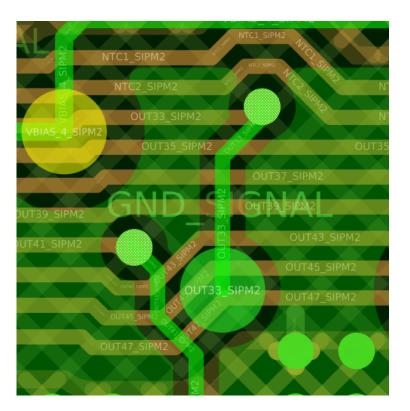


Backup PCB: blind via



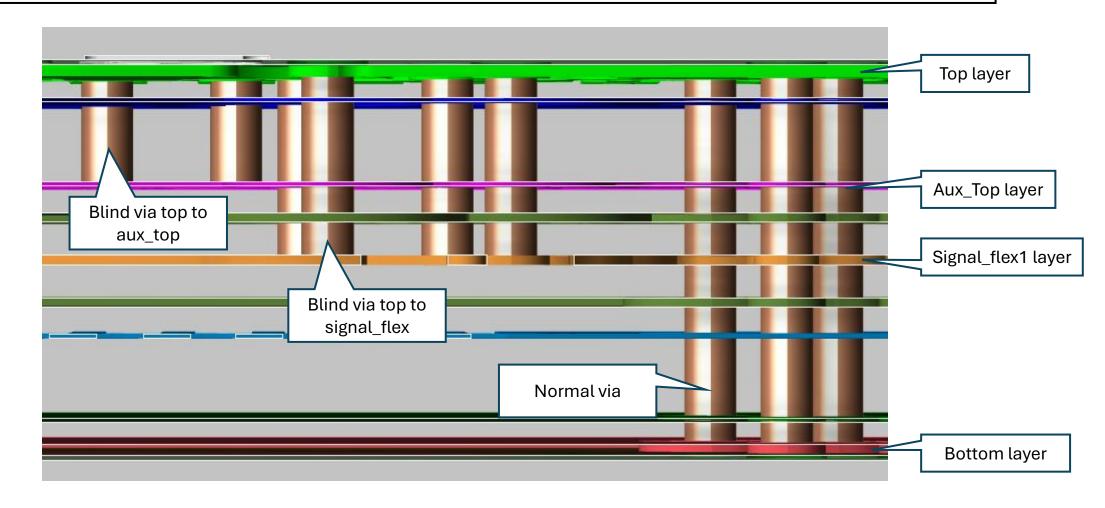
Two tipes of blind via has been used:

- One from the top layer to the aux_top layer, the firts internal conductor layer (left image)
- The second from the top layer to the signal_flex1 layer through the aux_top layer (bottom image)



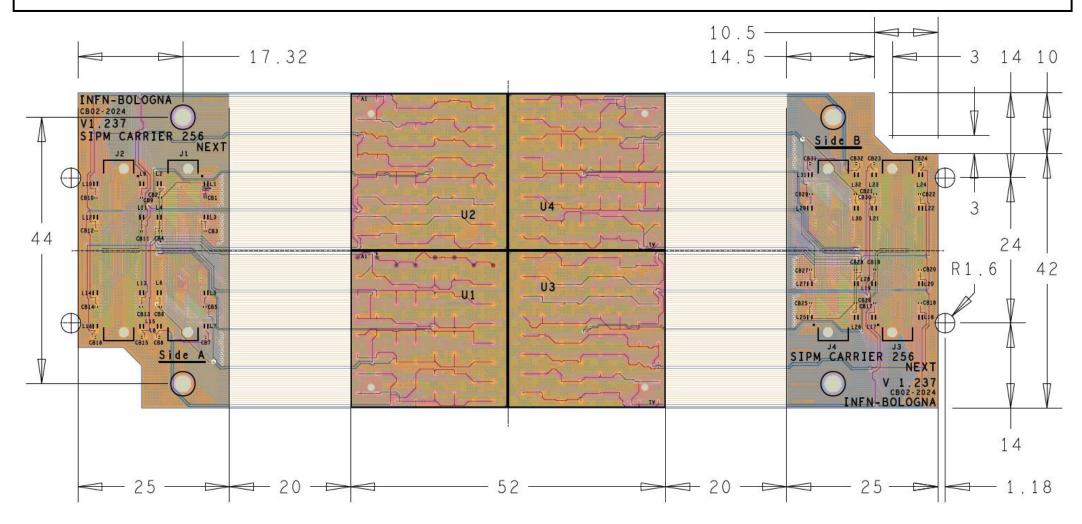


Backup: vias and blind vias



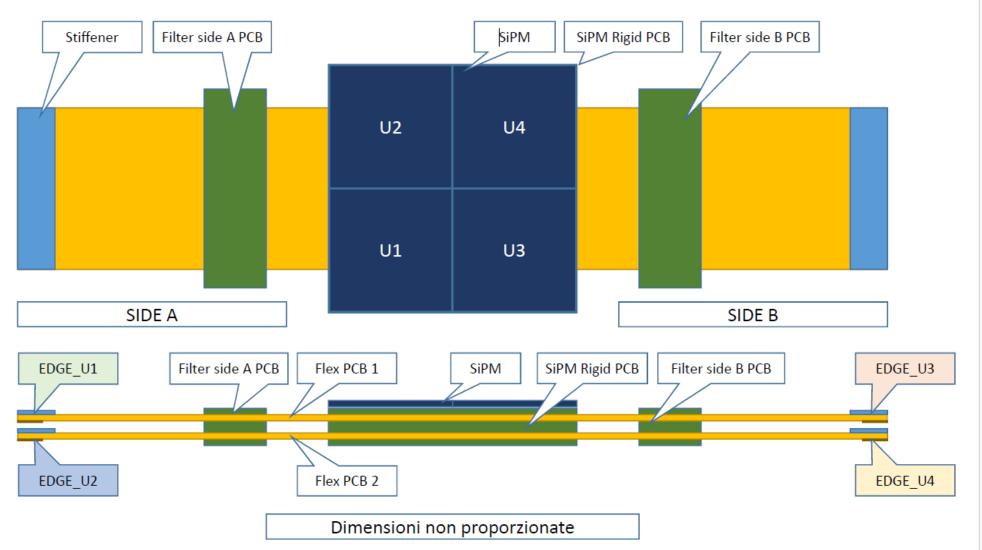


Backup: PCB





Backup: SIPM_CARRIER_V2





Backup: SIPM_CARRIER_V2 Stack Up

