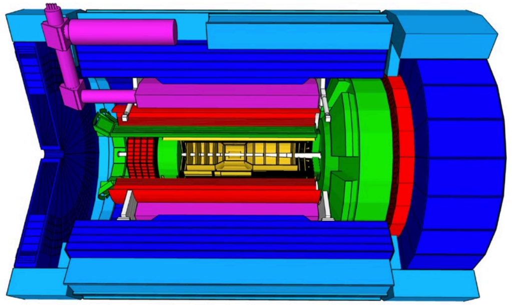
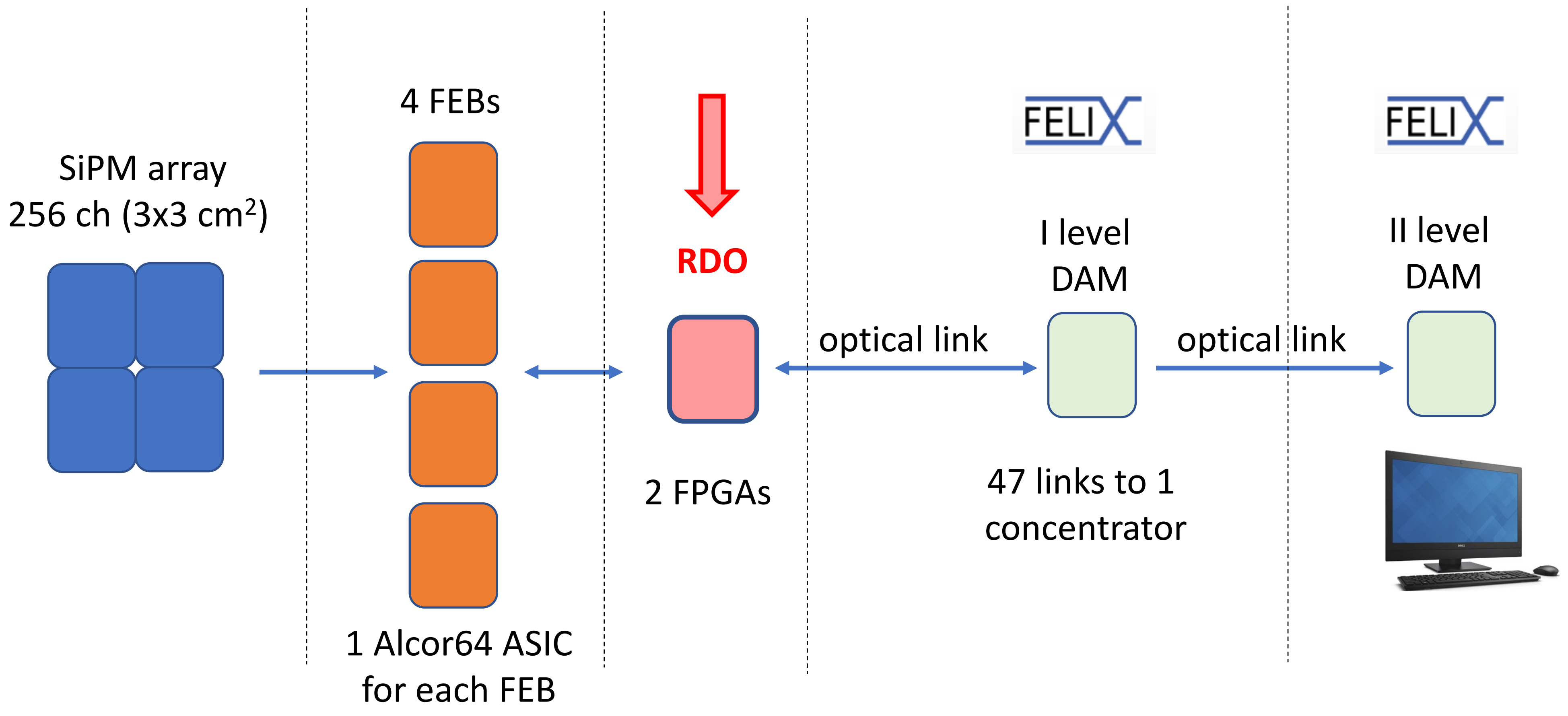


dRICH readout board: RDO

Davide Falchieri (INFN Bologna)
on behalf of the dRICH Collaboration

dRICH meeting - Electronics, 06 November 2024

Readout concept



The RDO board has to:

- receive and distribute the common clock (394 MHz) to the FEBs
- manage the readout of 4 Alcor64 (64 channels each)
- send data towards the ePIC DAQ

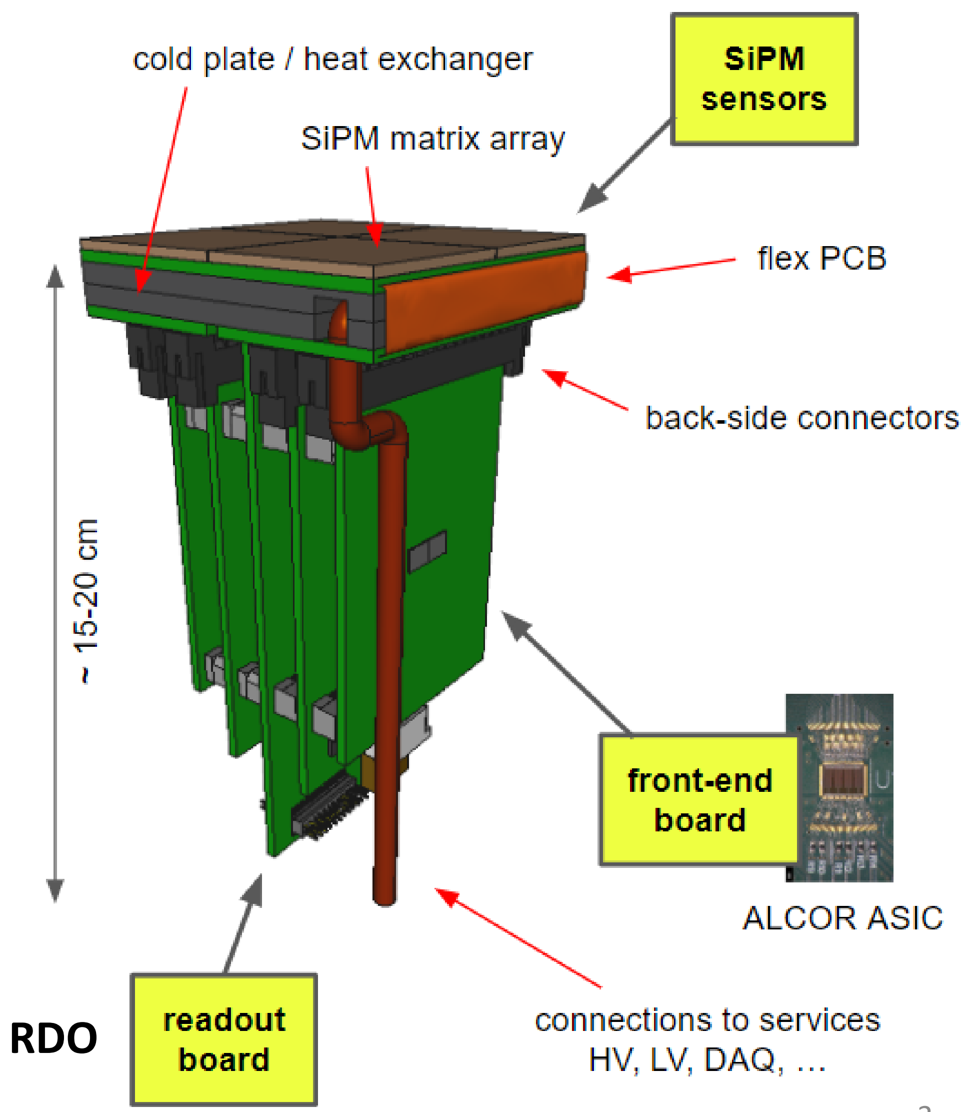
dRICH RDO overview

RDO is as a component of the dRICH PDU

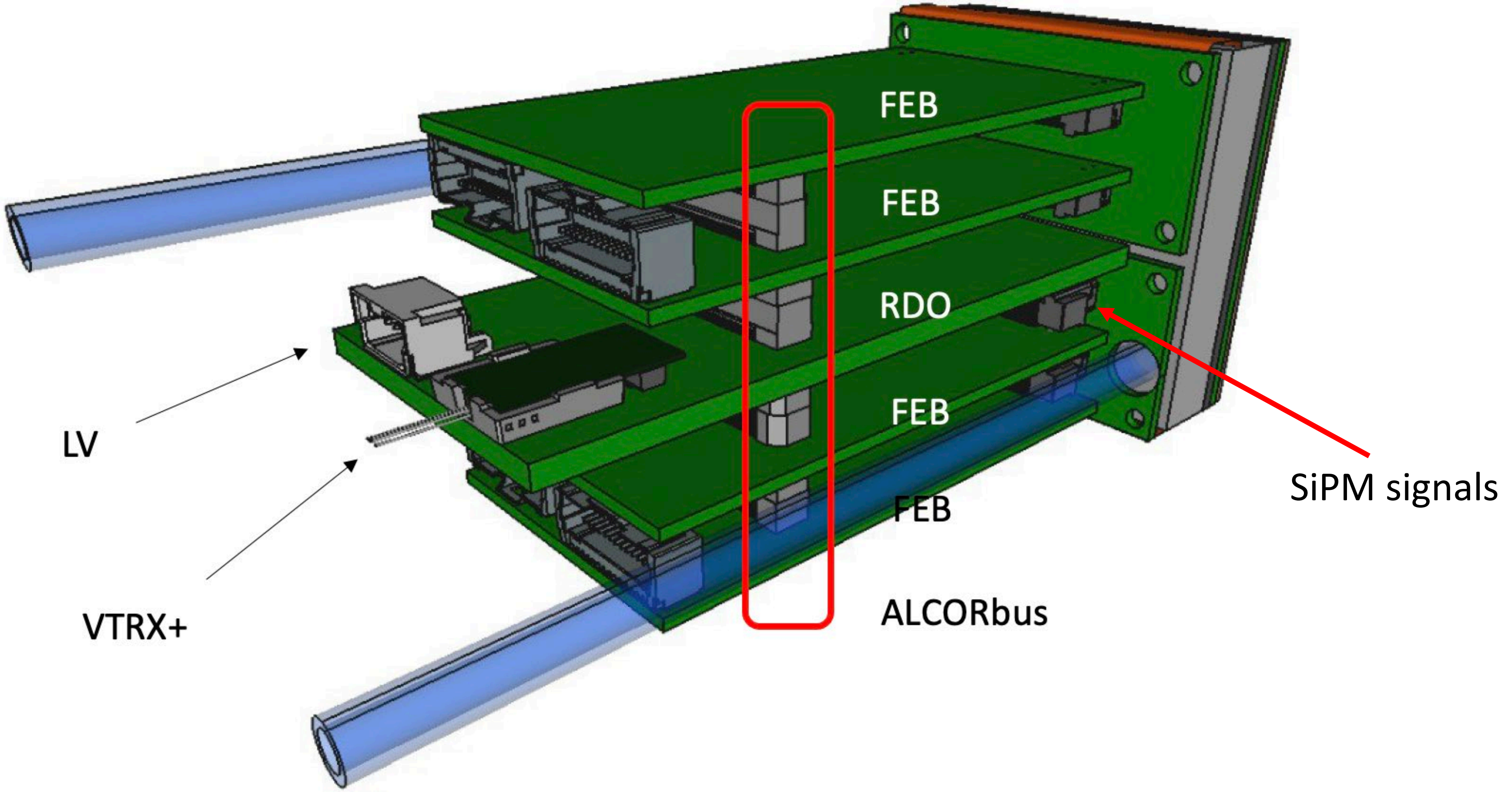
basic RDO specs:

- provides interface to ePIC DAQ
- provides readout/config to 4 Alcor64 (or 8 Alcor32)
- 1 optical link (TX/RX)
- services (temperature sensors, current monitor, …)
- **4 x 9 cm^2 surface available**

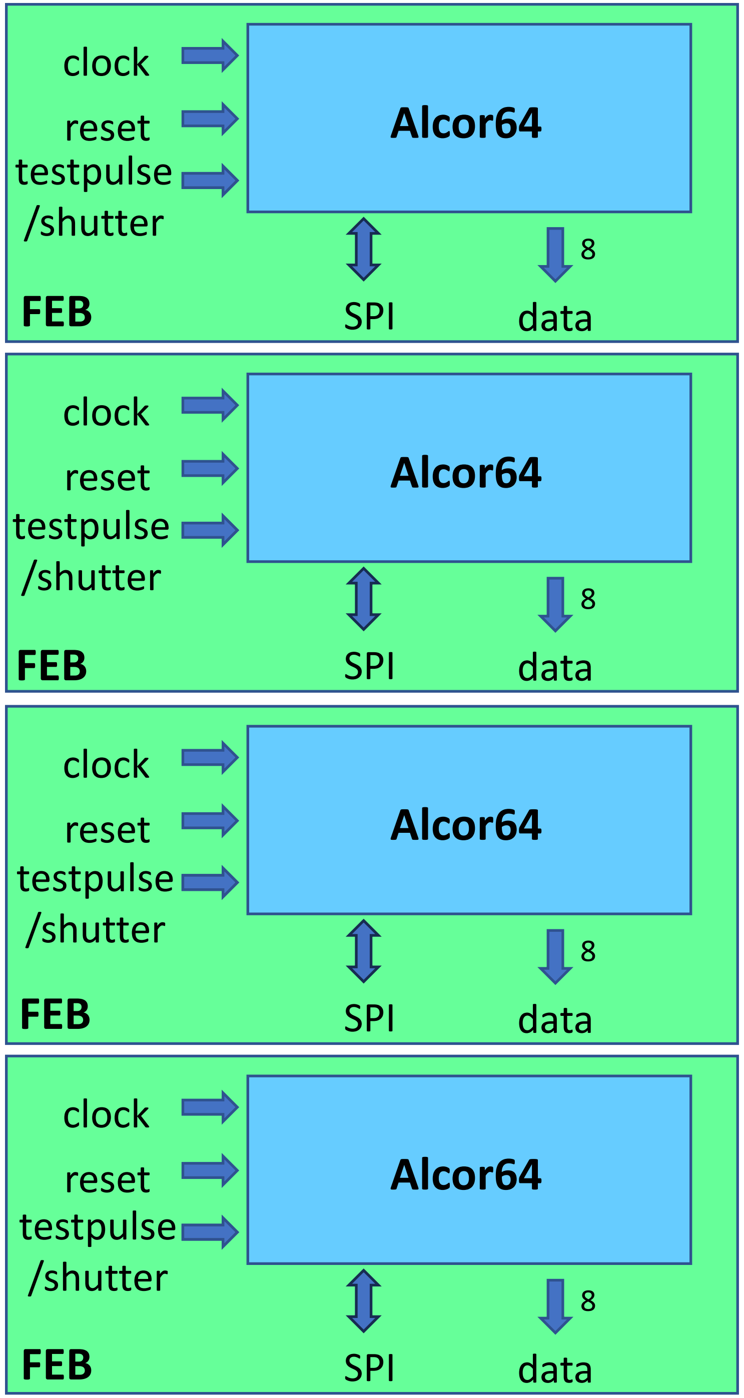
conceptual design of PDU layout

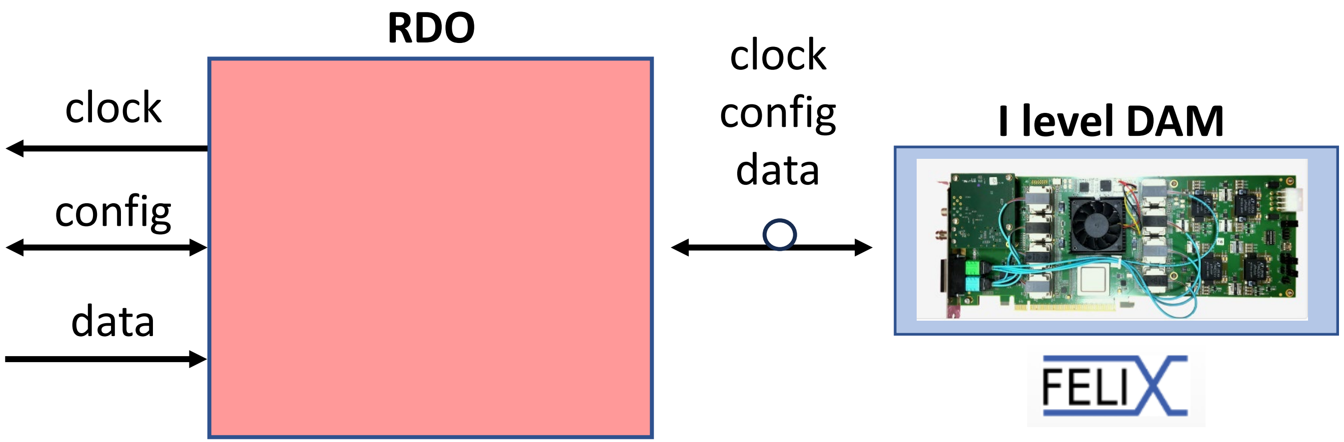


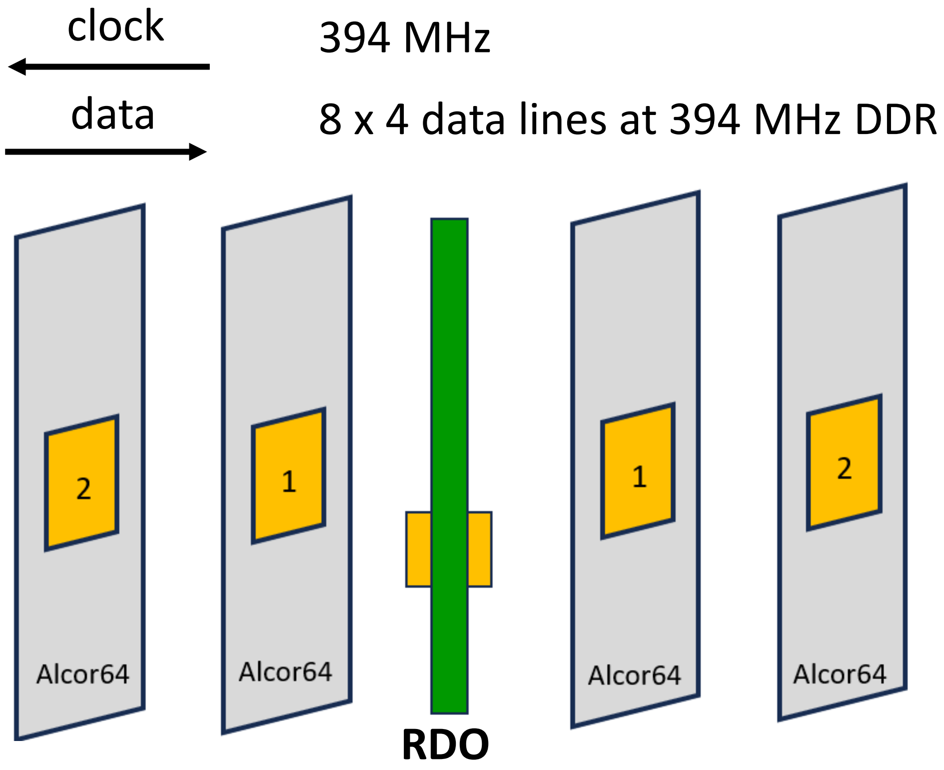
dRICH RDO overview



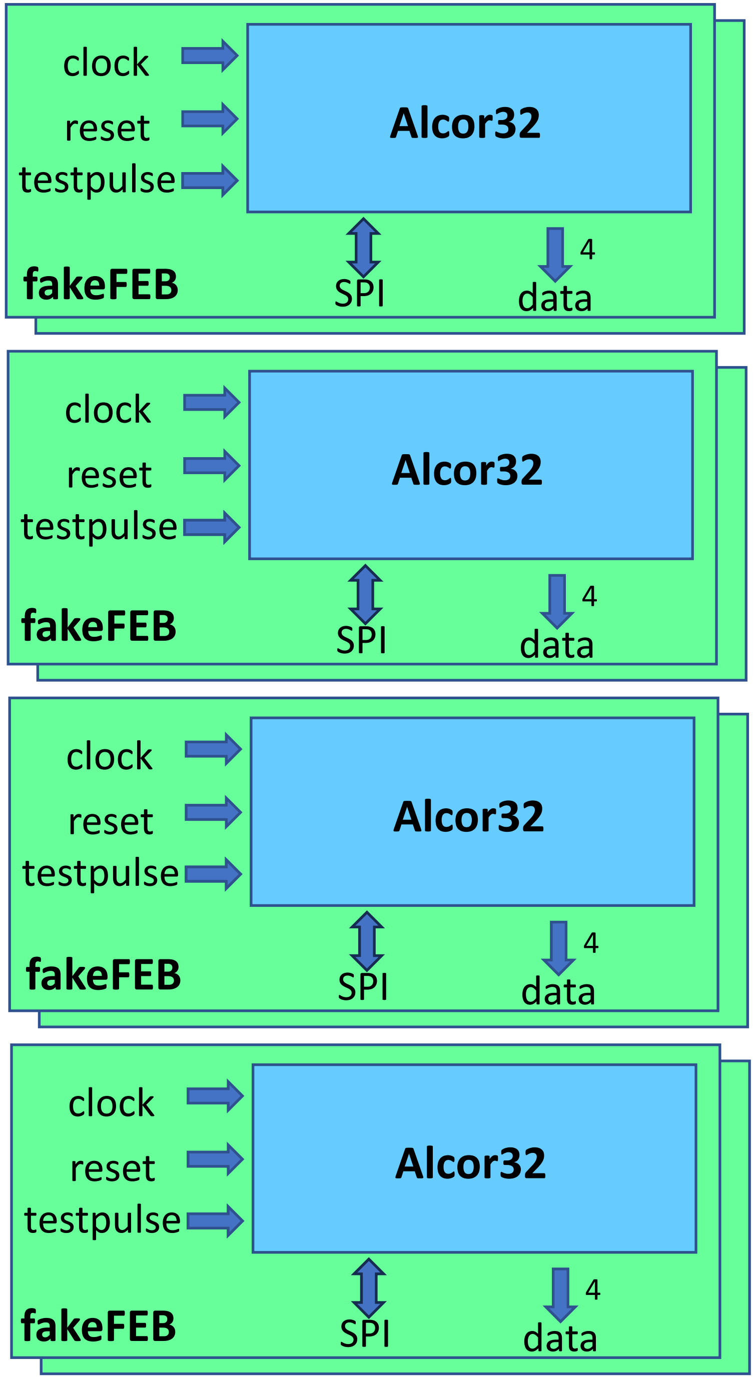
Readout concept: 4 Alcor64

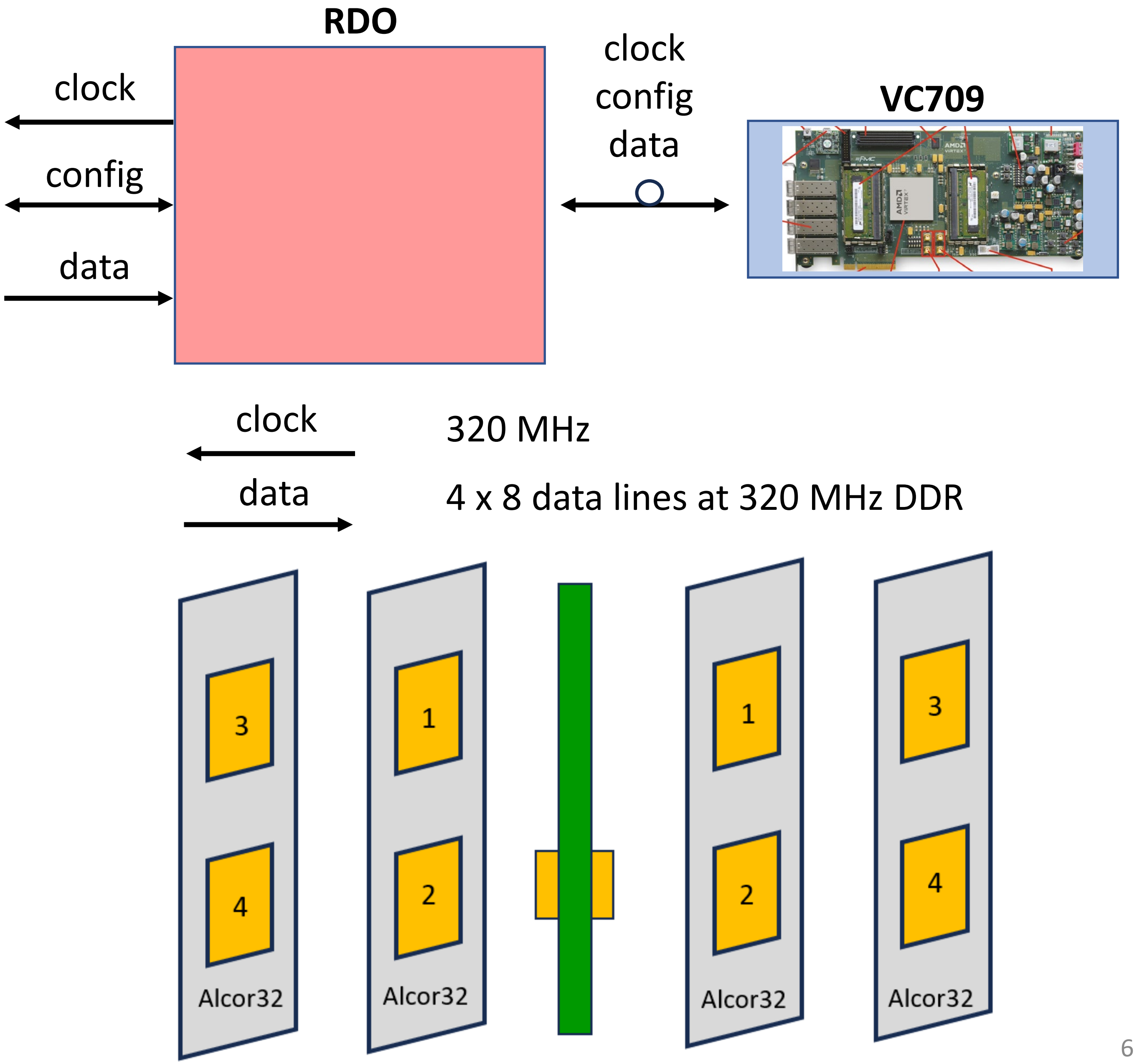




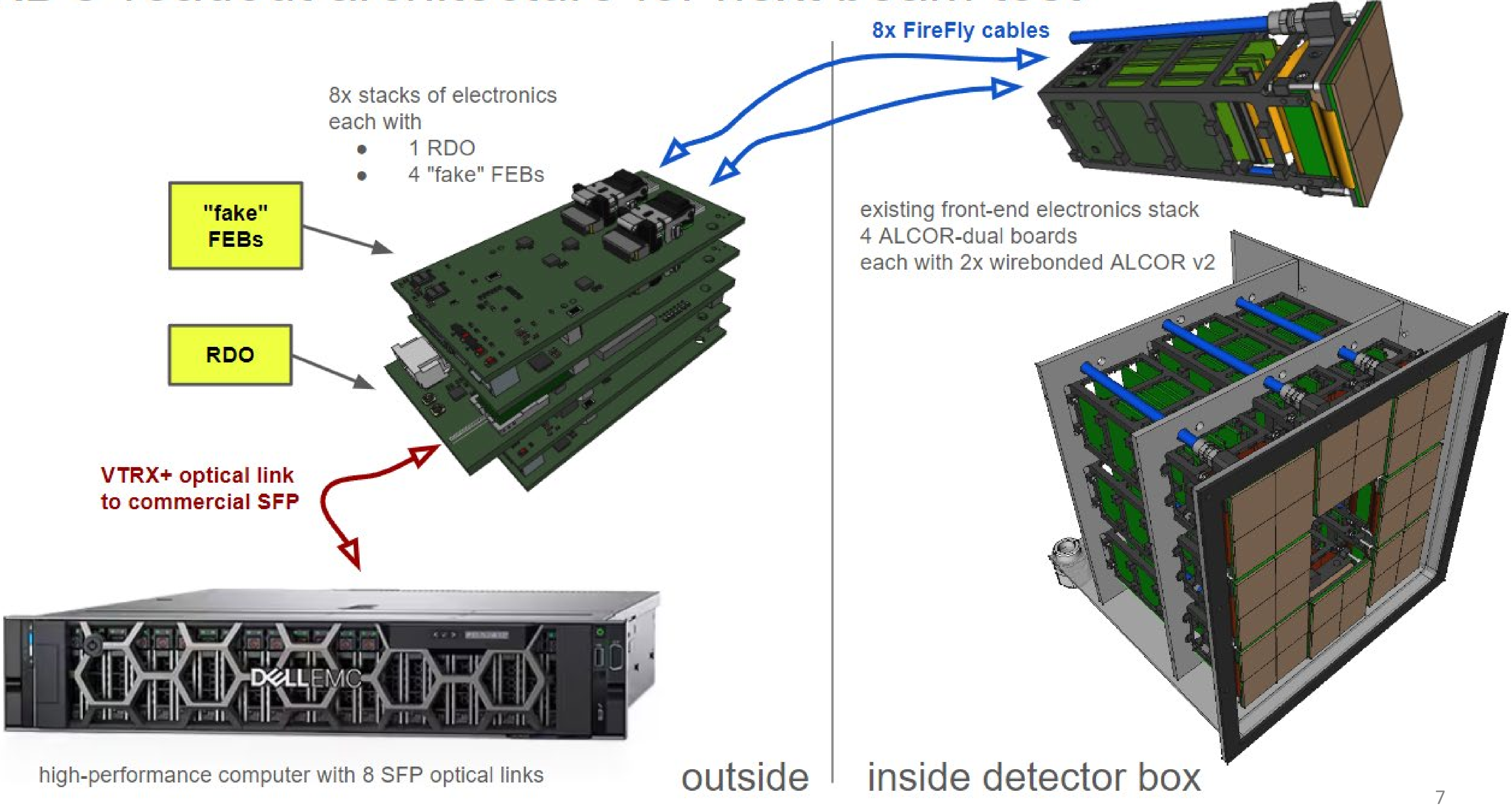


Readout concept: 8 Alcor32

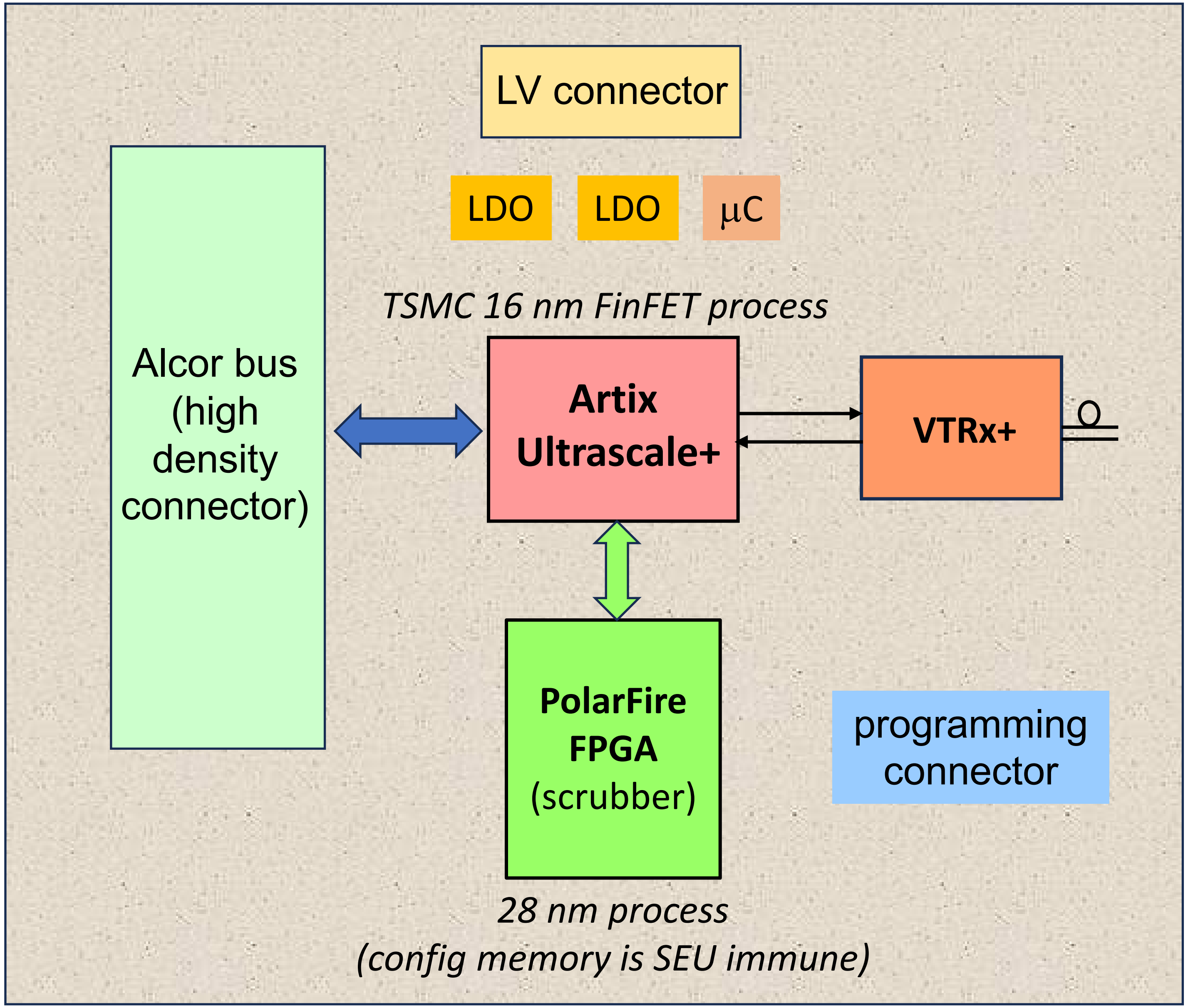




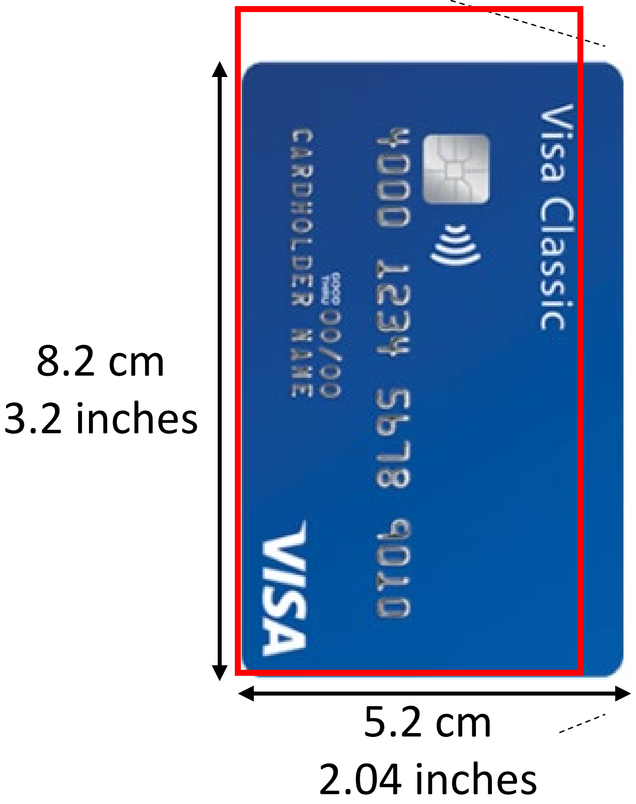
RDO readout architecture for next beam test



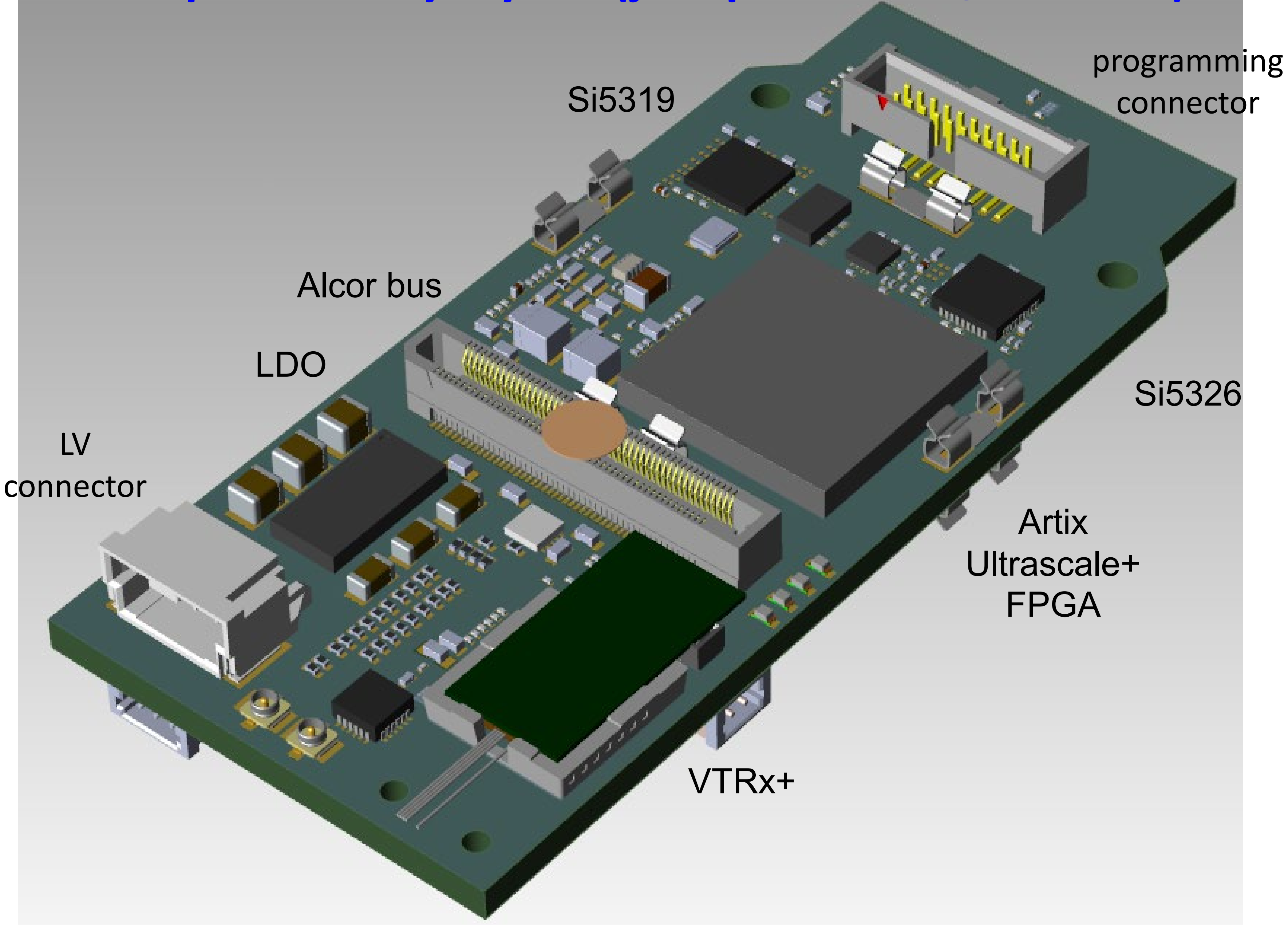
dRICH RDO architecture



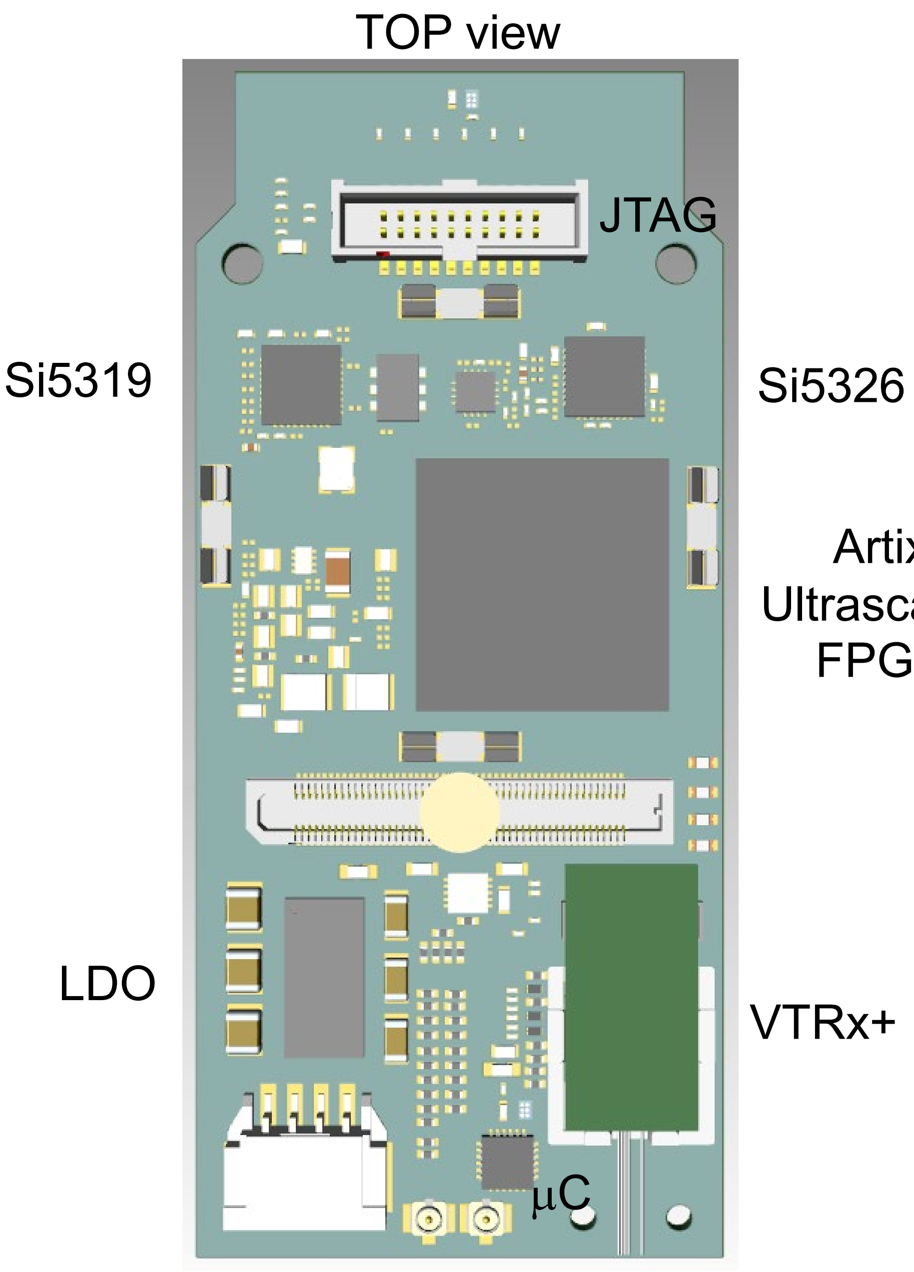
The real challenge for the dRICH RDO design is to fit in **a very limited size**, quite similar to a credit card



RDO preliminary layout (just placement, 3D view)

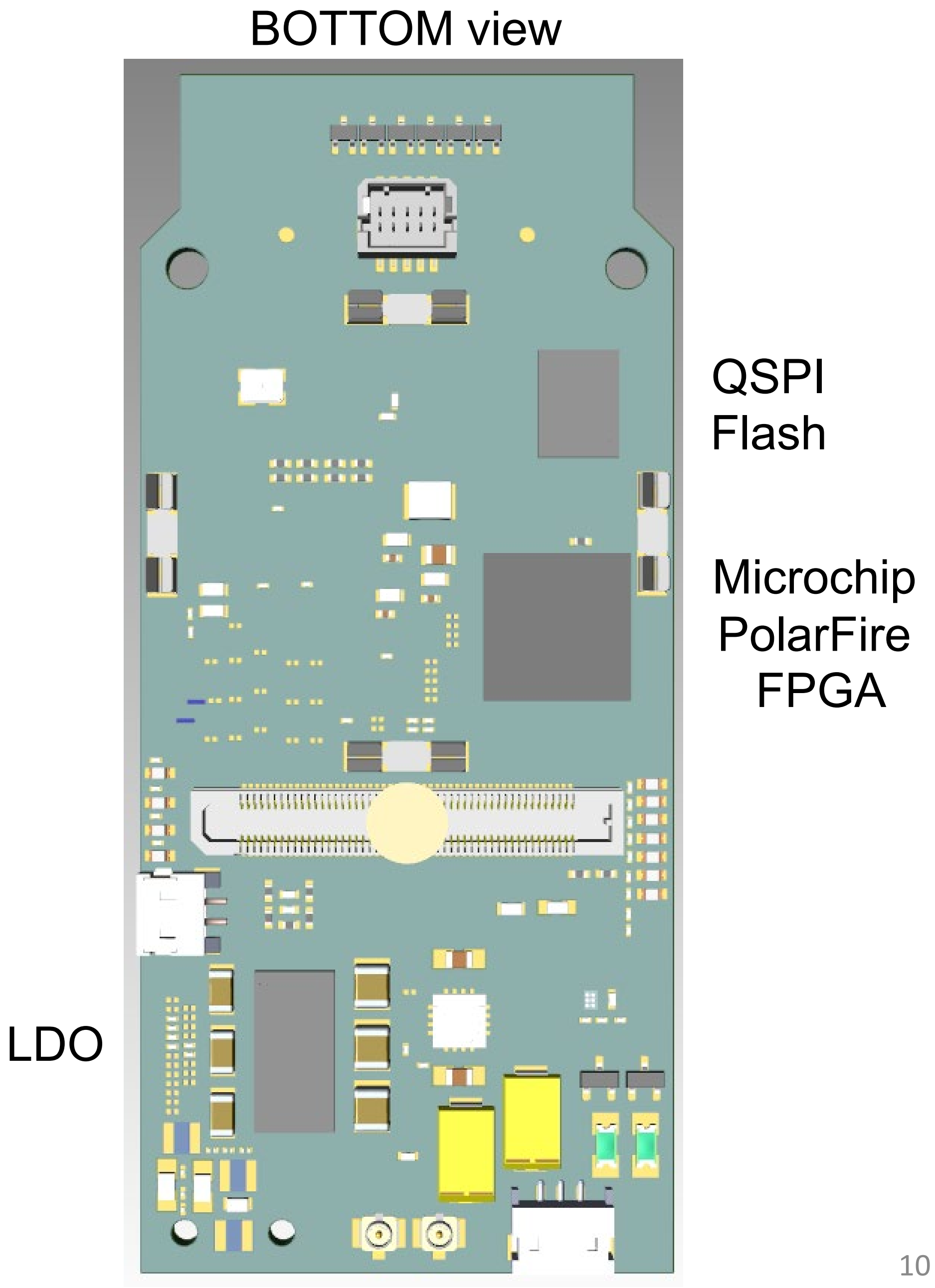


RDO preliminary layout (2D view)



Artix Ultrascale+ FPGA

Alcor bus



QSPI Flash

Microchip PolarFire FPGA

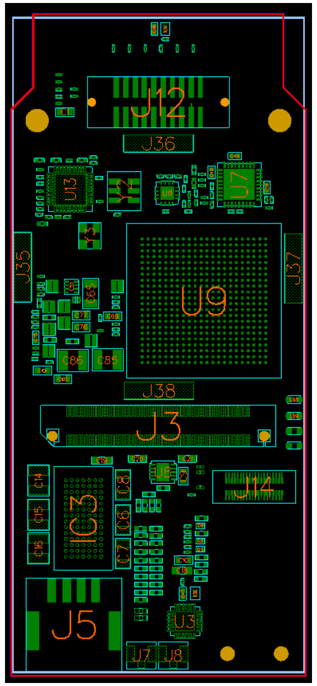
RDO main challenge: size

these pictures are on scale!

8.2 cm
3.2 inches

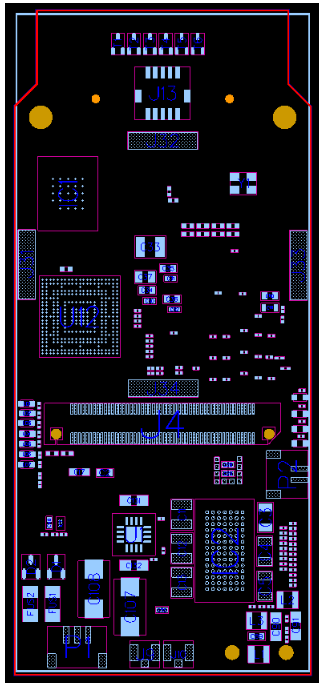
5.2 cm
2.04 inches

TOP



4.0 cm
1.57 inches

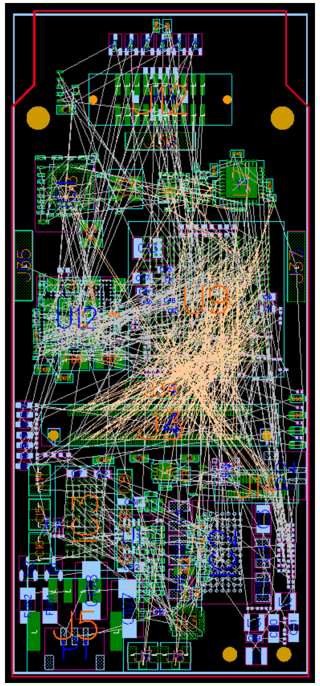
BOT



4.0 cm
1.57 inches

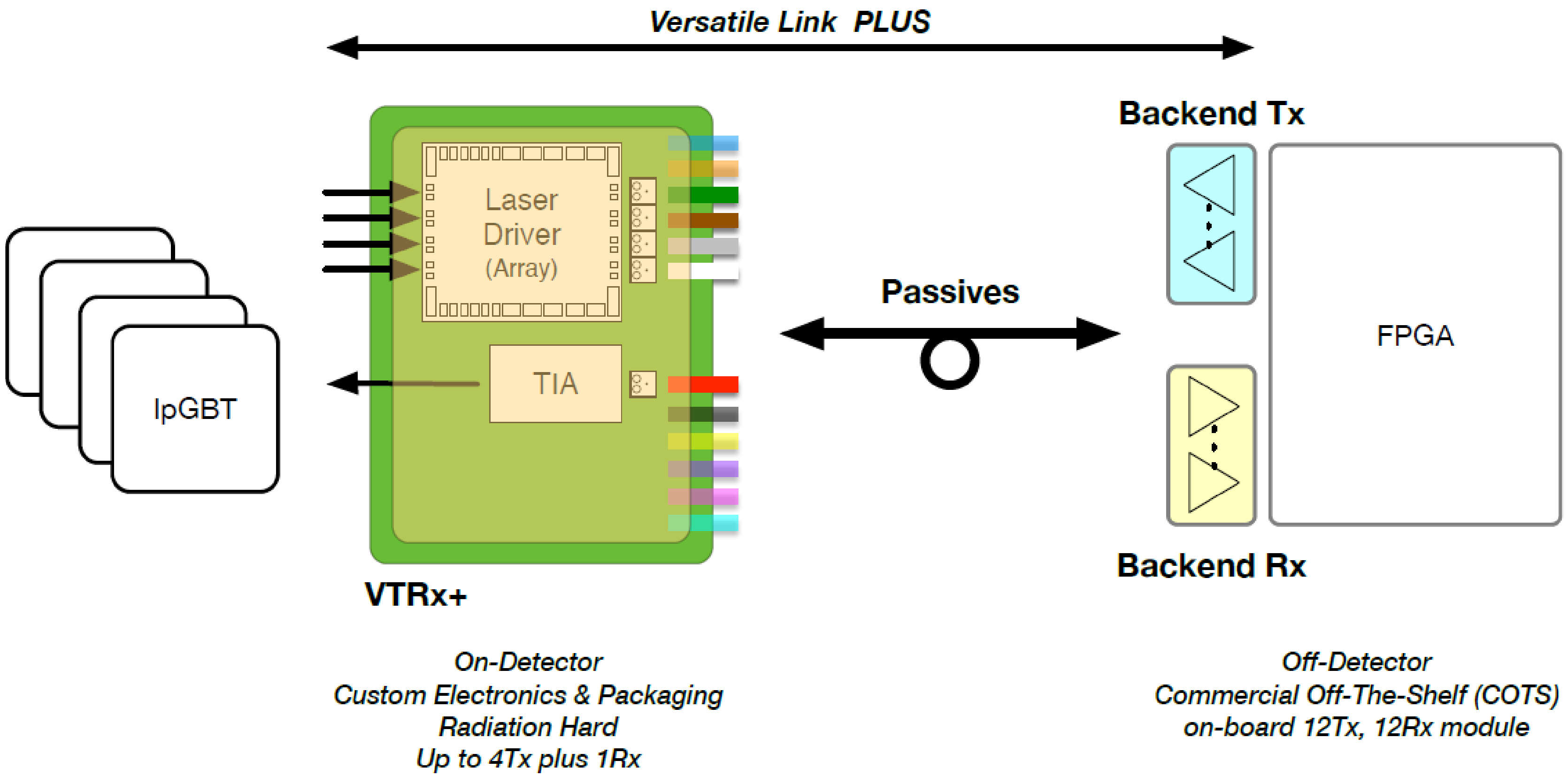
9.0 cm
3.54 inches

nets to route



The routing of all the signals is going to be a nightmare: 16-18 layers foreseen at minimum

Optical transceiver: VTRx+

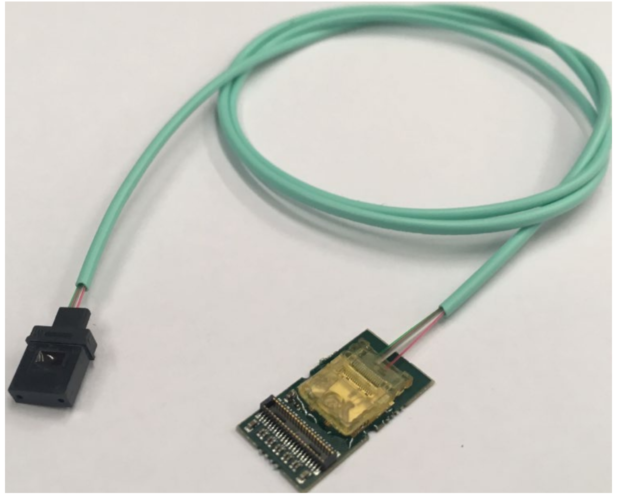


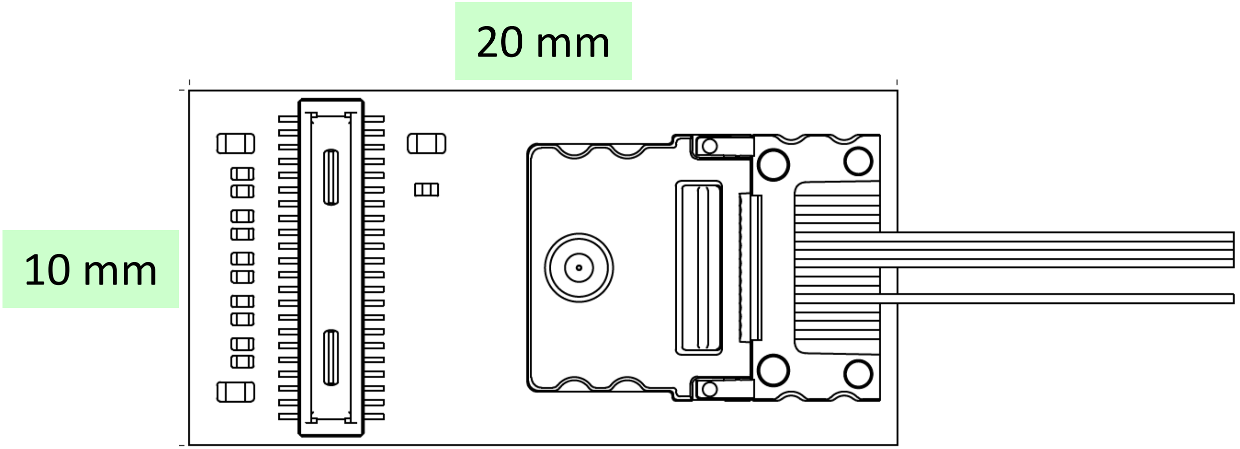
The Versatile Link+ (VL+) is a bi-directional digital optical data link with up to four upstream channels operating at up to **10.24 Gb/s** and one downstream channel operating at **2.56 Gb/s**. It is targeted to operate with the Low-power GigaBit Transceiver (lpGBT) serializer/deserializer chip at the front-end and with a lpGBT core instantiated in an FPGA at the back-end.

Optical transceiver: VTRx+

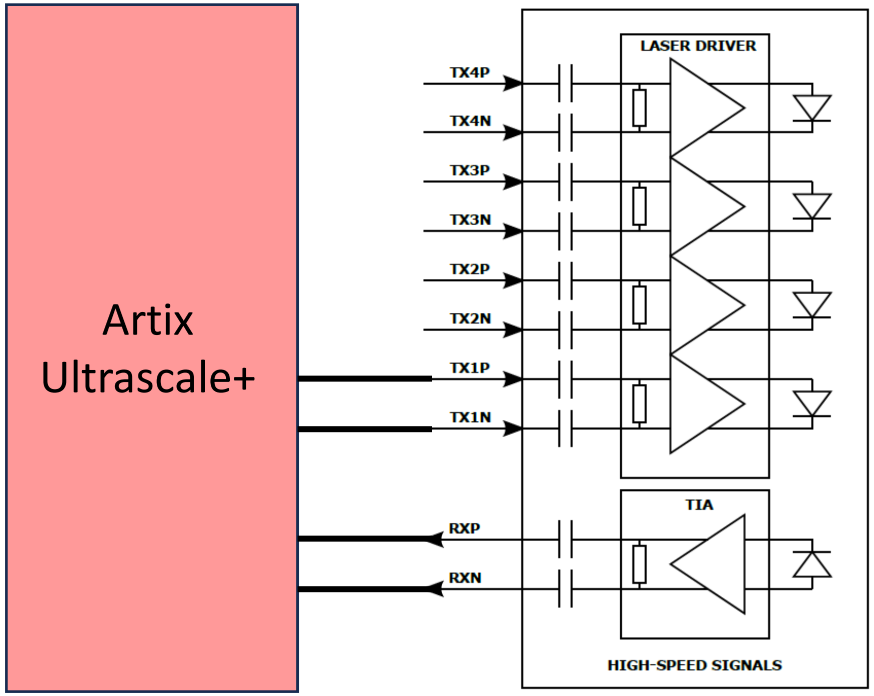
The front-end VTRx+ must withstand radiation, operate in a magnetic field and in many cases be as small and light-weight as possible

female MT connector

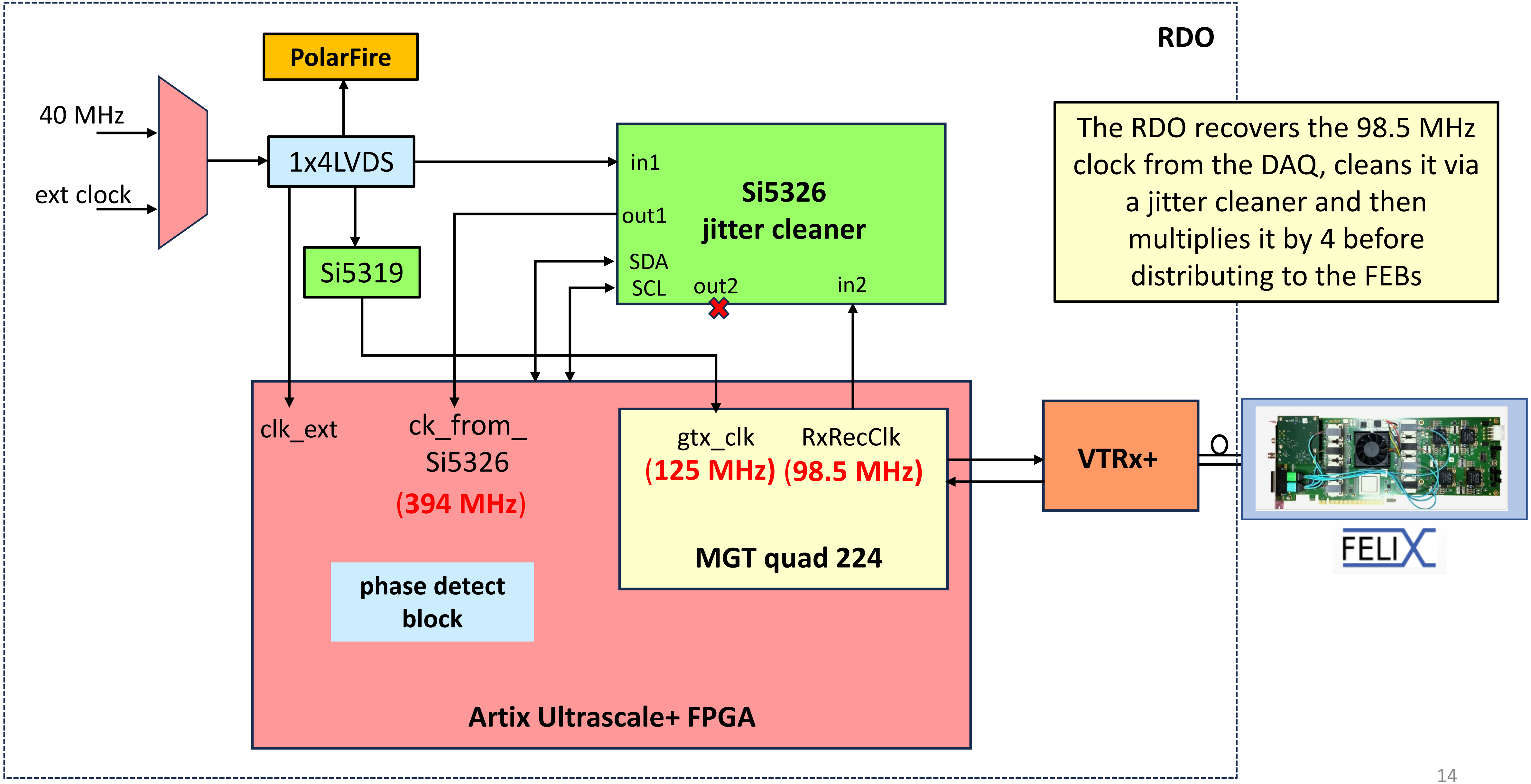




Standard Grade	1 MGy 1.7×10^{14} neutrons/cm^2 1.7×10^{14} hadrons/cm^2
Extended Grade	1 MGy 1×10^{15} neutrons/cm^2 1×10^{15} hadrons/cm^2

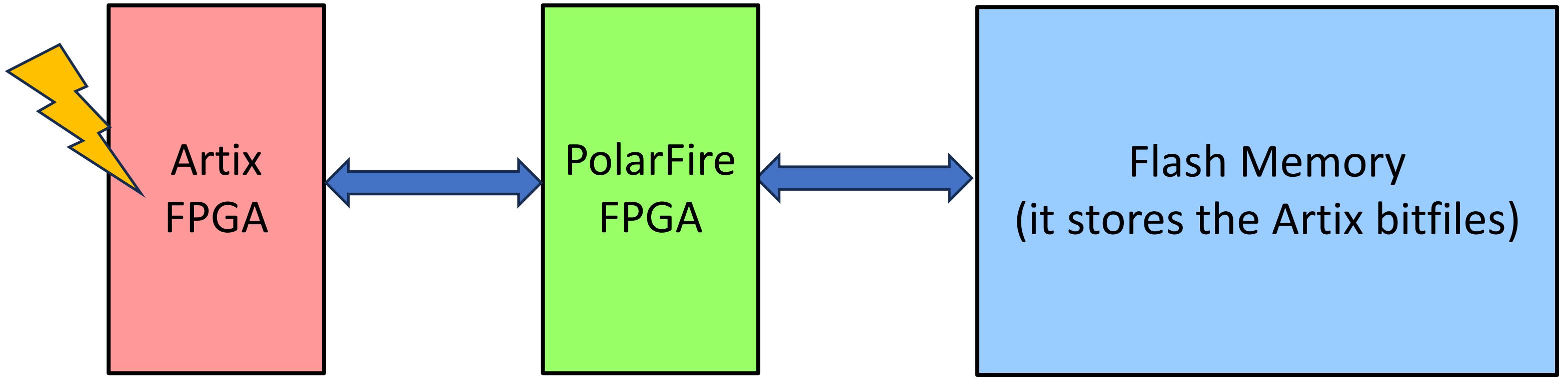


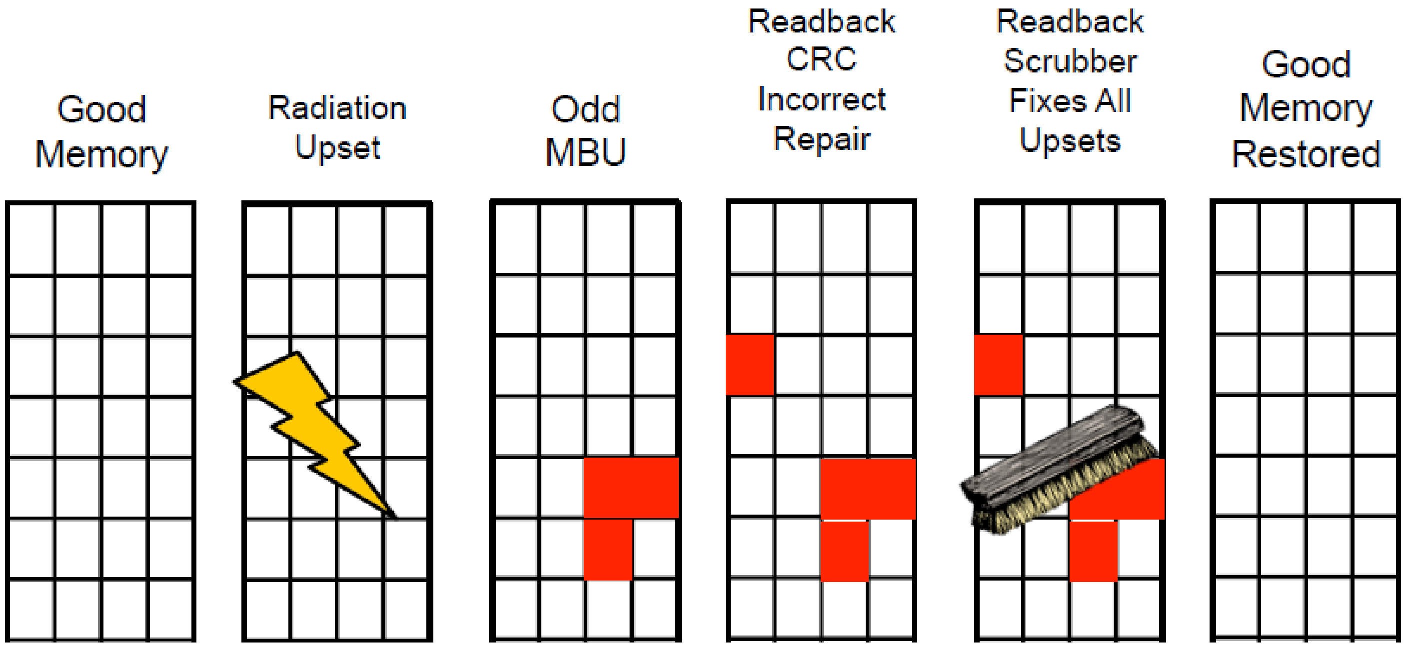
Clock distribution scheme



The RDO recovers the 98.5 MHz clock from the DAQ, cleans it via a jitter cleaner and then multiplies it by 4 before distributing to the FEBs

SRAM based FPGA configuration memory: scrubbing





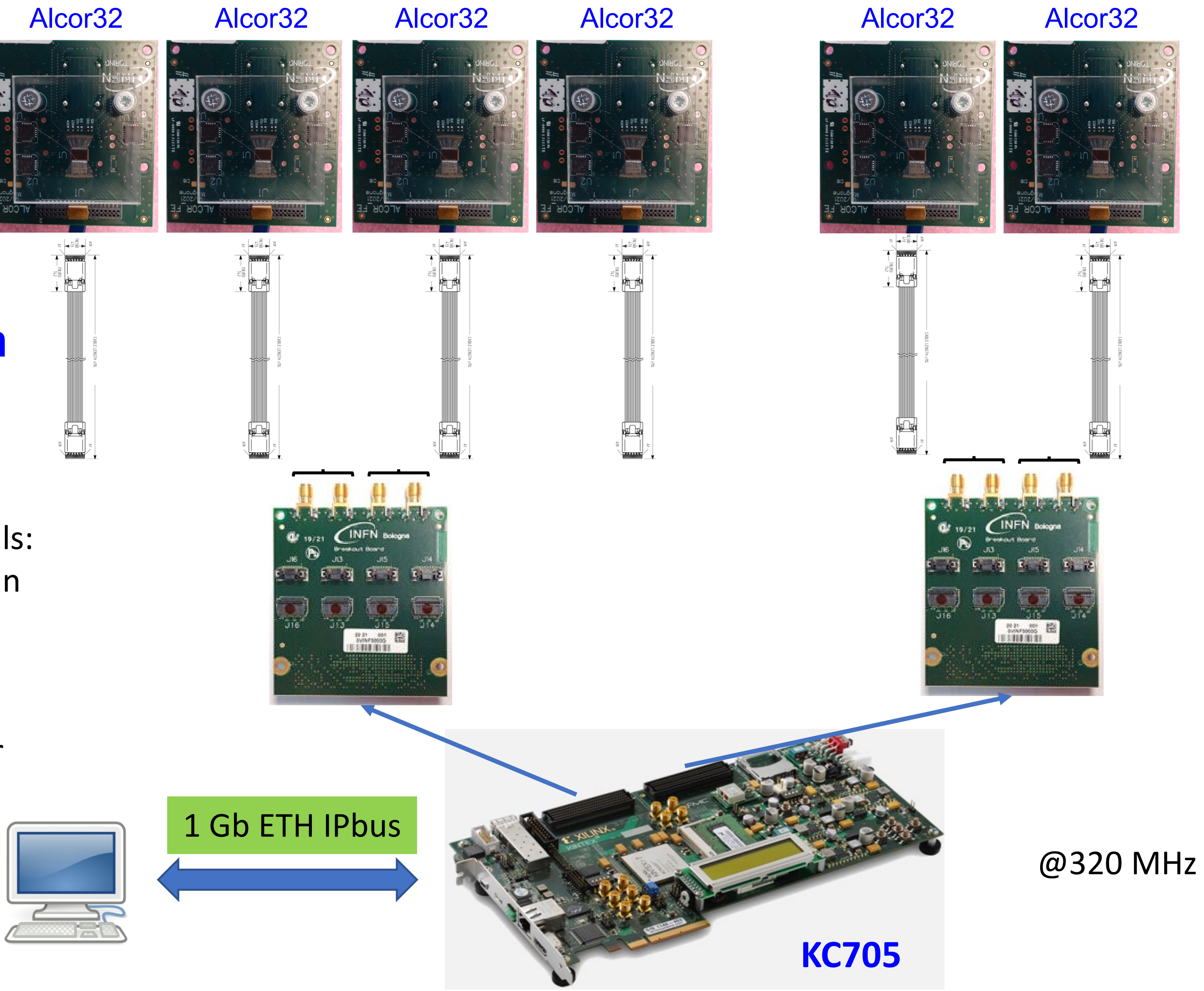
external storage

Scrubbing can be done with an internal device (like **Soft Error Mitigation IP**) or an external rad-tol device: we are using a Microchip PolarFire FPGA for the job

Starting point for RDO firmware design

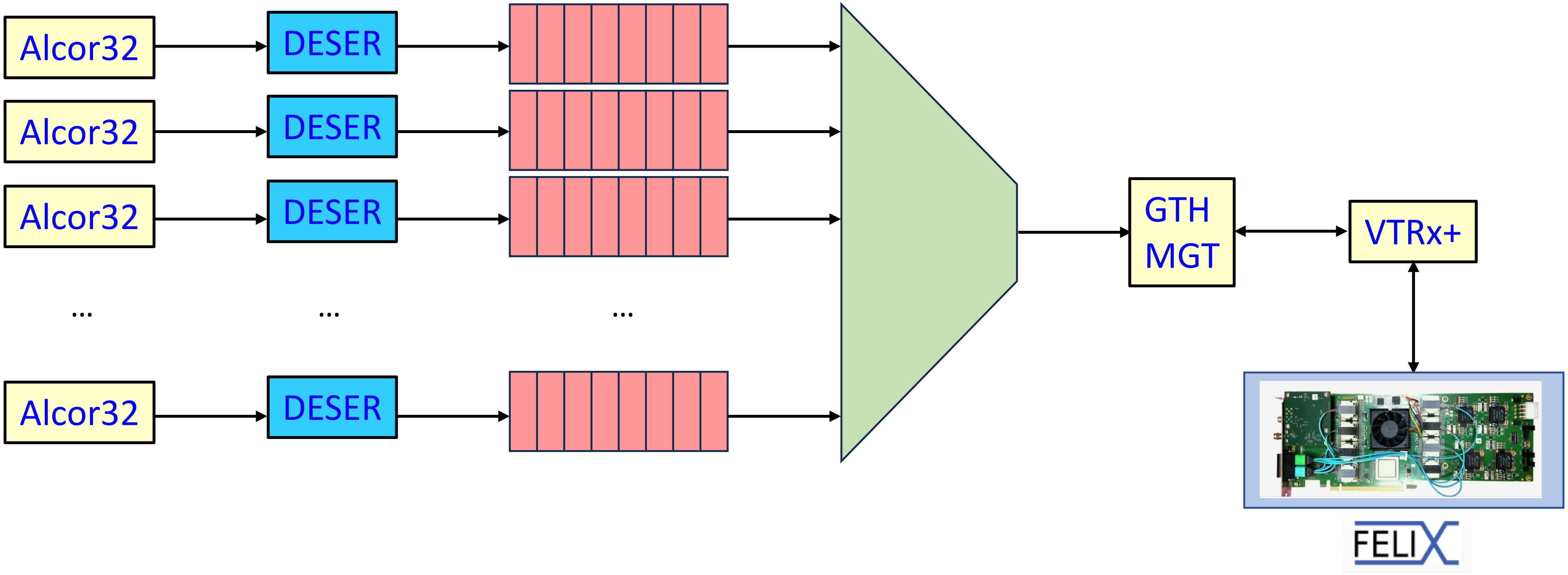
A first firmware for the Artix Ultrascale+ (starting from the KC705 firmware) has ben developed with the following goals:

- validate the pinout used in the schematics
- validate the FPGA performances
- estimate the FPGA power consumption



Firmware design for RDO

Main data flow from 8 Alcor32 chips (or 4 Alcor64) towards the DAQ system



Timing summary @ 400 MHz

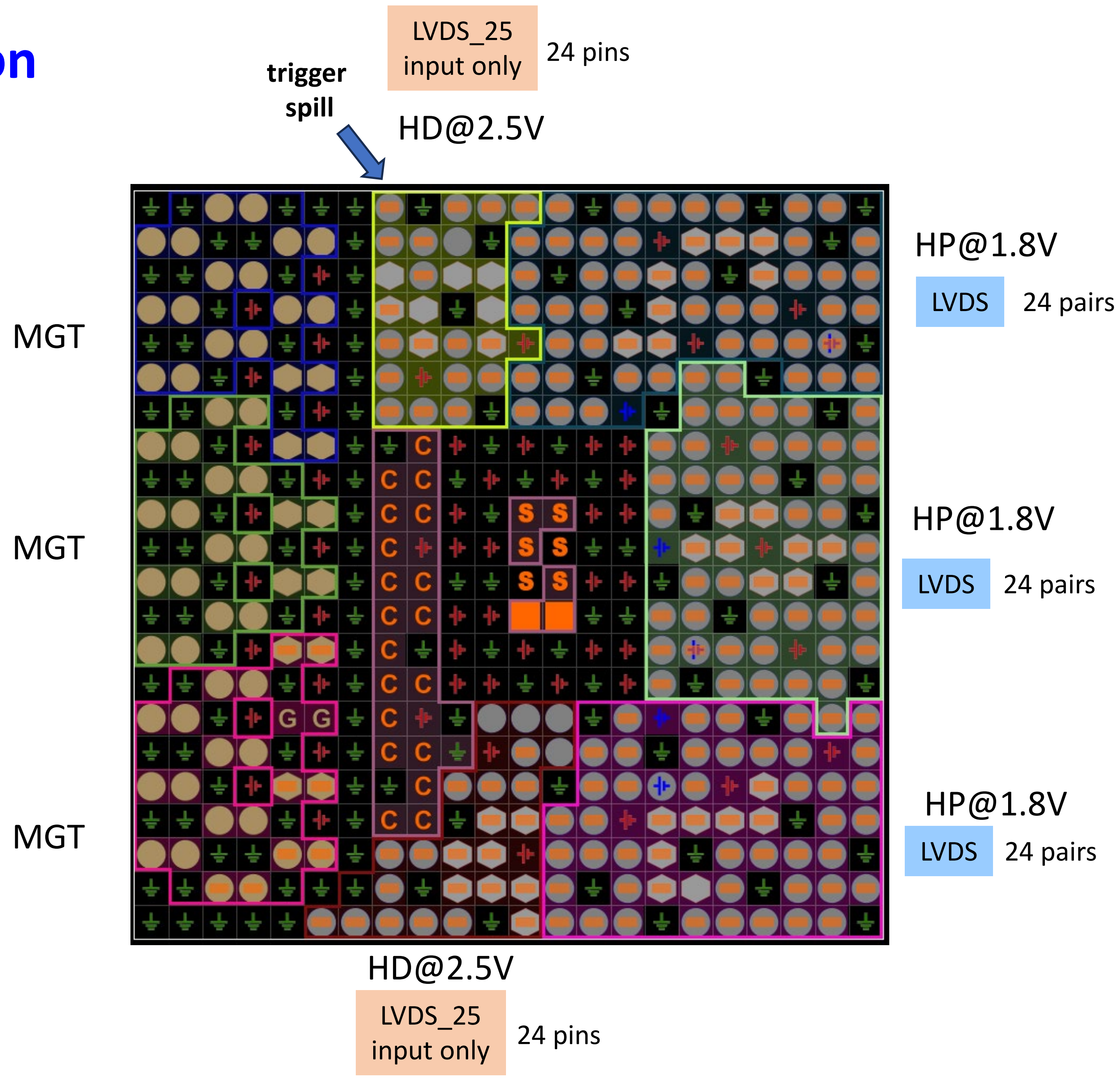
Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.385 ns	Worst Hold Slack (WHS):	0.010 ns	Worst Pulse Width Slack (WPWS):	0.250 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	70995	Total Number of Endpoints:	69295	Total Number of Endpoints:	35268

All user specified timing constraints are met.

Firmware was validated also @ 400 MHz

Pinout validation

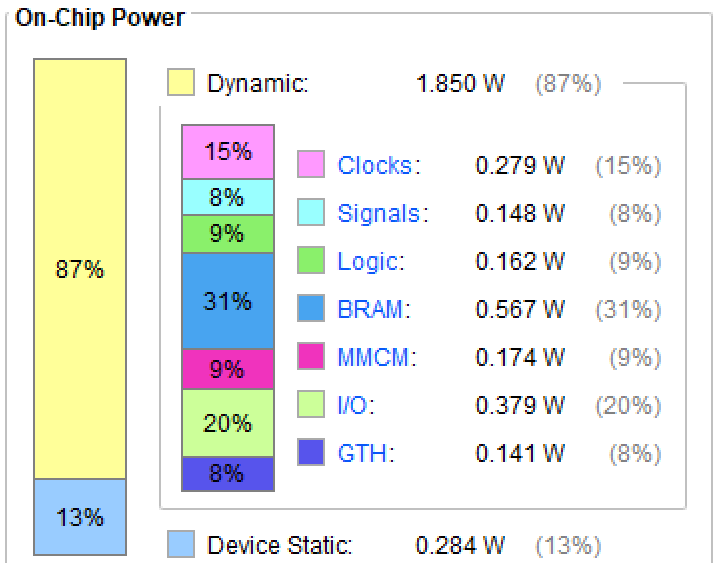


Power consumption @ 400 MHz

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

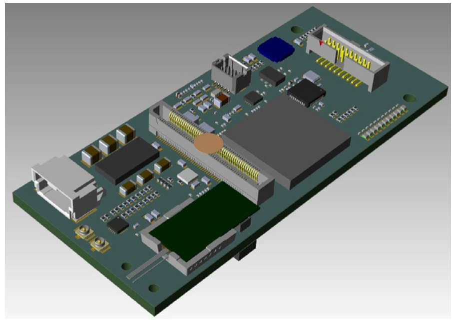
Total On-Chip Power:	**2.134 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**30.8°C**
Thermal Margin:	69.2°C (24.8 W)
Effective ϑJA:	2.7°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



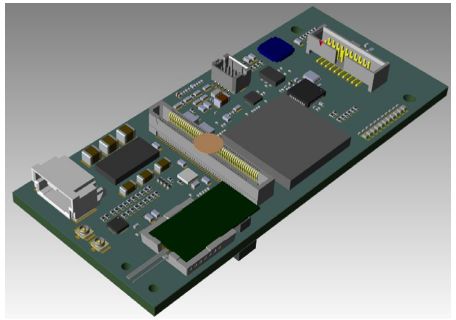
Power Supply

Supply Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)	Budget (A)	Margin (A)
Vccint	0.850	1.322	1.262	0.060	Unspecified	NA
Vccint_io	0.850	0.062	0.035	0.027	Unspecified	NA
Vccbram	0.850	0.106	0.106	0.001	Unspecified	NA
Vccaux	1.800	0.159	0.096	0.063	Unspecified	NA
Vccaux_io	1.800	0.066	0.042	0.023	Unspecified	NA
Vcco33	3.300	0.000	0.000	0.000	Unspecified	NA
Vcco25	2.500	0.011	0.006	0.005	Unspecified	NA
Vcco18	1.800	0.142	0.142	0.000	Unspecified	NA
Vcco15	1.500	0.000	0.000	0.000	Unspecified	NA
Vcco135	1.350	0.000	0.000	0.000	Unspecified	NA
Vcco12	1.200	0.000	0.000	0.000	Unspecified	NA
Vcco10	1.000	0.000	0.000	0.000	Unspecified	NA
Vccadc	1.800	0.008	0.000	0.008	Unspecified	NA
MGTAVcc	0.900	0.039	0.030	0.009	Unspecified	NA
MGTAVtt	1.200	0.107	0.093	0.014	Unspecified	NA
MGTVccaux	1.800	0.000	0.000	0.000	Unspecified	NA

The total RDO power consumption is ~3.5W



Status of the design and conclusions

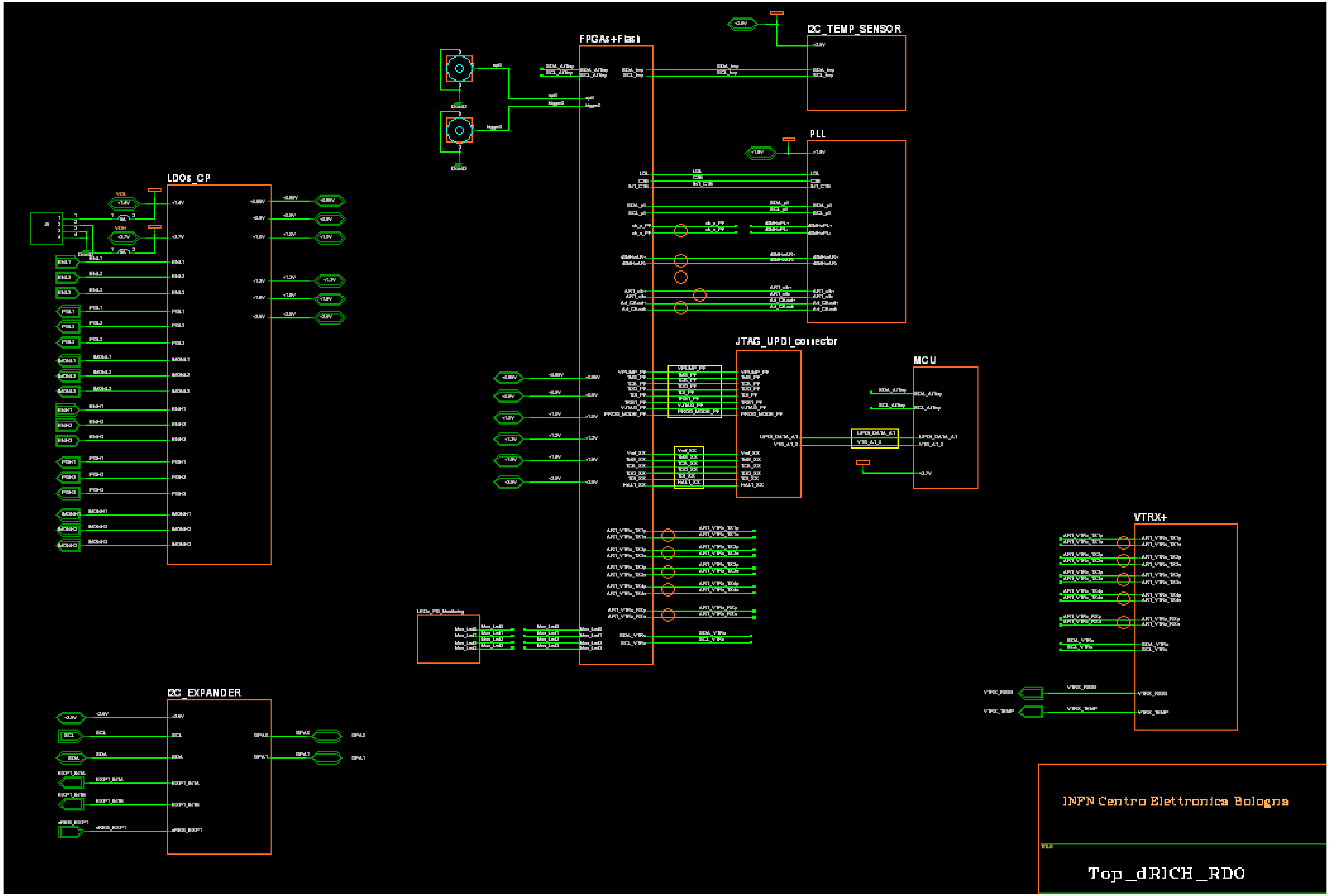


- the schematic design of **dRICH RDO** is finished:
  - now performing the final checks
- the desired placement is ready
- the PCB layout is going to start soon
- we plan to have the first prototypes ready beginning 2025 and to do extensive debug
- we are working on the firmware in the meanwhile

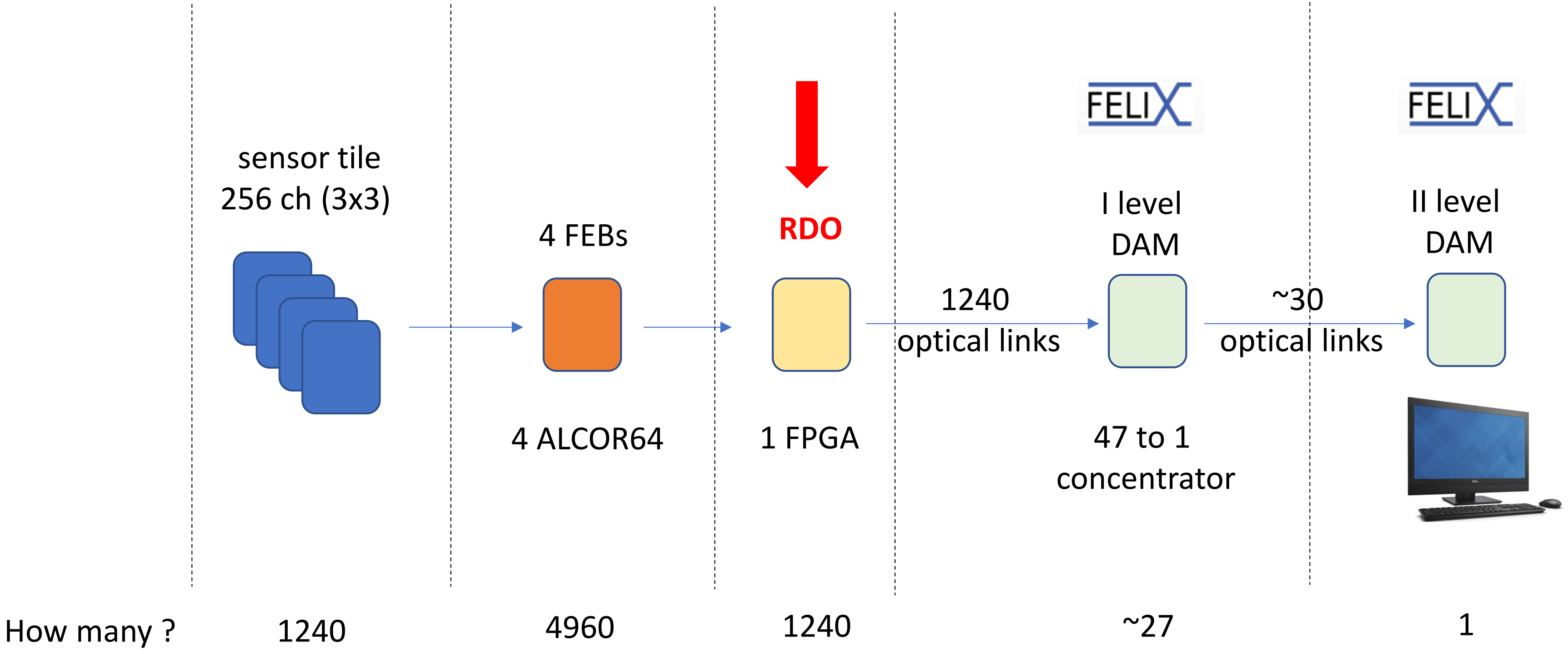
Thanks!

Backup

RDO schematics

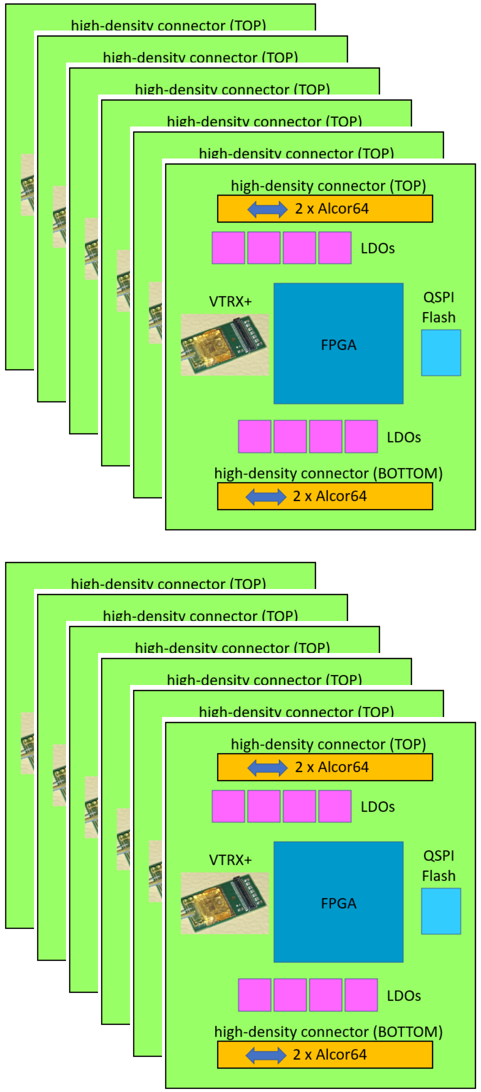


Readout concept



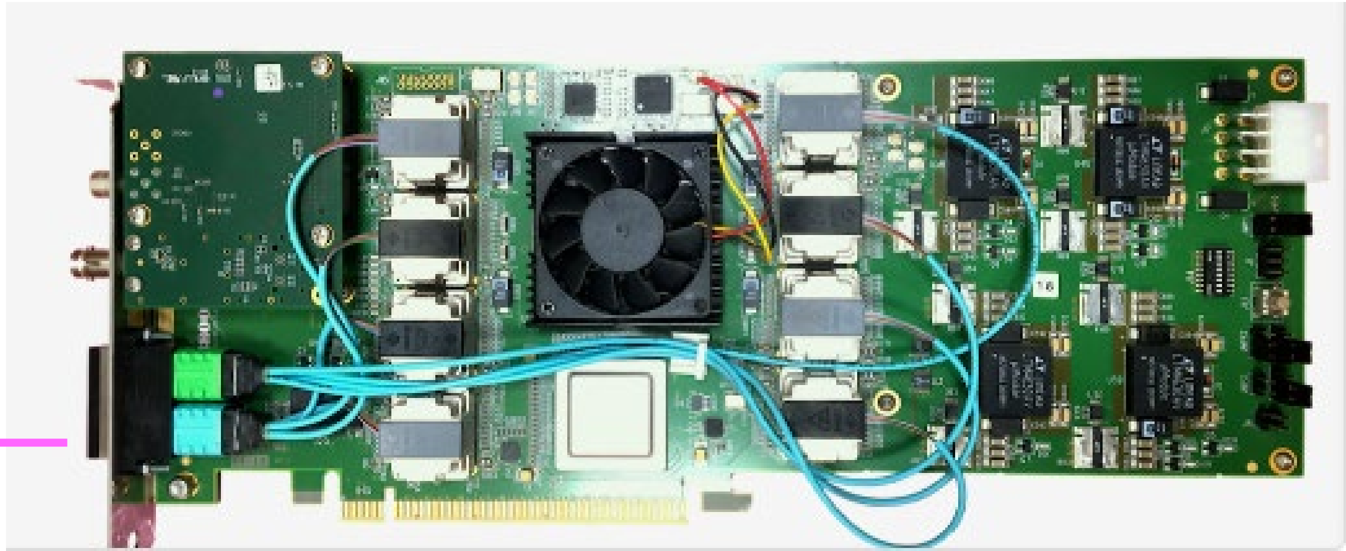
I level DAM: 42 to 1 concentrator

42 RDOs



42 optical links

Felix board

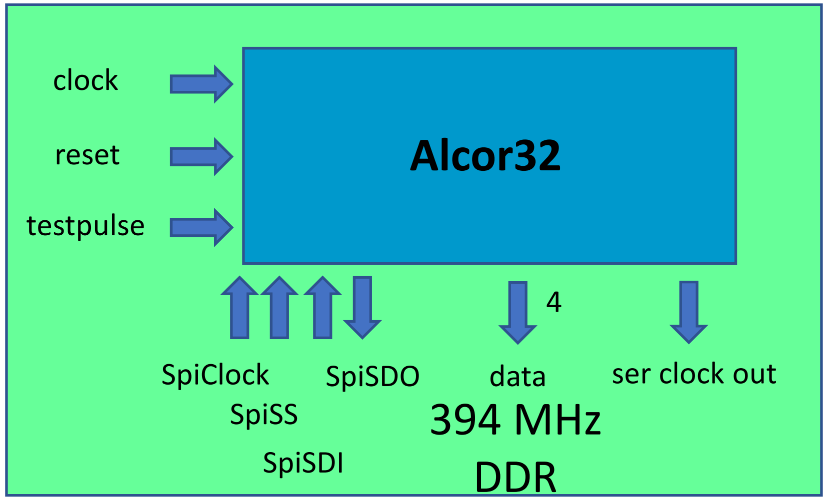


1 optical link towards II level DAM

this solution requires modifications to the standard Felix firmware

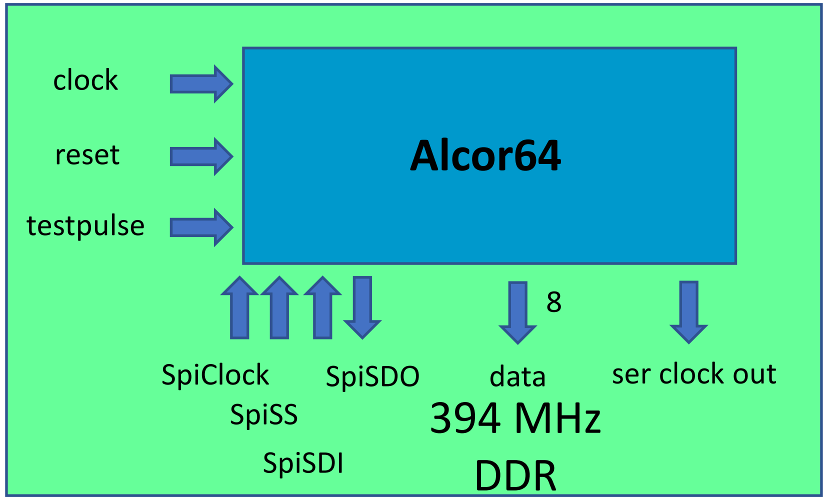
Alcor32 vs Alcor64 I/Os

394 MHz



12 LVDS pairs per chip

394 MHz



16 LVDS pairs per chip

First FPGA candidate: Xilinx Artix Ultrascale+ family

	AU7P	AU10P	AU15P	AU20P	AU25P
System Logic Cells	81,900	96,250	170,100	238,437	308,437
CLB Flip-Flops	74,880	88,000	155,520	218,000	282,000
CLB LUTs	37,440	44,000	77,760	109,000	141,000
Max. Distributed RAM (Mb)	1.1	1.0	2.5	3.2	4.7
Block RAM Blocks	108	100	144	200	300
Block RAM (Mb)	3.8	3.5	5.1	7.0	10.5
UltraRAM Blocks	–	–	–	–	–
UltraRAM (Mb)	–	–	–	–	–
CMTs (1 MMCM and 2 PLLs)	2	3	3	3	4
Max. HP I/O(1)	104	156	156	156	208
Max. HD I/O(2)	144	72	72	72	96
DSP Slices	216	400	576	900	1,200
System Monitor	1	1	1	1	1
GTH Transceiver(3)	4	12	12	–	–

Package (1)(2)(3)	Package Dimensions (mm)	AU7P	AU10P	AU15P	AU20P	AU25P
		HD I/O, HP I/O, GTH, GTY				
UBVA292	10.5x8.5	72, 58, 4, 0				
UBVA368	11.5x9.5		24, 104, 8, 0	24, 104, 8, 0		
SBVB484	19x19		48, 156, 12, 0	48, 156, 12, 0		
SBVC484	19x19	144, 104, 4, 0				
SFVB784	23x23				72, 156, 0, 12	96, 208, 0, 12
FFVB676	27x27		72, 156, 12, 0	72, 156, 12, 0	72, 156, 0, 12	72, 208, 0, 12

Xilinx Artix Ultrascale+ family

VCCINT = 0.850 V
VCCAUX = 1.800 V
VCCO = 1.140 – 3.400 V for HD I/O banks
VCCO = 0.500 – 1.900 V for HP I/O banks

HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.

HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.

GTH and GTY transceiver line rates are package limited: SFVB784, SBVB484, UBVA368, and UBVA292 to 12.5Gb/s

LVDS DC specifications (HP I/O banks)

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO} [1]	Supply voltage		1.710	1.800	1.890	V
V_{ODIFF} [2]	Differential output voltage: $(Q - \overline{Q})$, Q = High $(\overline{Q} - Q)$, $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	454	mV
V_{OCM} [2]	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF} [3]	Differential input voltage: $(Q - \overline{Q})$, Q = High $(\overline{Q} - Q)$, $\overline{Q}$ = High		100	350	600 [3]	mV
V_{ICM_DC} [4]	Input common-mode voltage (DC coupling)		0.300	1.200	1.425	V

Second FPGA candidate: Microchip PolarFire family

	MPF050	MPF100	MPF200	MPF300	MPF500
Logic Elements (4LUT + DFF)	48K	109K	192K	300K	481K
Math Blocks (18 × 18 MACC)	150	336	588	924	1480
LSRAM Blocks (20 Kb)	160	352	616)	952	1520
uSRAM Blocks (64 × 12)	450	1008	1764	2772	4440
Total RAM (Mb)	3.6	7.6	13.3	20.6	33
uPROM (Kb)	216	297	297	459	513
User DLLs/PLLs	8	8 each	8 each	8 each	8 each
250 Mbps–12.7 Gbps Transceiver Lanes	4	8	16	16	24
PCIe® Gen 2 Endpoints/Root Ports	2	2	2	2	2
Total User I/O	176	296	364	512	584

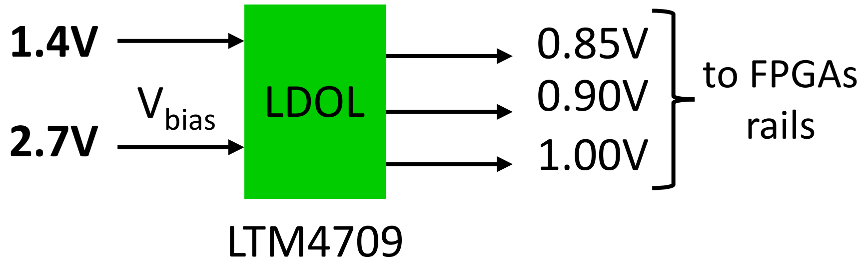
Differential DC input levels

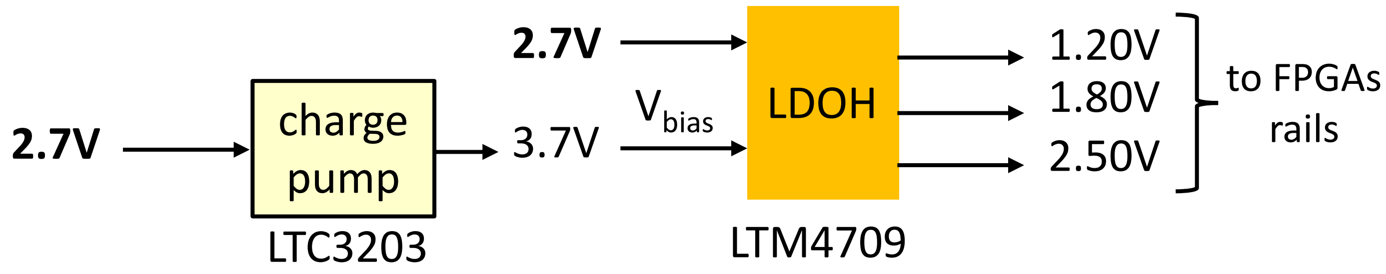
I/O Standard	Bank Type	V_{ICM_RANGE} Libero Setting	V_{ICM} [1,3] Min (V)	V_{ICM} [1,3] Typ (V)	V_{ICM} [1,3] Max (V)	V_{ID} [2] Min (V)	V_{ID} Typ (V)	V_{ID} Max (V)
LVDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS25 [7]	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS18G[4]	GPIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS18 [7]	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6

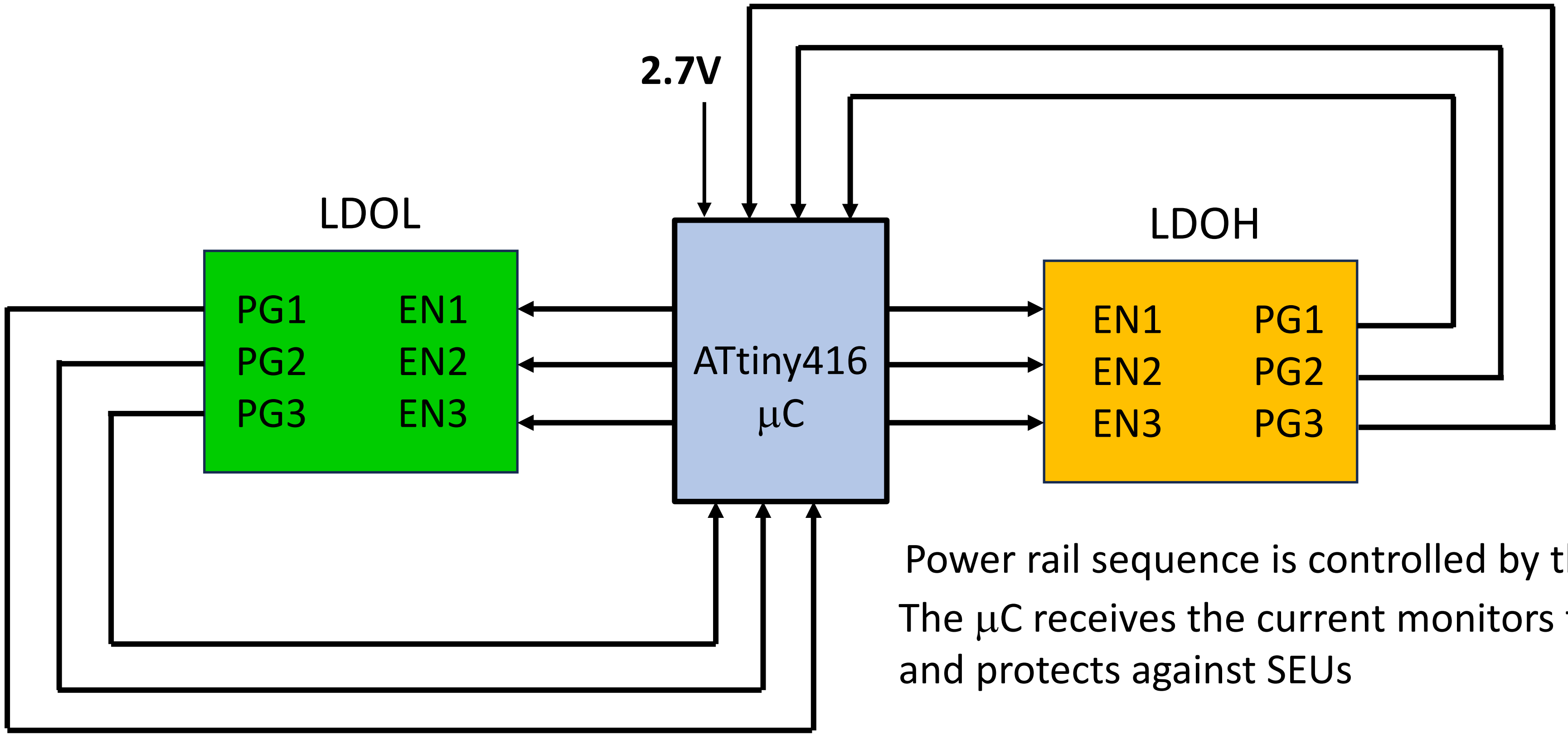
Differential DC output levels

I/O Standard	Bank Type	V_{OCM} [1] Min (V)	V_{OCM} Typ (V)	V_{OCM} Max (V)	V_{OD} [2] Min (V)	V_{OD} [2] Typ (V)	V_{OD} [2] Max (V)
LVDS33	GPIO	1.125	1.2	1.375	0.25	0.35	0.45
LVDS25 [4]	GPIO	1.125	1.2	1.375	0.25	0.35	0.45
LVDS18G[4]	GPIO	1.125	1.2	1.375	0.25	0.35	0.45

Power management





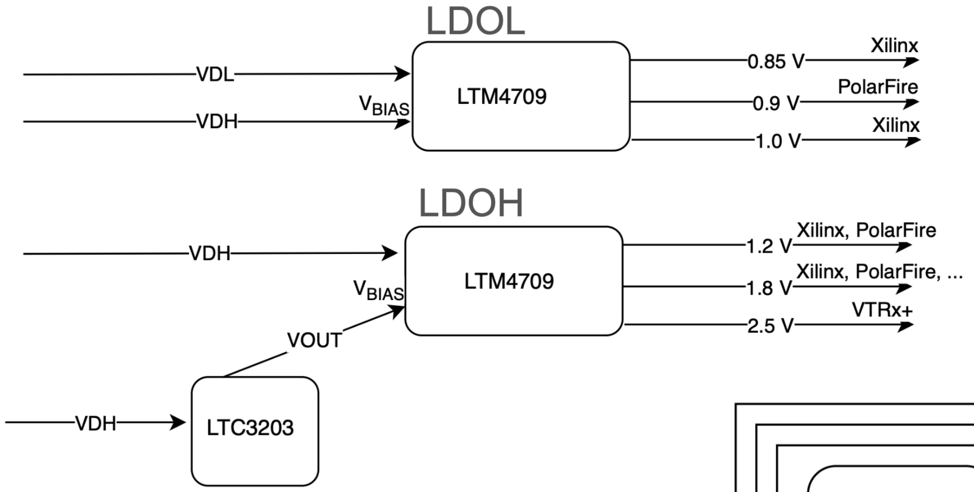


Power rail sequence is controlled by the ATtiny

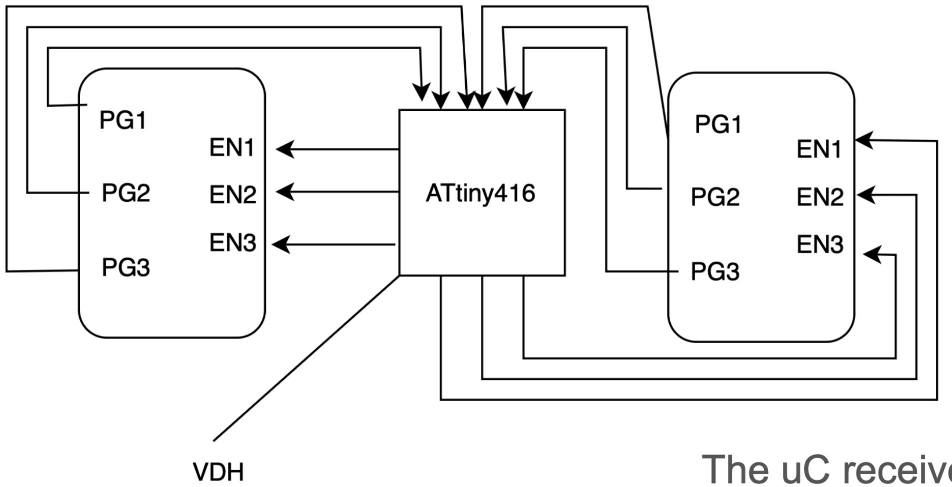
The μC receives the current monitors from the 2 LDOs and protects against SEUs

Power management

VDH: the high primary digital V: 2.7 V
VDL: the low primary digital V: 1.4 V
VOUT needs to be 3.7 V



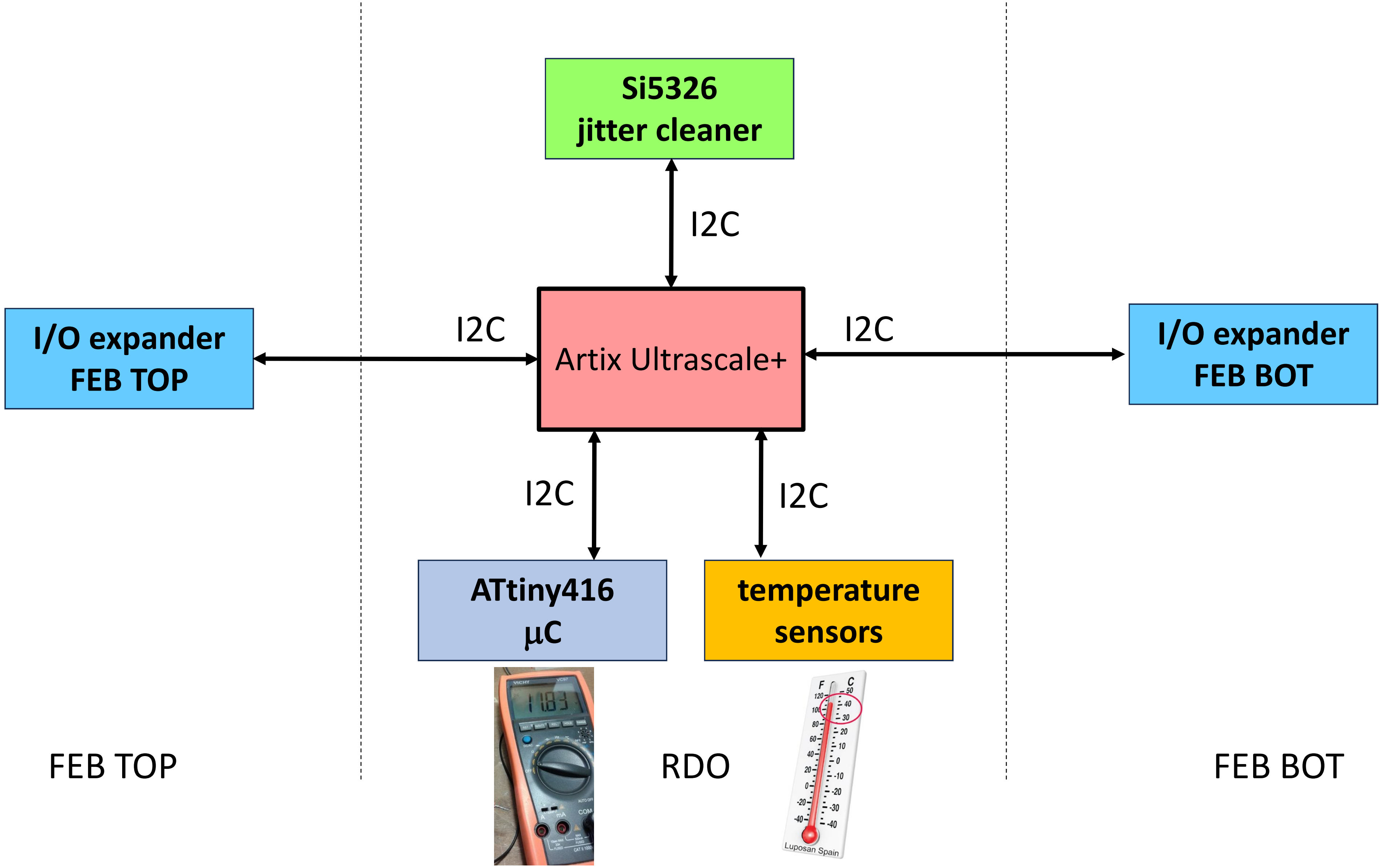
LTC3203 https://www.analog.com/en/products/ltc3203.html



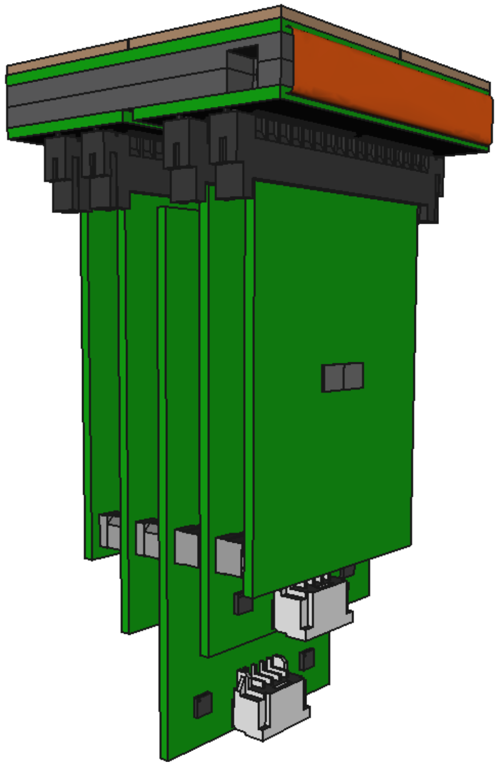
The uC receives the current monitors from the two LDOs and protect against SEL

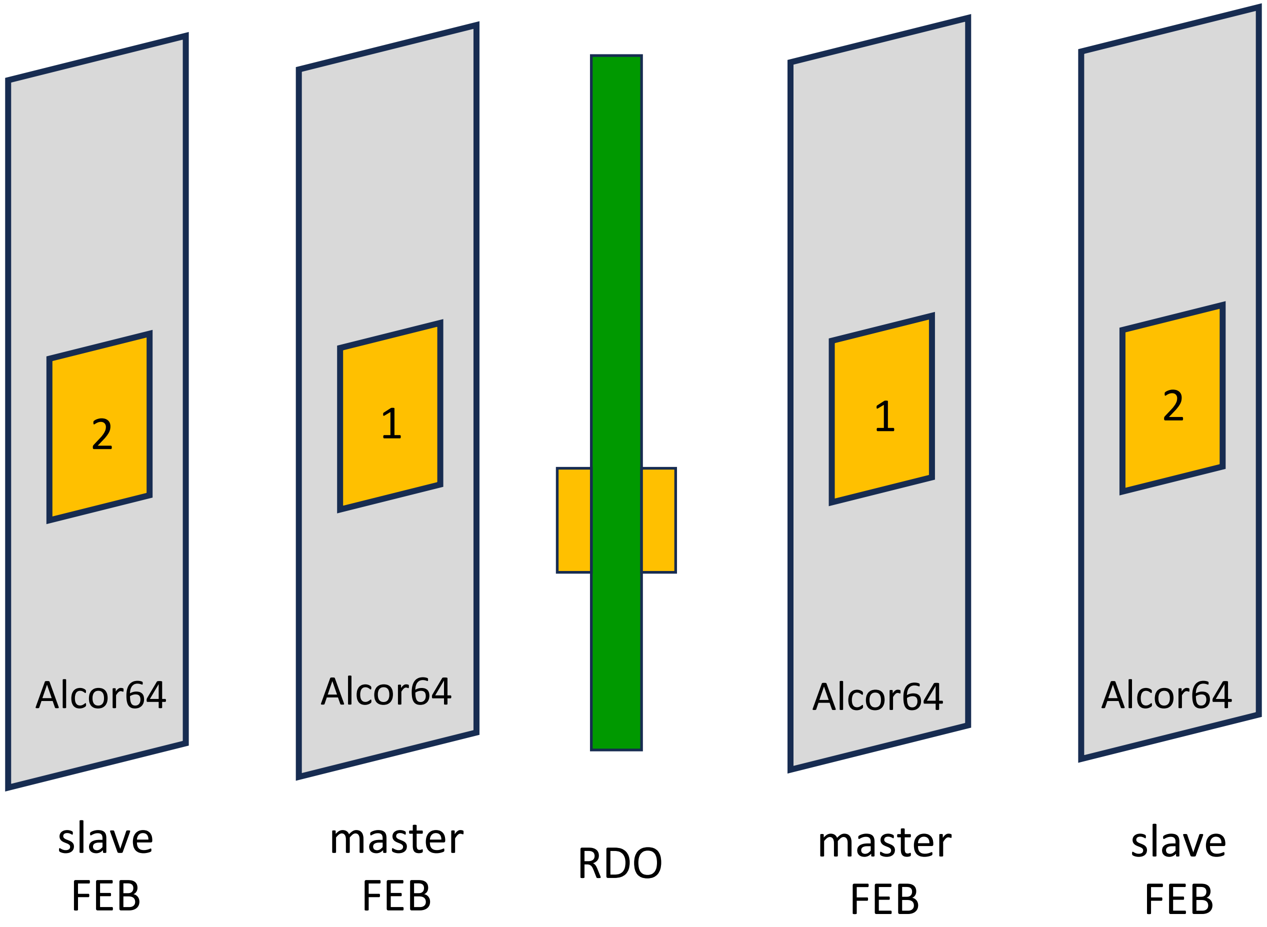
ATtiny416:
Product Selection Guide
Datasheet

Slow control connections

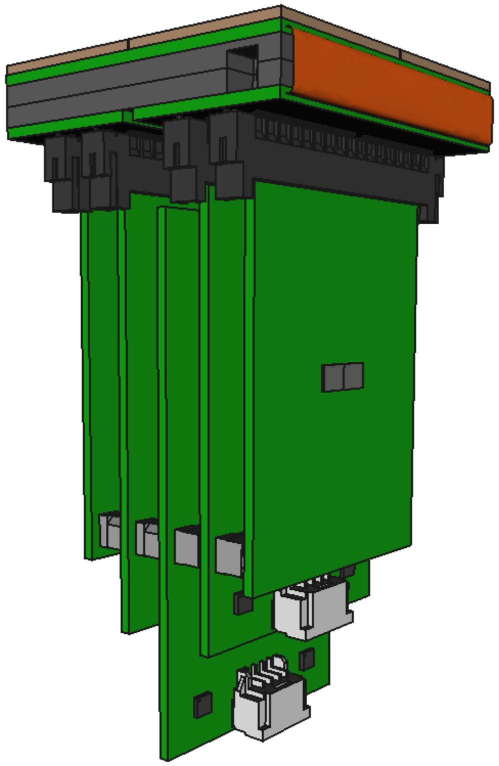


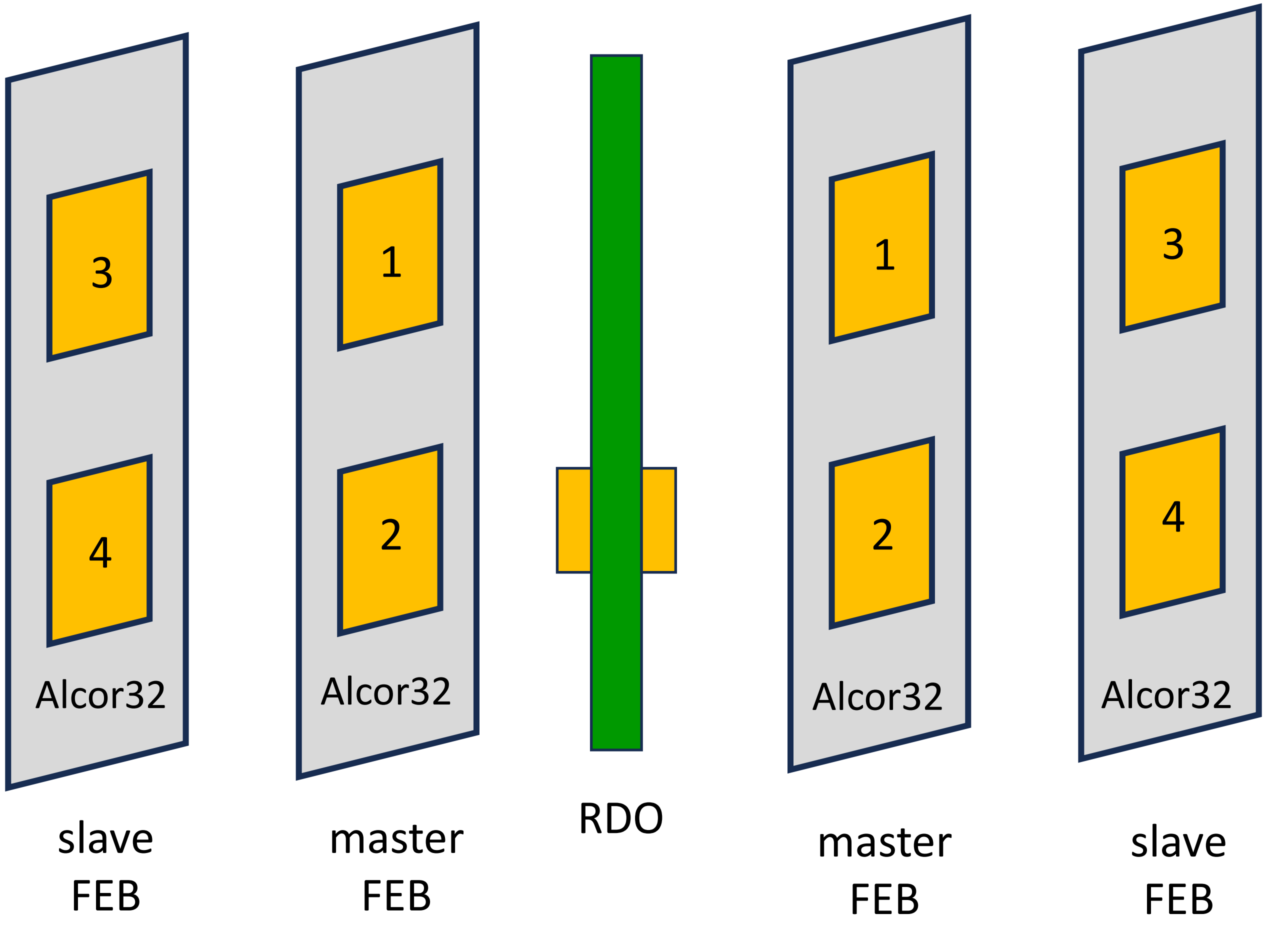
When ALCOR64 is ready



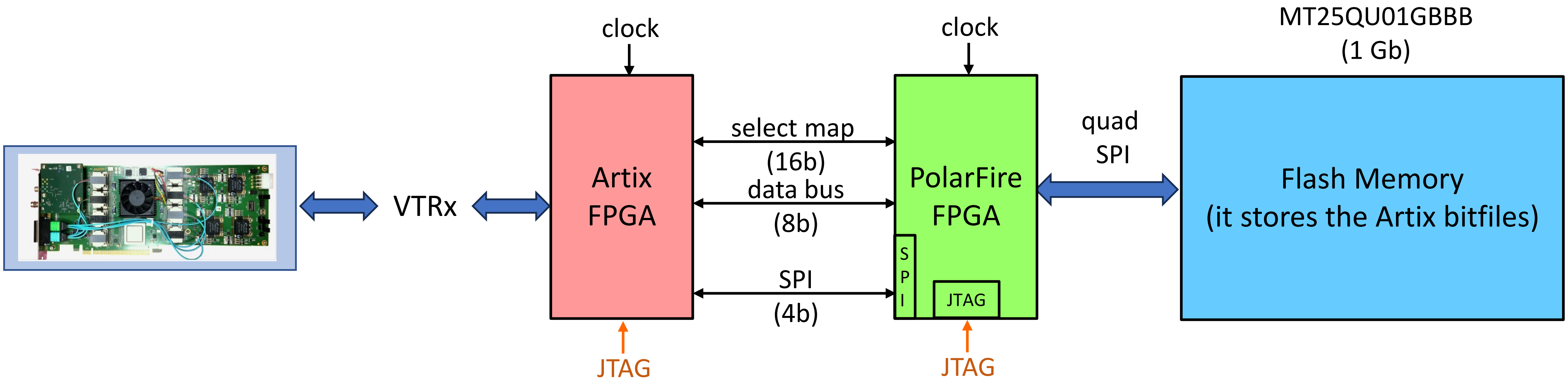


In a first stage



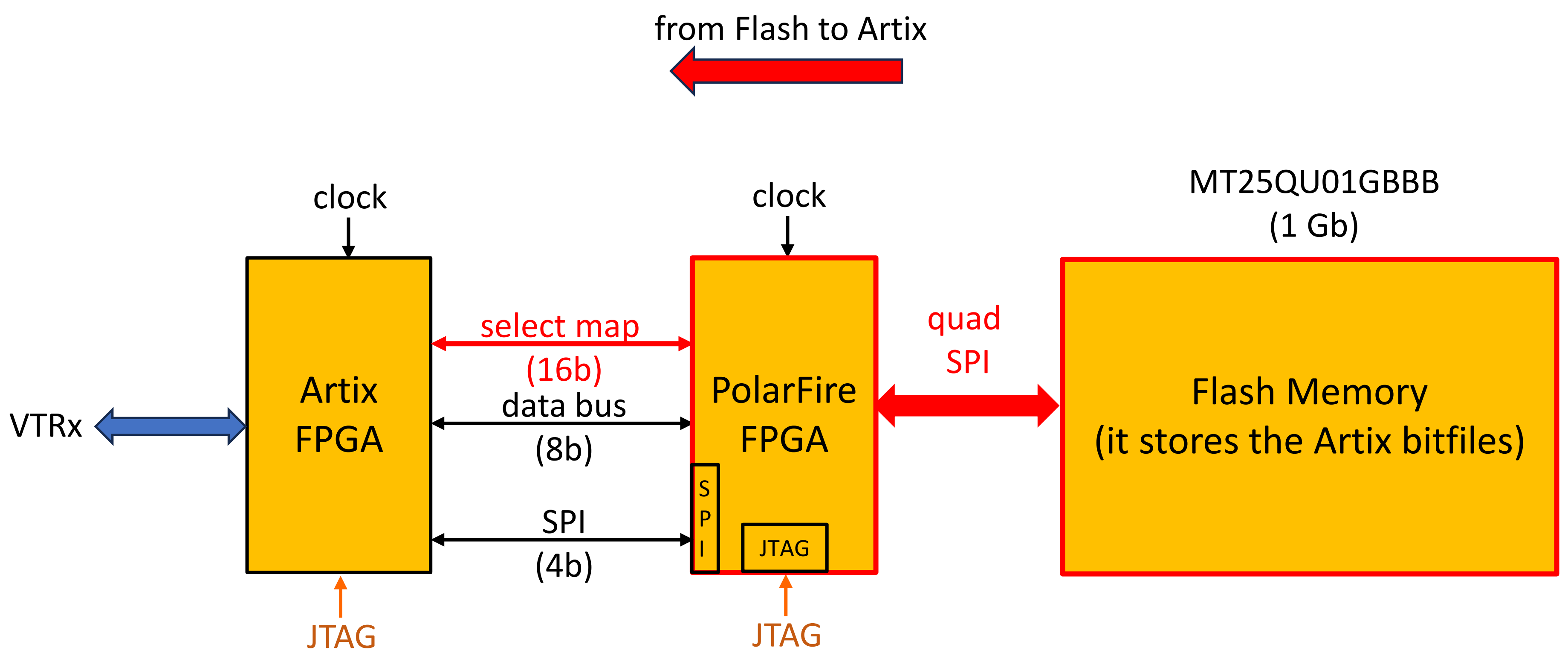


How to program the FPGAs



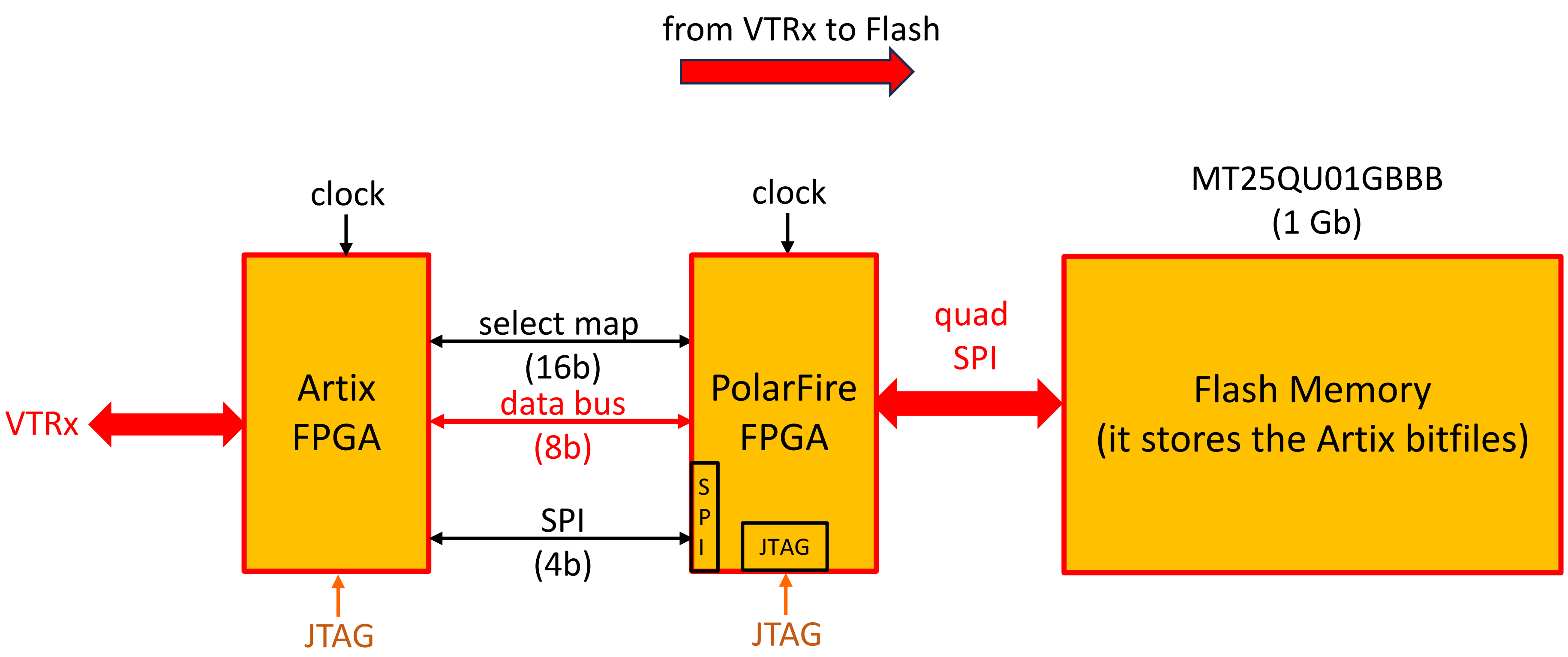
- JTAG ports are available to easily program the FPGAs during the first lab tests
- FPGAs and FLASH memory need to be remotely programmed when needed

How to program the FPGAs



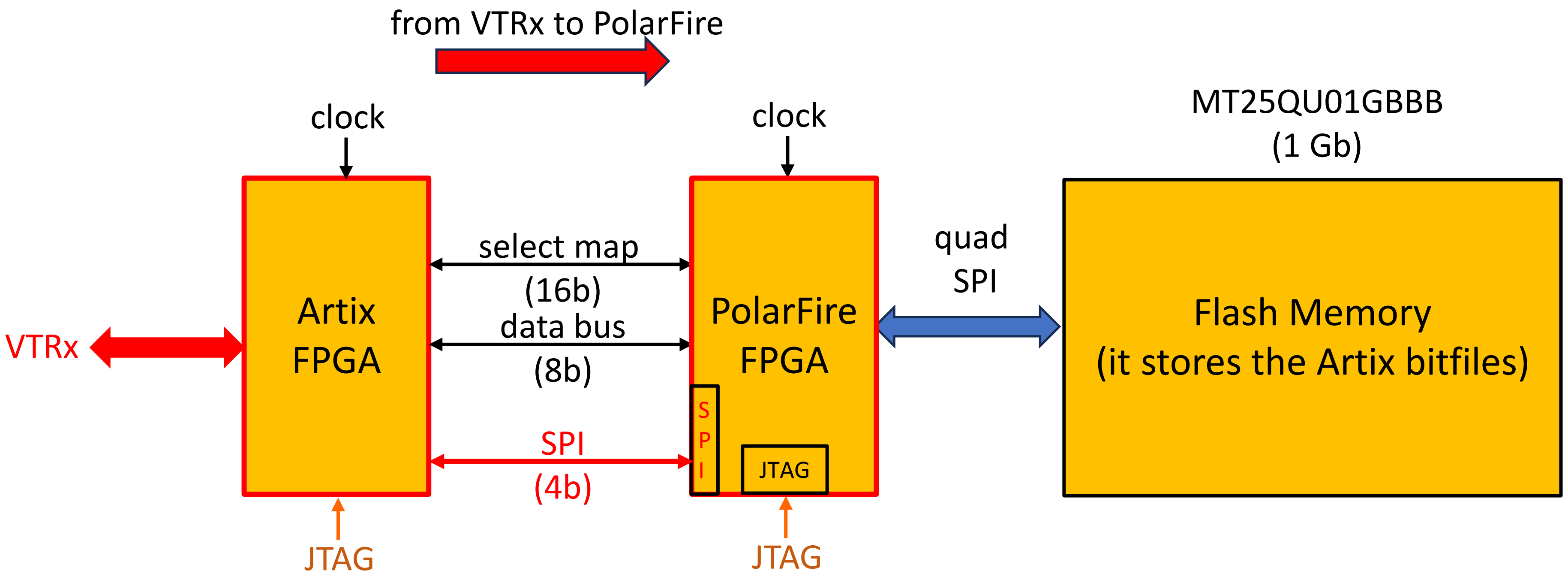
Step 1: Artix Ultrascale+ programming from Flash

How to program the FPGAs



Step 2: programming the Flash memory

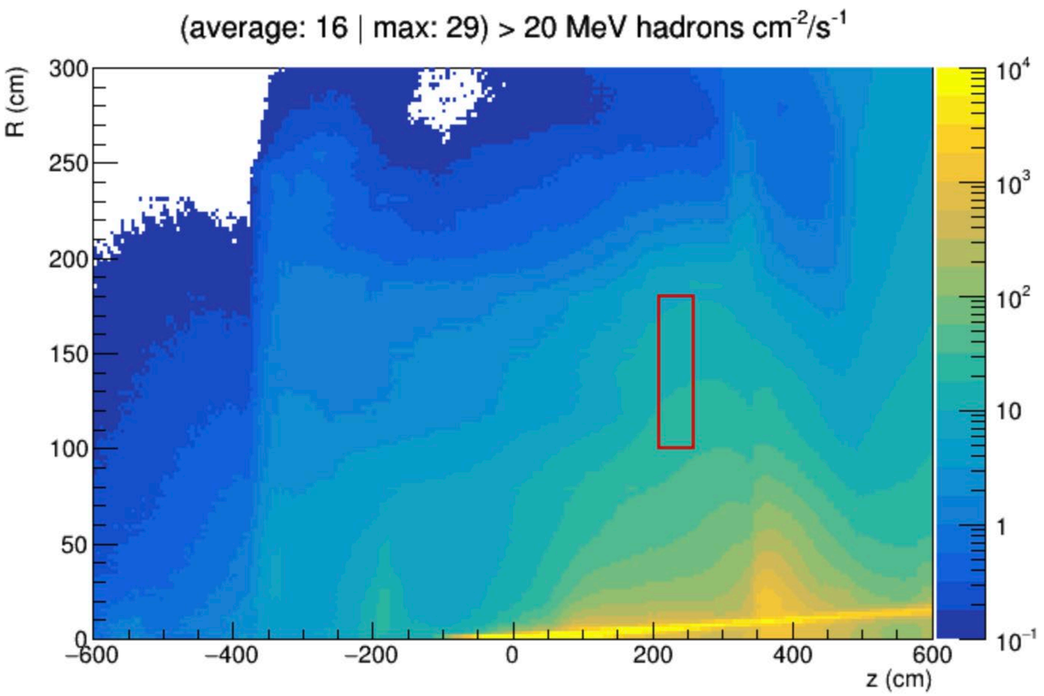
How to program the FPGAs



Step 3: programming the PolarFire

SEU rates

Xilinx declares 2.67 × 10^{-16} cm^2/bit cross-section for CRAM bits
AUP15 has 42.8 × 10^{+6} configuration bits
dRICH flux (hadrons > 20 MeV): 200 $cm^{-2}s^{-1}$ (safety factor: 5)



1 SEU every 4.3x105 s/FPGA

1 SEU every 3.5x10^2s/dRICH

1 SEU every 6 minutes in whole dRICH

- SEU rate (if confirmed) seems manageable
- a scrubber might not be strictly needed
- RDO final design to be validated with a full irradiation test