FPC設計の試み

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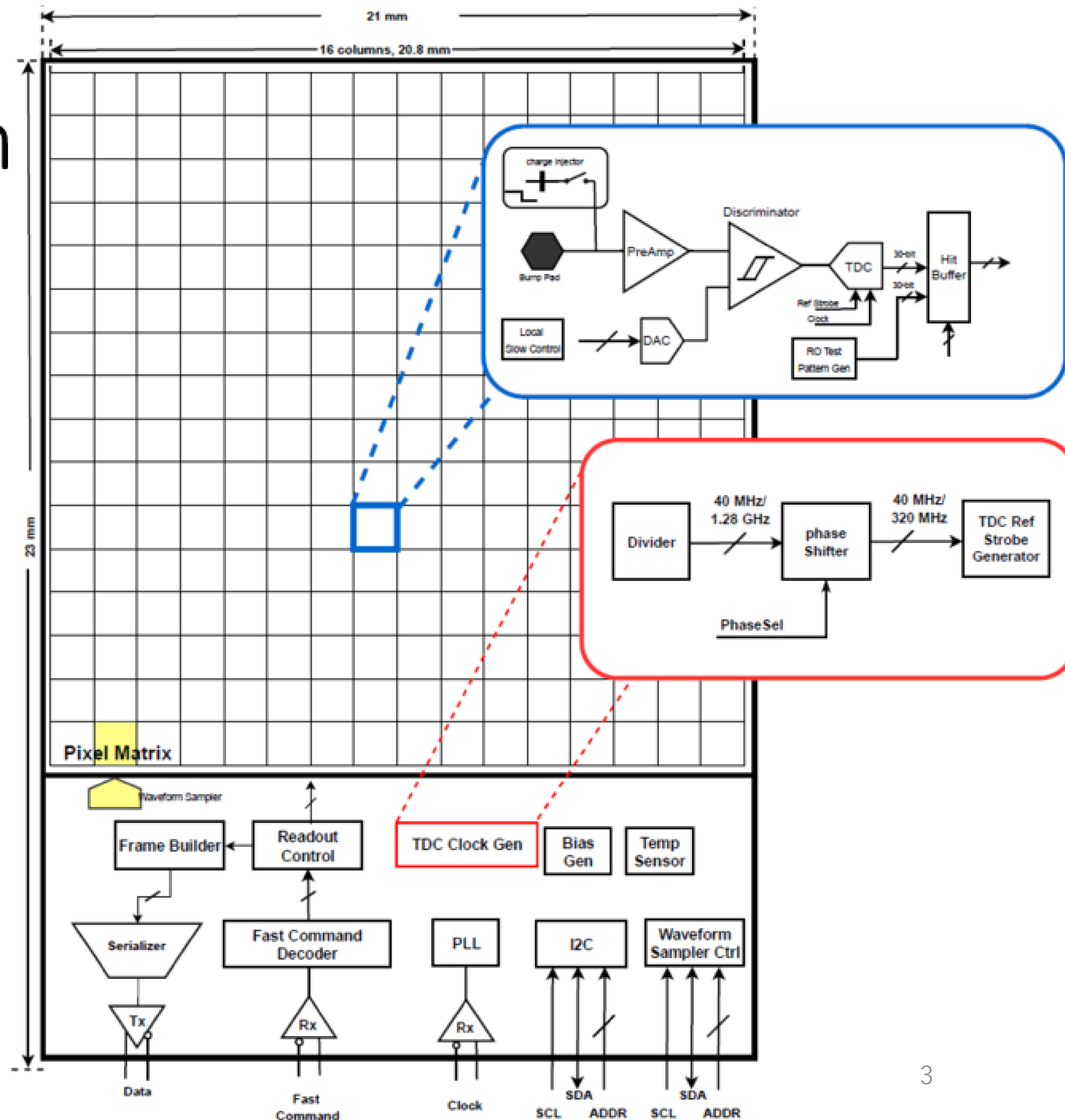
FPCの試み

- BTOFの構造
  - 表裏構造：
    - 各面にセンサー＋ASIC
    - 各面にFPC
- Sensor
  - 64x2 strips = 3.2 x 2 cm^2
    - (0.5mm x 1cm)
- ASIC
  - ETROC (CMS- pad LGAD用)を想定
    - 21x23mm^2
    - 128 signals – IN : Bump bonding
    - 信号線: 31 lines (28? 必要なのは19？)
    - 電源・GND　40

ETROC2 overall design

- 16 x 16 pixels, size 1.3 x 1.3 mm^2,match LGAD sensor.
- Analog Front-end (PA+Discriminator)+TDC
- L1 trigger-driven readout
- Flexible trigger path for trigger/test
- Fast waveform sampling for one pixel
- Interface of ETROC:
  - 40 MHz reference clock
  - I2C slow control
  - 320 Mbps fast control
  - Two serial data output at 320/640 Mbps
- Time resolution contribution: < ~40 ps
- TSMC 65nm CMOS process, 1p9m
- Power: 1 Watt/chip @ 1.2V
- 100 MRad TID tolerance, SEE protection for control/readout



- ETROC signal lines
  - RX: CLK (40MHz ref, LVDS)
  - RX: I2C (slow control, 2 lines)
  - RX: Fast Command (320Mbps LVDS)
  - RX: Addr (5bits I2C)
  - TX: Data (320Mbps, LVDS)
  - TX: Temp out
  - RX : Signal (from Sensor, bump bonding)
- ETROC Power
  - LV(Digital, Analog) たくさん
  - GND (Separate? Common?)

- センサー
  - HV
  - GND (Common?)

Prithwish Tribedy から 全員 へ

PT: connections:
1．I2C
2．CLK
3．HV
4．LV
5．GND
6．Data

PT: pls. see my list before, I might have missed something : I2C, CLK, HV, two LV, data

let's follow up offline

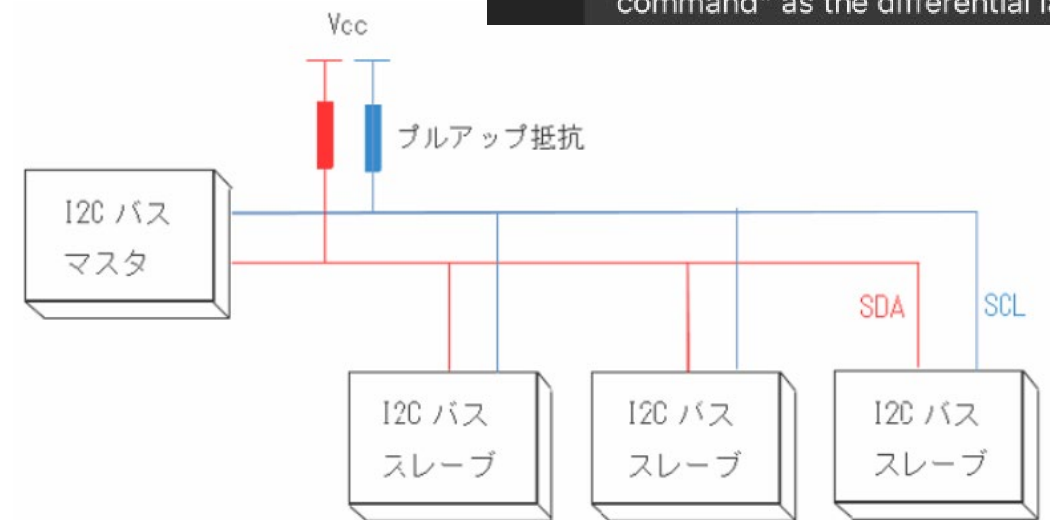
Kentaro Kawade から 全員 へ

KK: OK

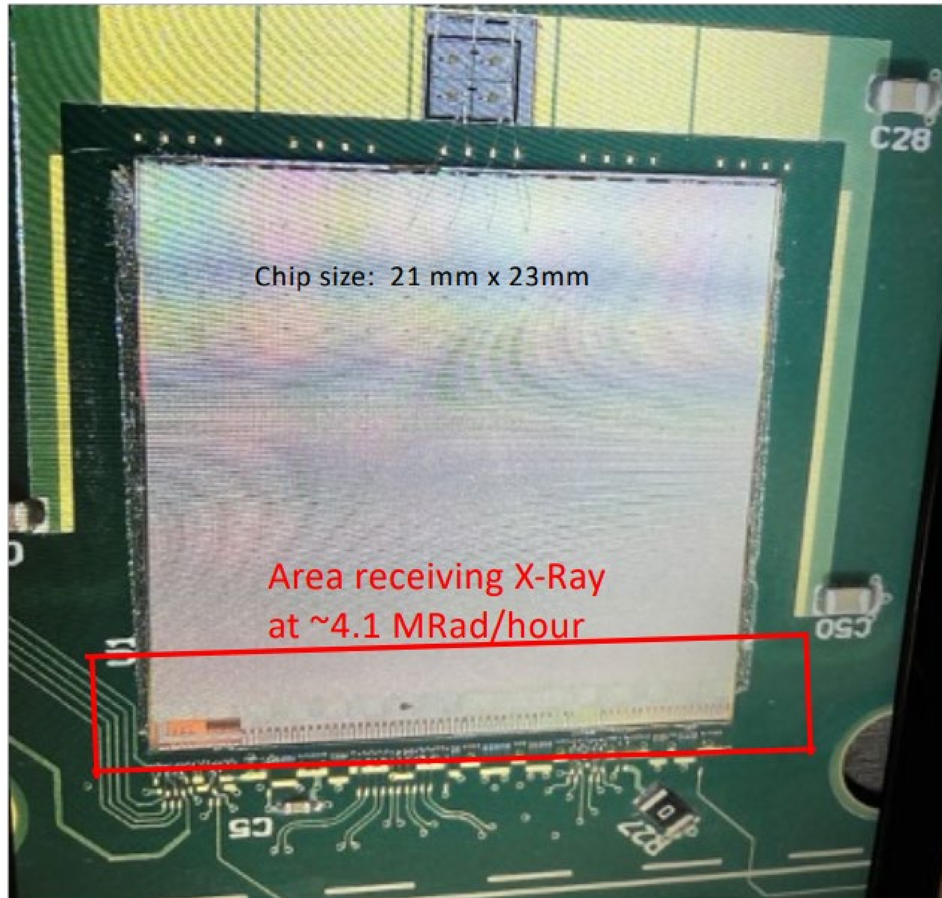
Tonko Ljubicic から 全員 へ

TL: Per ASIC: 3 differential lanes, 2x I2C, at least. Perhaps 1-2 more for sensors etc.

Prithwish, you missed "fast command" as the differential lane.

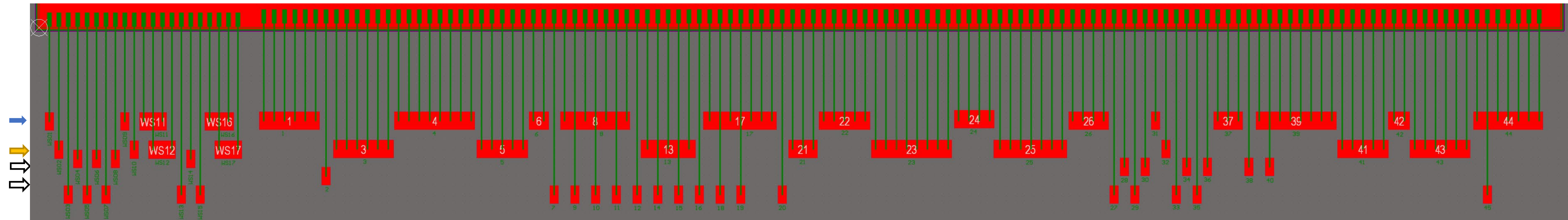


ETROC2 test board



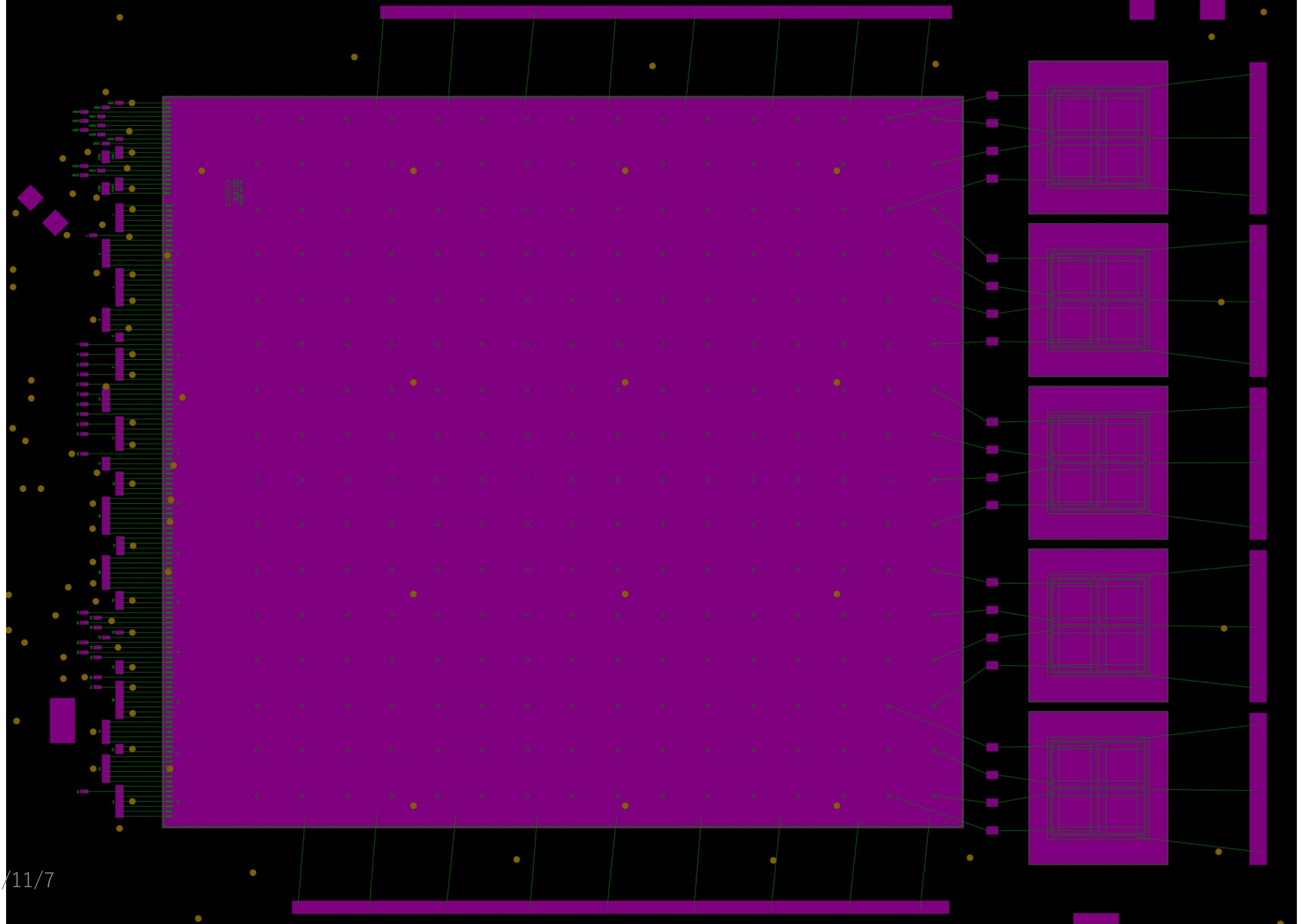
- https://indico.cern.ch/event/1255624/contributions/5445274/attachments/2724858/4735205/ETROC2-TWEPP-2023-poster-v5.pdf

ETROC2 bonding diagram



- One row of 17 PCB pads are ground
- One row of 13 PCB pads are power supplies
- Two rows of 31 PCB pads are signals, pin#40 is GND

Smallest PCB pad size : 5x10 mils
Smallest PCB pad pitch : 10.236 mils (0.26 mm)
Smallest bonding distance : 1.4 mm
Longest bonding distance : 2.451 mm



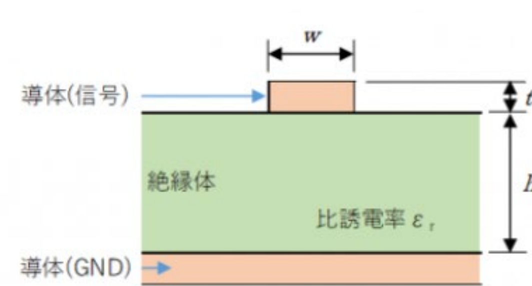
ETROC2					
PCB pin#	Pin name	Die pad#	PCB pin#	Pin name	Die pad#
1	VSS_A	1-6	23	VDD_D	60-67
2	VREF	7	24	VSS_D	68-71
3	VDD_A	8-13	25	VDD_D	72-78
4	VSS_A	14-21	26	VSS_D	79-82
5	VDD_A	22-26	27	**I2CAddr0**	83
6	VSS_A	27-28	28	**I2CAddr1**	84
7	**CLK40p**	**29**	29	**I2CAddr2**	85
8	VSS_D	30,32,34,36	30	**RSTn**	86
9	**CLK40n**	31	31	VSS_D	87
10	**~~CLK1280p~~**	33	32	VDD_D	88
11	**~~CLK1280n~~**	35	33	**SCL**	89
12	**FCp**	37	34	**SDA**	90
13	VDD_D	38,40,42	35	**I2CAddr3**	91
14	**FCn**	39	36	**I2CAddr4**	92
15	**DOLp**	41	37	VSS_D	93-95
16	**DOLn**	43	38	VDD_EFUSE	96
17	VSS_D	44,46,48-50	39	VSS_A	97, 99-104
18	**DORp**	45	40	VSS_AO	98
19	**DORn**	47	41	VDD_A	105-109
20	**VP**	51	42	VSS_A	110-111
21	VDD_D	52-54	43	VDD_A	112-117
22	VSS_D	55-59	44	VSS_A	118,120-124
			45	**VTemp**	119

~~Wave Sample~~		
PCB pin#	Pin name	Die pad#
WS01	DVSS	WS01
WS02	DVDD	WS02
WS03	**ADDR4**	WS03
WS04	**ADDR3**	WS04
WS05	**ADDR2**	WS05
WS06	**ADDR1**	WS06
WS07	**ADDR0**	WS07
WS08	**WR_EN**	WS08
WS09	DVSS	WS09
WS10	DVDD	WS10
WS11	AVSS	WS11,WS13
WS12	AVDD	WS12,WS14
WS13	**SCL**	WS15
WS14	**SDA**	WS16
WS15	**RSTn**	WS17
WS16	AVSS	WS18,WS20
WS17	AVDD	WS19,WS21

PCB-DIE pin map

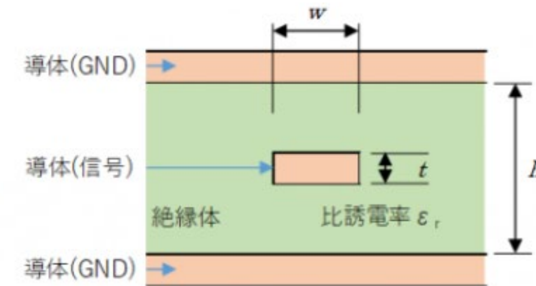
Technology limits

- FPCのサイズ制限
  - 長尺FPC　(INTTの経験)
    - FPCサイズ　130cm x 50cm
      - プリント電子(株)様が特大露光機を所有
    - Line & Space = 130um x 130um
  - 通常のFPC
    - FPCサイズ　50x50cm^2
      - 露光機のサイズで決まっている。
    - Line & Space = 50um x 50um が可能
- インピーダンス制御
  - ストリップライン法：　ラインをGNDで挟む。　外来ノイズに強い。
  - マイクロストリップライン法：　GNDは下だけ。
- 長尺になることによる課題
  - インピーダンス制御のために厚い誘電体が必要　←　時代と逆行
  - 液晶ポリマーへのスルーホール用穴あけ、メッキの困難
  - 積層時の基材の熱縮小によるスルーホール位置の制御
  - 積層時の圧着装置のサイズ制約による圧着のよれ



$$Zo = \frac{87}{\sqrt{(\varepsilon_r + 1.414)}} \times \ln \frac{5.98h}{0.8w + t}$$

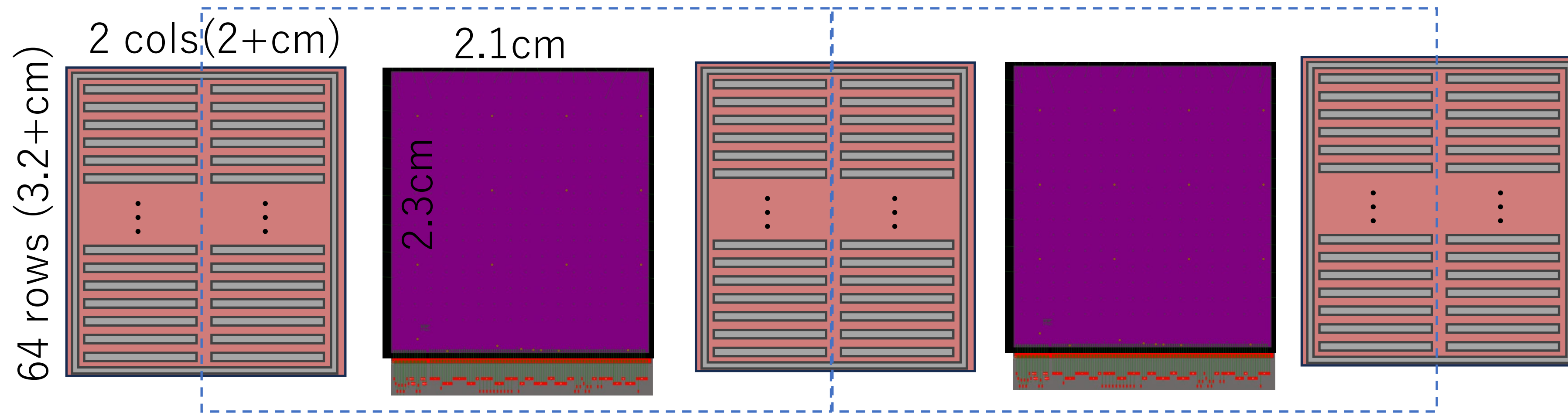
図１．マイクロストリップライン断面図



$$Zo = \frac{60}{\sqrt{\varepsilon_r}} \times \ln \frac{4h}{0.67\pi w \left(0.8 + \frac{t}{w}\right)}$$

図２．ストリップライン断面図

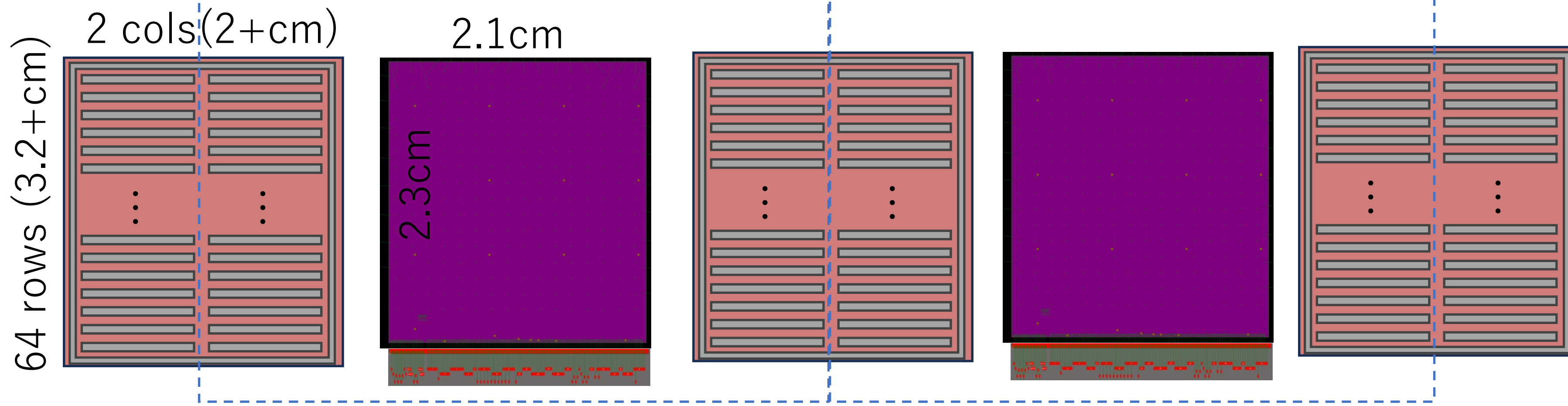
配置例

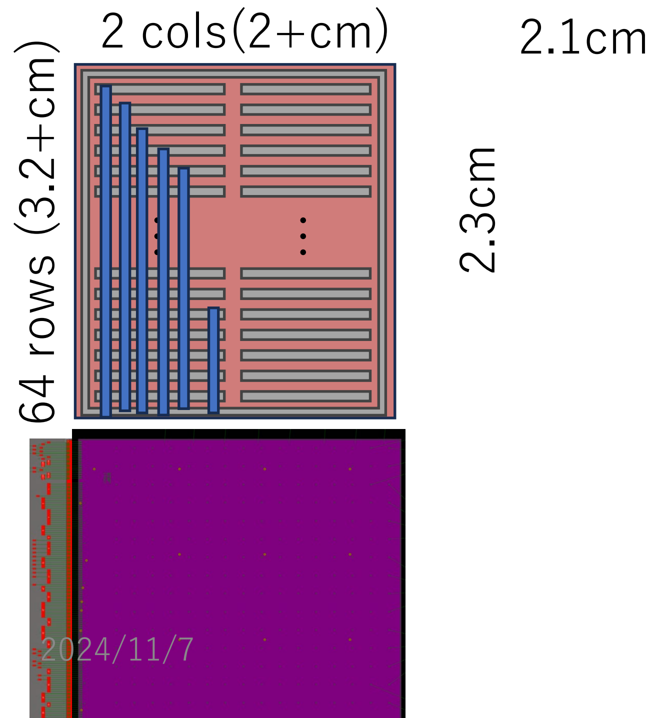


- ASIC(ETROC2)とセンサーのサイズがほぼ同じ：隙間なく配置できるのか？
- モジュール構造ができない: ハードウェアの切れ目と接続の切れ目がずれてる

配置例

ASIC縦置き



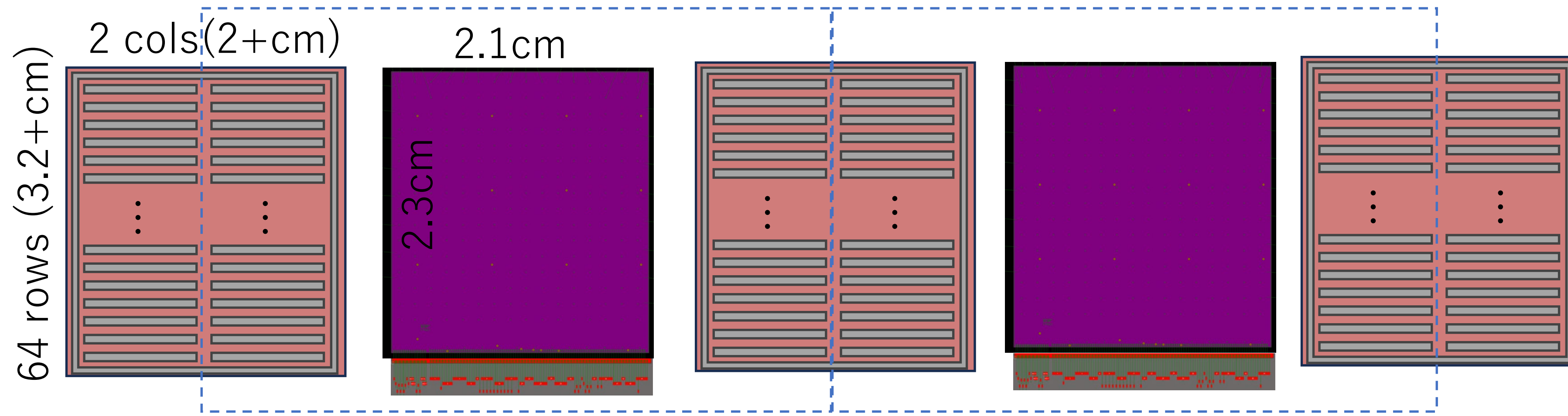


2.1cm

2.3cm

配置例

ASIC縦置き



- ASIC(ETROC2)とセンサーのサイズがほぼ同じ：隙間なく配置できるのか？
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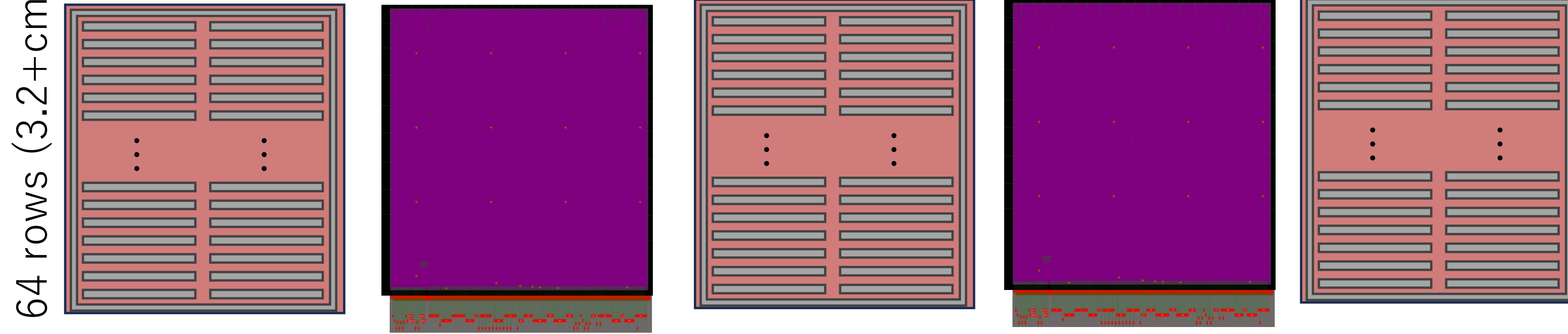
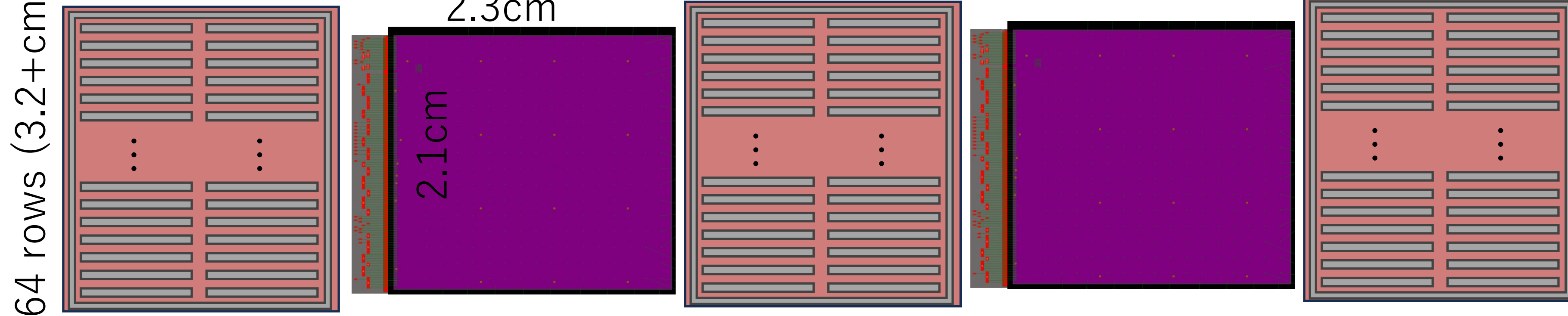
ASIC縦置き



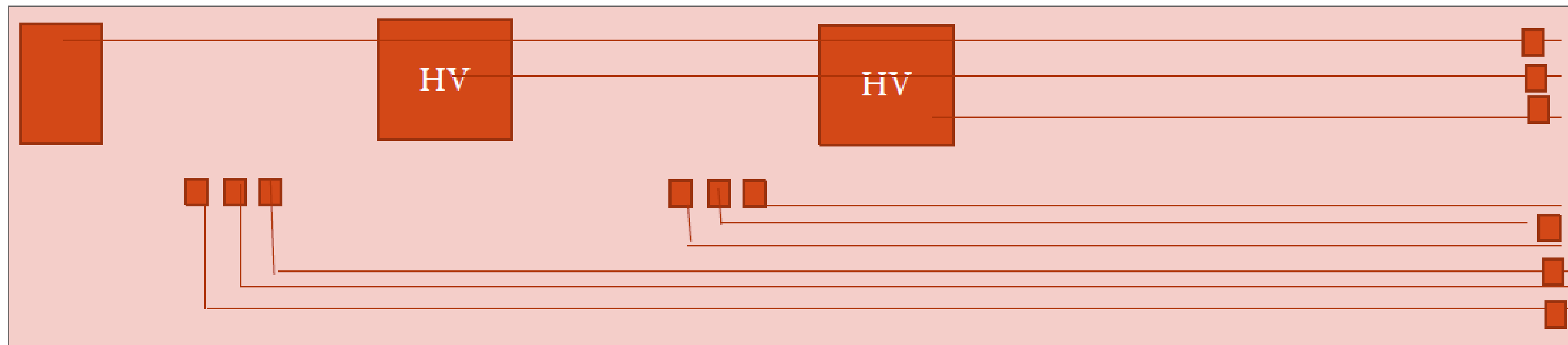
配線の取り回しが難しい(できない)

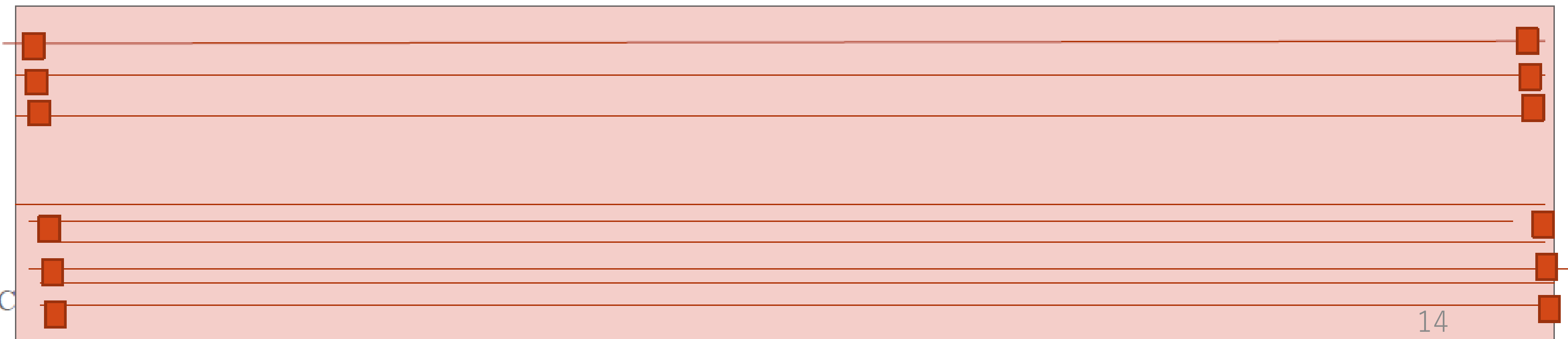
ASIC横置き



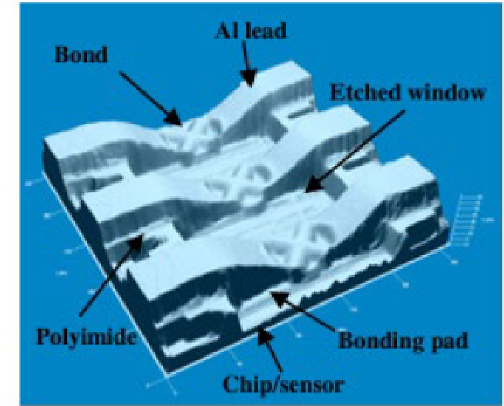
FPC idea

- Build two type of 2 layer (channels and ground) FPC 'connection' and 'extension'
- Each 'connection' FPC service a number of ASICs that fit in a single plane

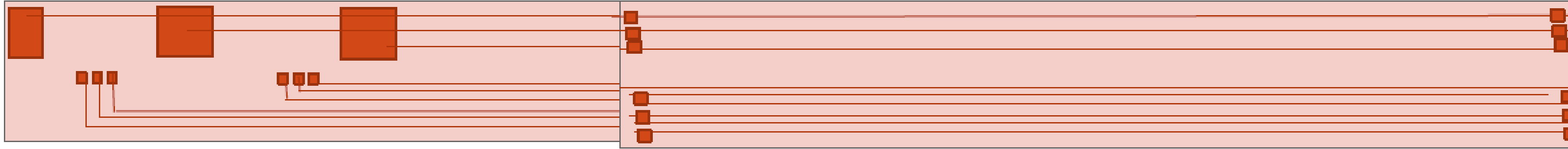




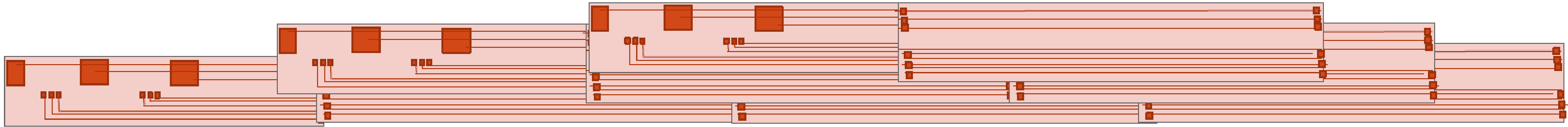
FPC idea



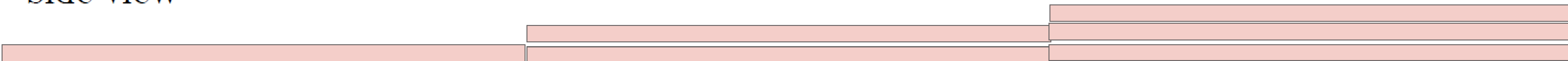
- FPCs are spTAB bonded to be extended so it's flush



- Flex are stacked and glued on the stave one on top of the other to service the entire stave

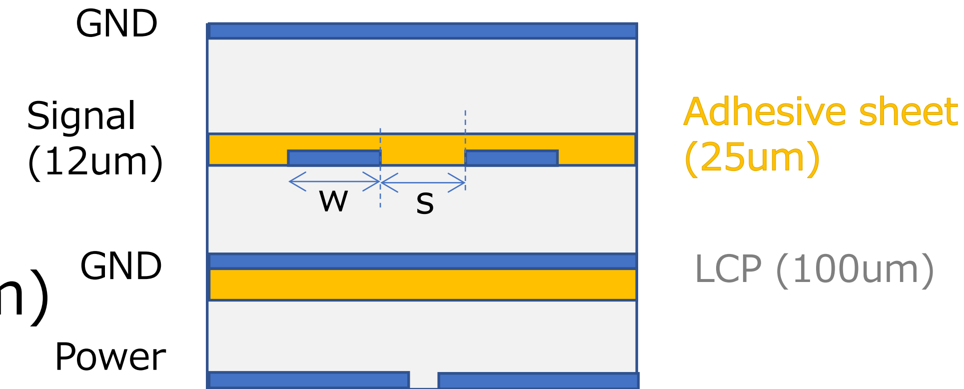


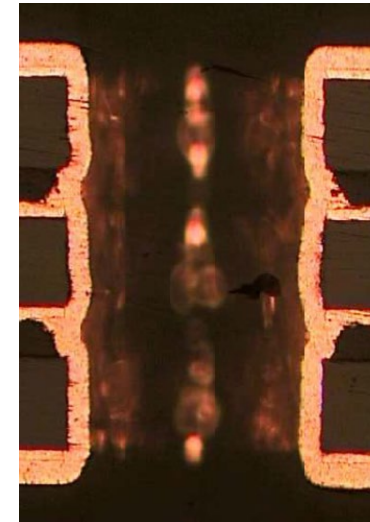
- Side view



BEX

- Cable design (prototype)
  - Dimension (L x W): 120 x 5 cm^2
  - 4 layers (signal , 2xGND, PWR): $X = 0.8\% X_0$
    - Cu : 12um thick per layer + 30 um Cu plating on surface
  - Lines : 124 lines (Line and space : 130 & 130 um)
  - Z_{diff} : 100Ω by strip line structure
    - Signal layer is sandwiched by GND layers
  - Liquid Crystal Polymer (LCP) as substrate
    - Less signal loss due to low di-electric constant & tan(δ)
    - Thick LCP available for Z_{diff} : 100um

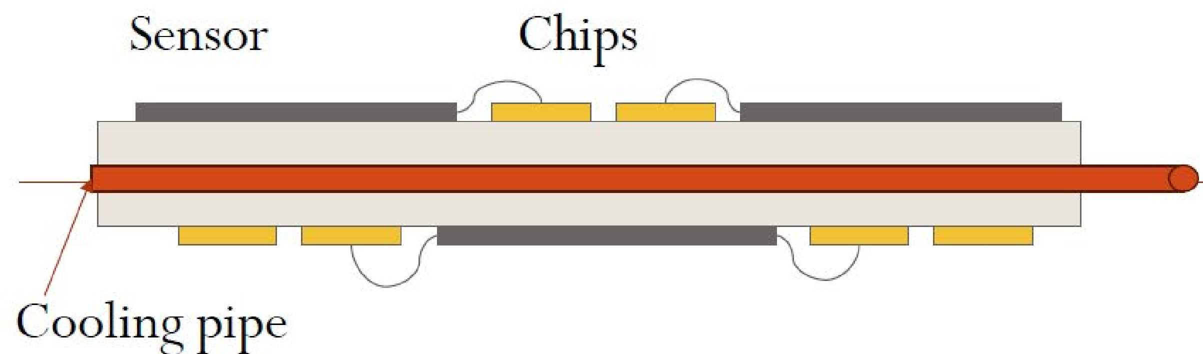


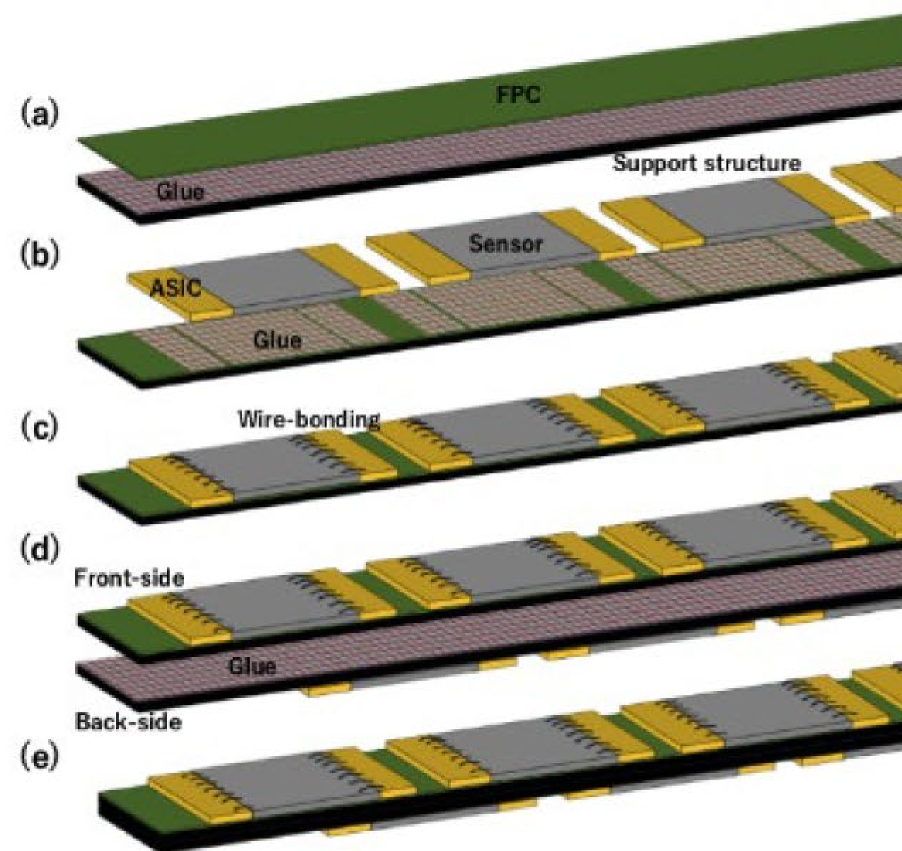


From Simone's slide

Double-sided design

- "Original": 2 ASIC per sensor originally, now 1 ASIC per sensor
  - 1 ASIC service two half sensor

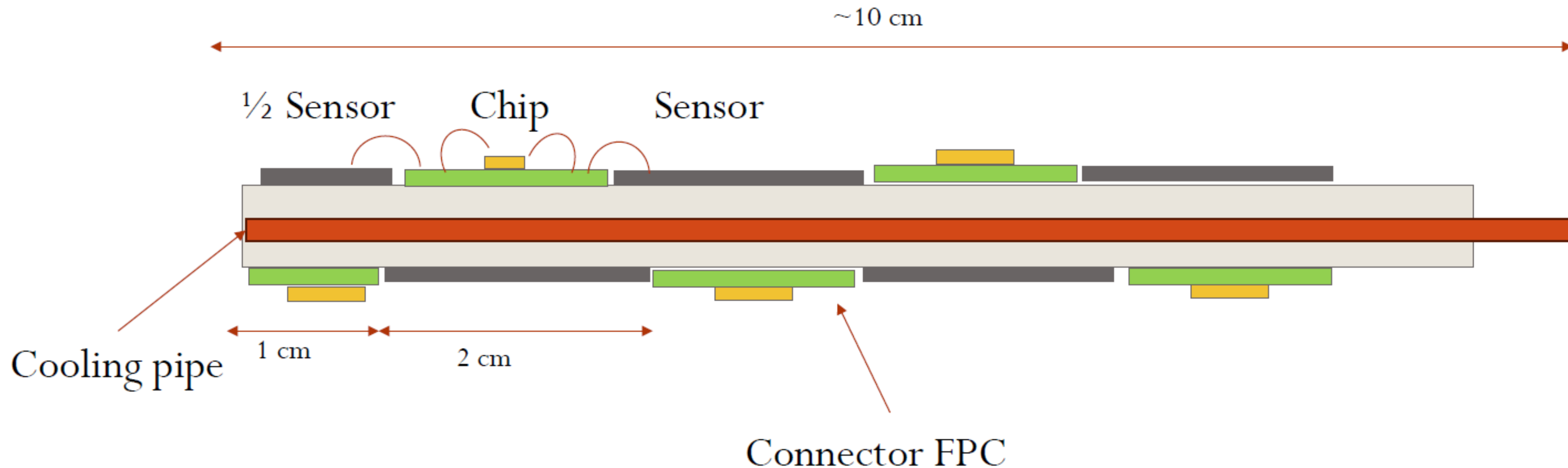


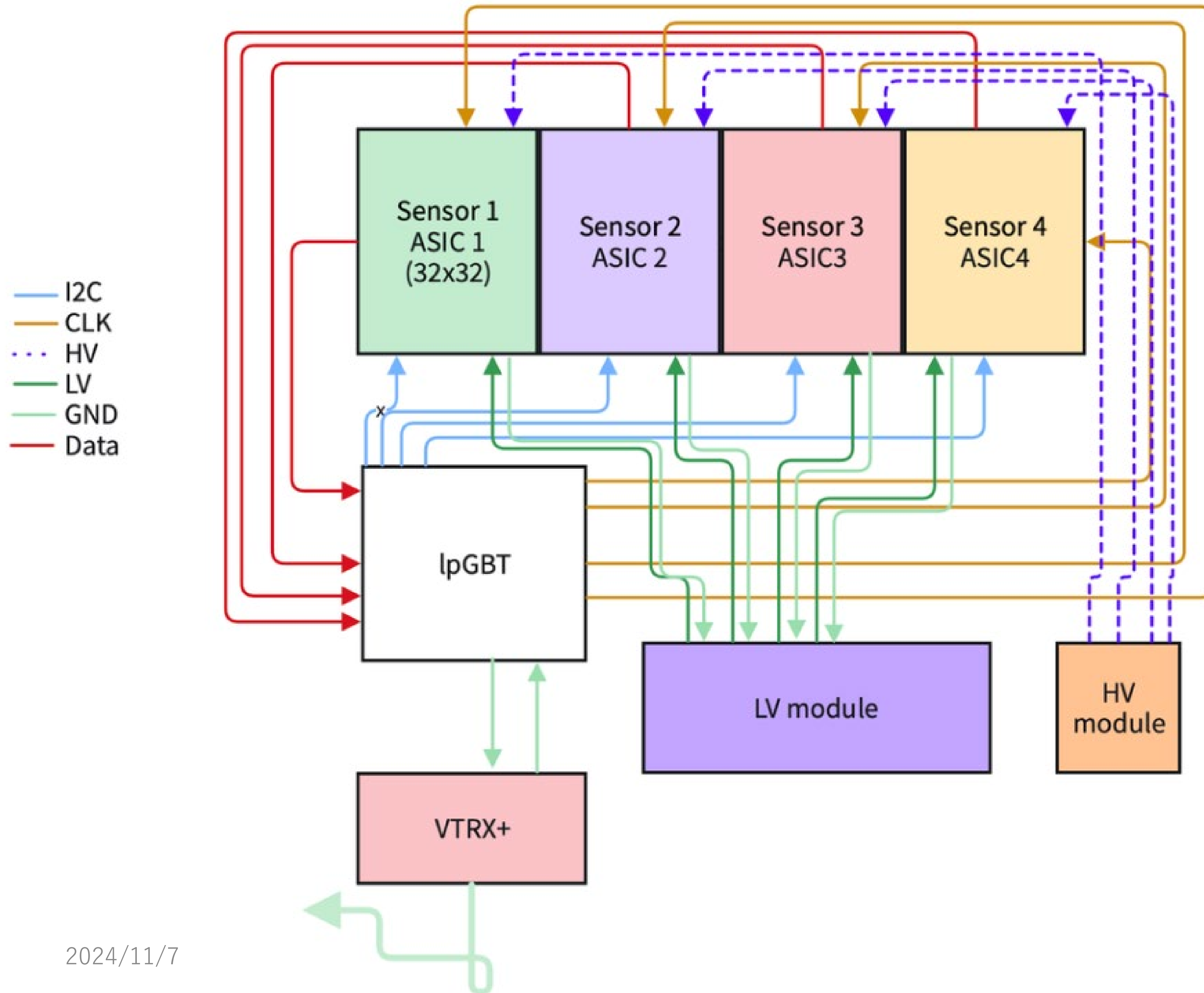


From Simone's slide

Double-sided design

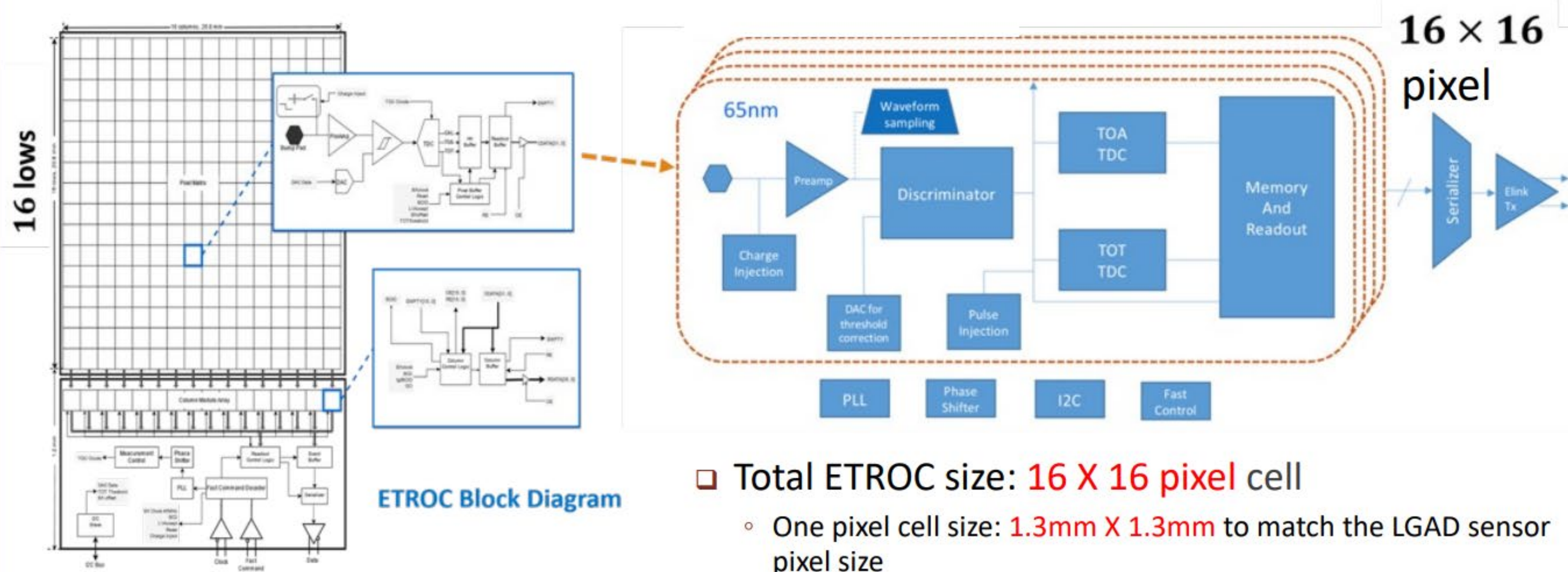
- Since last discussion two changes:
  - 1 chip between two sensors
  - "Connector" board to match sensor/chip pitches, sensor and chip wire bonded to it and the connector is wire bonded to the FPC




I2C
CLK
HV
LV
GND
Data
Sensor 1
ASIC 1
(32x32)
Sensor 2
ASIC 2
Sensor 3
ASIC3
Sensor 4
ASIC4
x
lpGBT
LV module
HV
module
VTRX+

ETROC

- ETROC is a ASIC for CMS – Endcap Timing Layer w/ LGAD

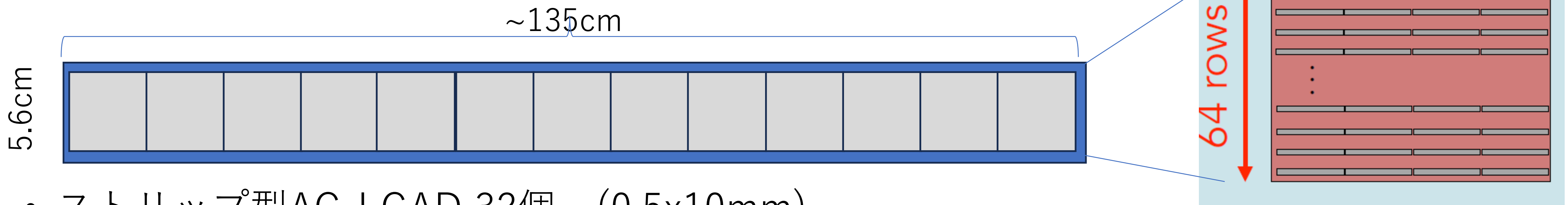


- Total ETROC size: 16 X 16 pixel cell
  - One pixel cell size: 1.3mm X 1.3mm to match the LGAD sensor pixel size
- Targeting signal charge (1MIP): ~6 fC
- TDC (time-to-digital converter) range
  - ~5 ns TOA (time of arrival)
  - ~10 ns TOT (time over threshold)

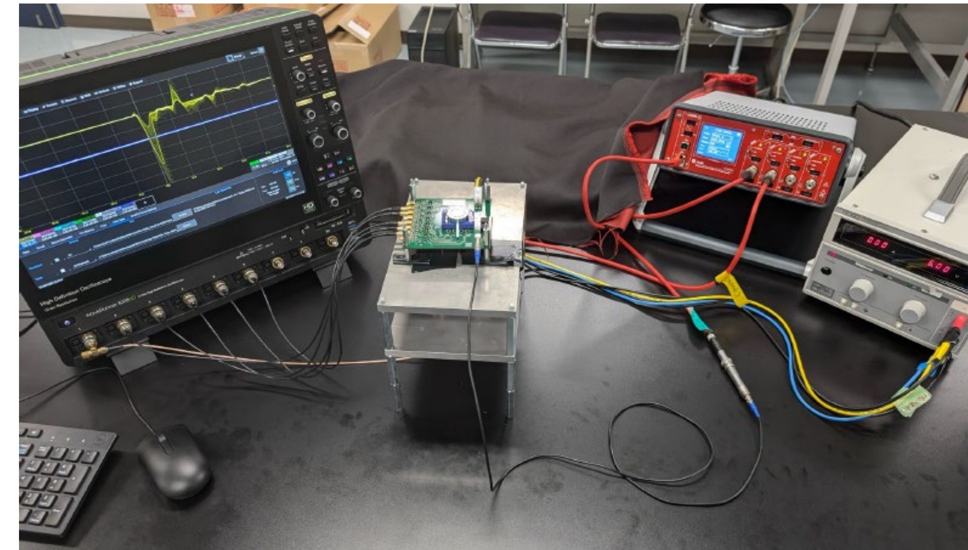
PCBデザインの制約

- 部品面のデザイン
  - センサーの裏面は銅箔
  - ASICの裏面は銅箔：　熱を逃がすため。　GNDはピンから
  - ASIC間の接続は？
  - (少し)パタンが必要：ChipID、Power, GND,

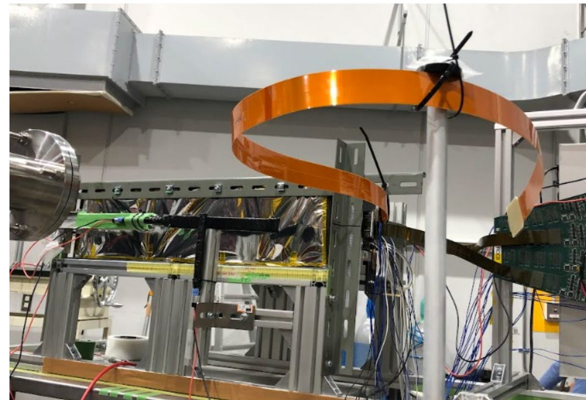
Barrel TOF検出器に向けて



- ストリップ型AC-LGAD 32個　(0.5x10mm)
  - 広島大にePIC-TOF(AC-LGAD)テストベンチ構築 (**松谷さん　19aWB102-2**)
  - KEK中村さんにお借りした試作AC-LGAD＋アンプボード



- 長尺FPC～130cm
  - 信号層＋電源層
  - sPHENIXで130cm長尺FPC
  - 多層、高速伝送
  - 剥離耐性、放射線耐性



2025年にフルサイズの試作を目指す