EIC Project – MPGD DSC

Highlights from Readout electronics

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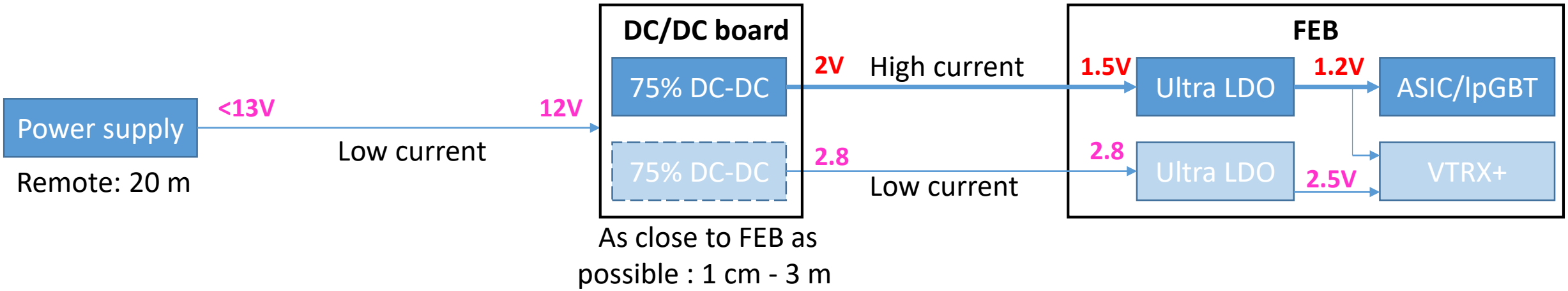
8 November 2024

Caution

- Several evolutions since Tracker and eDAQ TDRs
  - → Generalization of VTRX+ use
  - → Opportunity of lpGBT use
- MPGD groups evaluate impact of these evolutions
  - → A dedicated electronics meeting planed beginning of December
- Information provided in this document is based on the following assumptions
  - → All MPGD FEBs are 256-channel units
    - 4 Salsa ASICs per FEB
  - → FEB electrical-optical interface is VTRX+
  - → lpGBT use is considered
    - Low impact on power consumption
    - Does not change number of optical cable assemblies per FEB
  - → FEBs are equipped with linear low dropout voltage regulators (LDO)
  - → Magnetic field tolerant (bulky) DC/DC voltage regulators are placed somewhere – as close to FEBs as possible
    - Place yet to be determined depending on DC/DC board design and dimensions
- Reminder : there are 640 FEBs
  - → 128 for CyMBaL with electron and hadron side access
  - → 128 for µRWell-ECT with electron and hadron side access
  - → 384 for µRWell-BOT
  - → Common design with form-factor adaptation per detector type

Low Voltage - How many cables coming from MPGDs?

- A 256-channel FEB board needs high current 1.5V power and low current power > 2.8V



- Option 1: DC/DC boards within the vicinity of detector modules
  - → Low current 10-12 volts delivered to detector module
  - → Cable harness with two power cables and two sense wires
    - Alpha Wire 2424C : commercial harness including shield and coating : ø = 6 mm

- Option 2: DC/DC boards outside the detector modules
  - → DC/DC board input cable harness : same as in option 1
  - → FEB input cable harness includes a pair of cables for high current and a pair of cables for low current
    - Harness diameter including shield and coating depends on the FEB – DC/DC distance
    - Ø of commercial products : from 4.6 mm @ 30 cm distance to 6 mm @ 2m distance

DC/DC (and LDO) component count

- MPGDs strongly count on collaboration efforts to reuse ePIC development or to adapt it per detector type
- So far 2 CERN components are considered : bPOL12 and bPOL48
- bPOL12 option : 12V input – 4A current
  - → 2 components per FEB
  - → 640 FEBs : 1400 units including prototyping and quality assurance
- bPOL48 option : 48V input – 8A current
  - → 1 component per FEB
  - → 640 FEBs : 750 units including prototyping and quality assurance
- Reminder: linear regulators need to be accounted if radiation hardness is of concern
  - → Understand if CERN linPOL12 can be available for VTRX+ 2.5V powering
    - Up to 12V input – 25-80 mA output
    - 1 or 2 per FEB
  - → Understand if CMS HgCAL LDO can be available for Salsa, lpGBT and VTRX+ 1.2V powering
    - Up to 2V input – 3A current
    - 2 or 4 per FEB

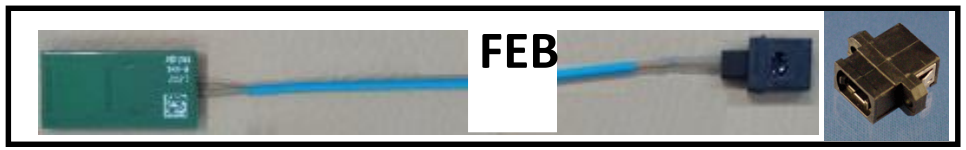
Cooling estimate

- RDO : irrelevant
  - → Either inexistent
  - → Or can be placed anywhere in low restriction area due to FEB – RDO optical interface
- 256-channel FEB : 8.5 W with 25% safety margin
  - → Raw power budget with minimal margin : ~6.8 W
  - → Does not include DC/DC board contribution
    - Design under study within the collaboration - place to be identified
- Heat stability
  - → Usual slow increase with electronics aging : difficult to estimate but tolerated by low power supply margins
  - → Radiation damage : low influence
  - → Temperature : TBD – will be known after measurements on Salsa2 prototype
- Temperature
  - → Operating temperature : no particular constraints within a reasonable ranges : 20-35°C can be considered as baseline
  - → Stability : ±2°C
- Cooling : TBD
  - → Study needs to be initiated

Readout / Data - How many cables coming from MPGDs?

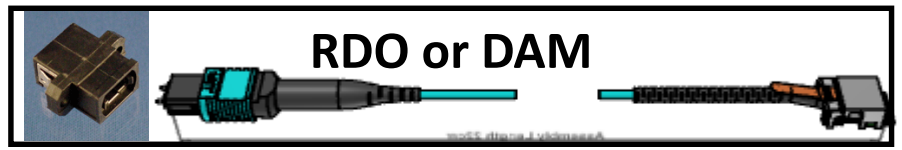
- There is single MPO parallel-optic cable per FEB
  → Whether lpGBT is used or not

- Our approach is to contain VTRX+ pigtail within the FEBs
  → Securing fragile part
- Commercial optical fibers between intermediate patch panels
  → Plenty of choice : will be compatible with the majority of ePIC subdetectors



Short pigtail / on board

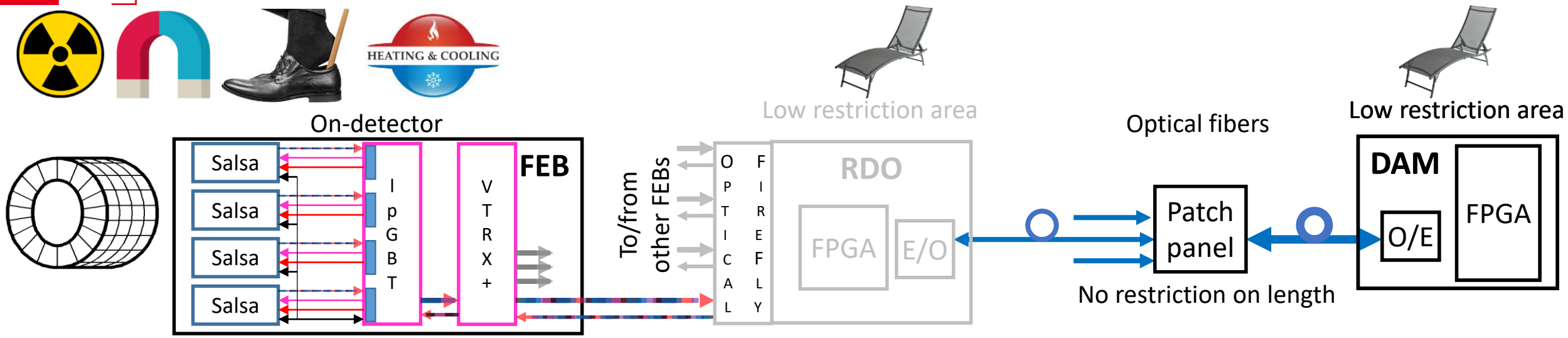
COTS MPO fibers of
adapted length
between patch panels



Short pigtail / on board

Backup

FEB based on Salsa's heterogeneous interface with lpGBT

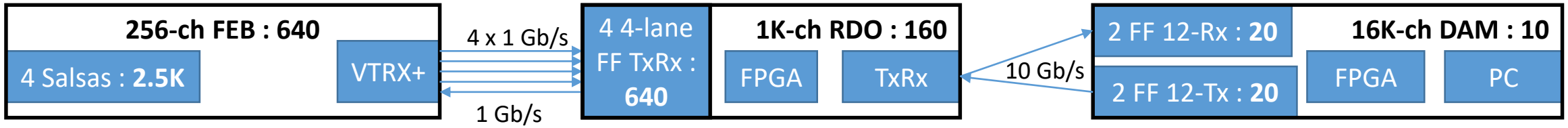


- 256-channel FEB
  - → lpGBT provides a bidirectional interface between 4 Salsas and remote backend FPGA (on RDO or DAM)
    - Clock, fast synchronous commands, asynchronous slow control, physics and calibration data, monitoring
  - → VTRX+ is used with only one TX line
  - → All ASICs are radiation hard

- RDO or DAM : common hardware with FireFly transceivers from Samtec
  - → Placed anywhere in user friendly area
    - No particular restrictions on power consumption, cooling infrastructure, radiation, magnetic field

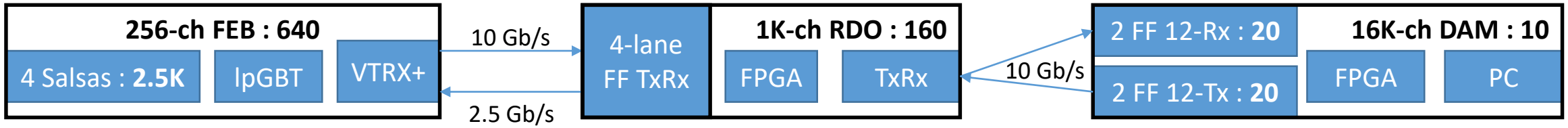
160K-ch MPGD readout configurations and component count

- FEB with direct Salsa-VTRX+ interface



Low density 1 Gb/s grade

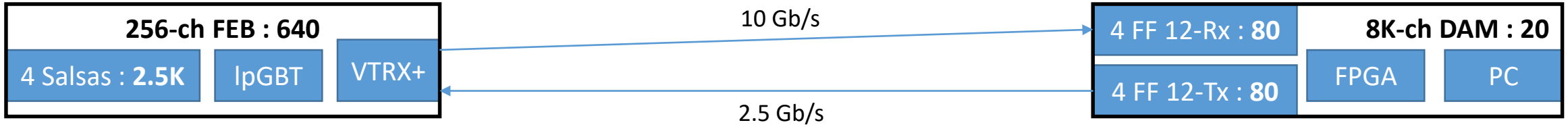
- FEB with lpGBT-VTRX+ interface



High density 10 Gb/s grade

4 times less 4-lane FF

- FEB with direct DAM interface



High density 10 Gb/s grade

No RDOs to design, produce, install, debug and maintain

4 times more 12-lane FF pairs
2 times more DAMs

256-channel lpGBT-based FEB for CyMBaL : dimensions

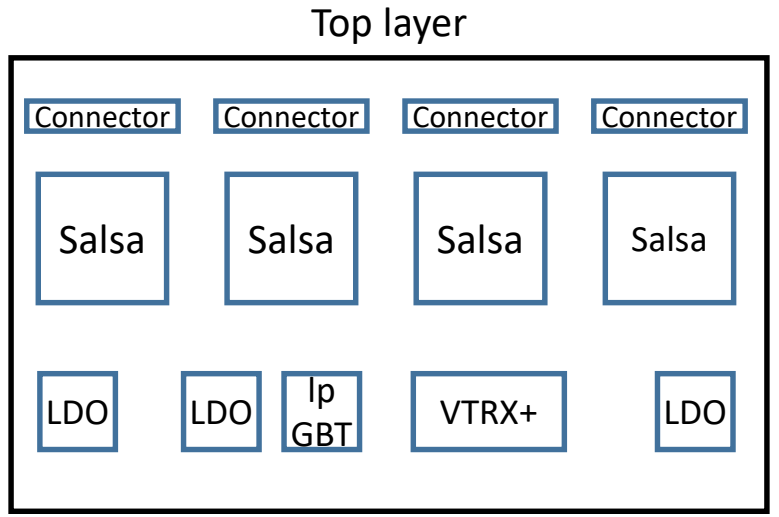
- Assuming 16 x 16 ball 1 mm pitch BGA package for Salsa
- Low profile 40-pin connectors for input signals over micro-coaxial cables
- Active components on both sides of the board

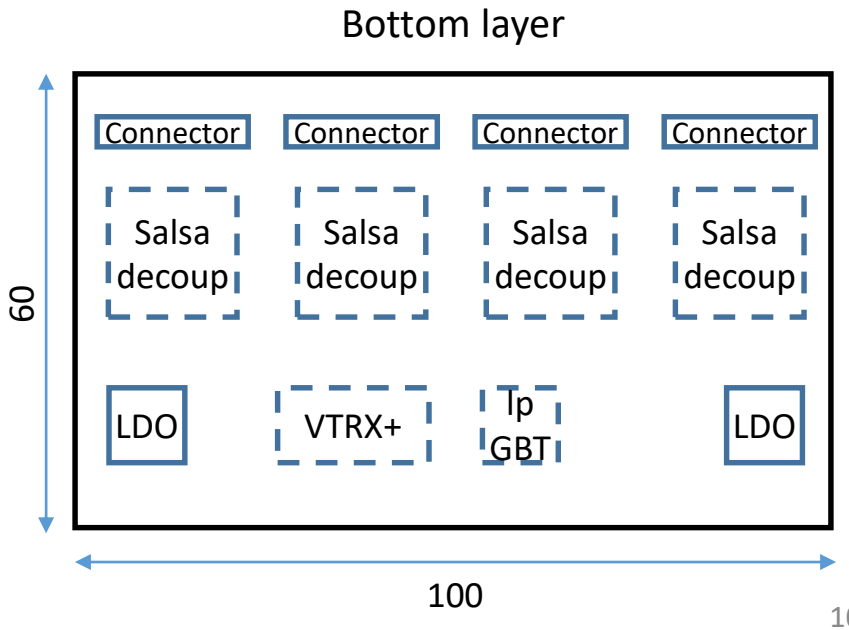
- Length and width give an idea

- Height of the board
  - → Need to accommodate cooling
  - → Need to include mechanical fixture for VTRX+ connector
    - The fragile optical pigtail to be secured within the board

- On-board linear low dropout regulators

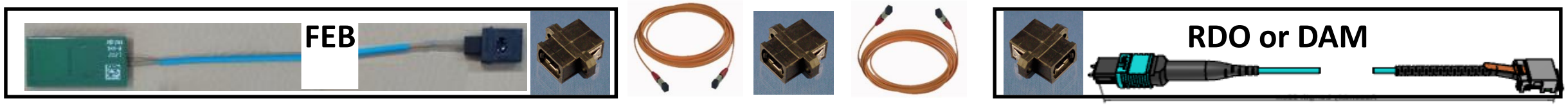
- Radiation-hard magnetic field tolerant DC/DC converters
  - → On a companion board
  - → Count on common collaboration efforts
    - Type, surface including air core, height, shielding, cooling





FEB height : ~10 mm

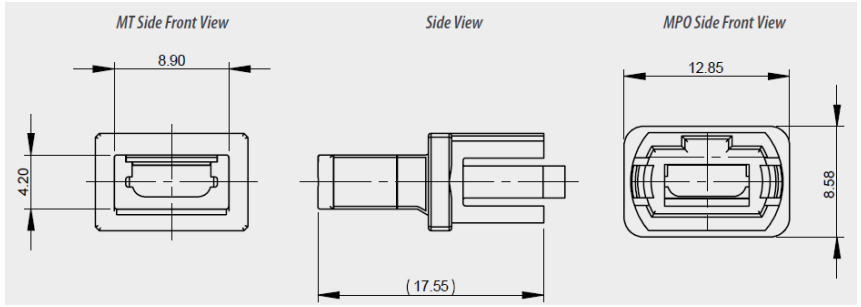
- Protect fragile VTRX+ and its pigtail by containing it within the FEB



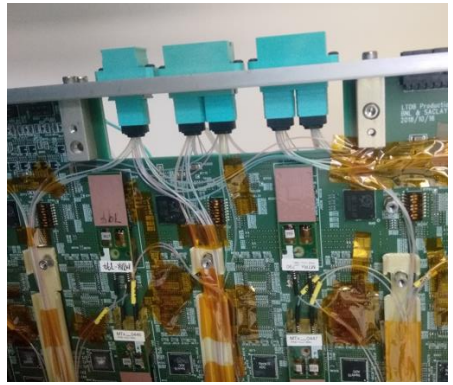
Short pigtail / on board | Fibers of adapted length between patch panels | Short pigtail / on board

→ Common practice for commercial FireFly components in industry and VTRX predecessor in HEP community
→ Can limit pigtail length options to very few if not to 1 value : as small as farthest placement from front panel
  - Potential to have a common pool of VTRX+ components for all subsystems
→ Easier maintenance

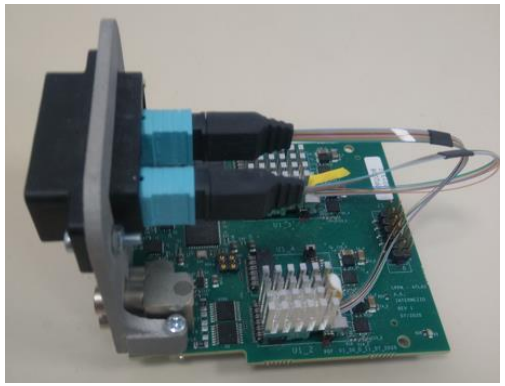
- MT-MPO low-profile adapter from Senko : 7P5-SM-1
  → 8.6 mm height



VTRX example



FireFly example



256-channel lpGBT-based FEB : power

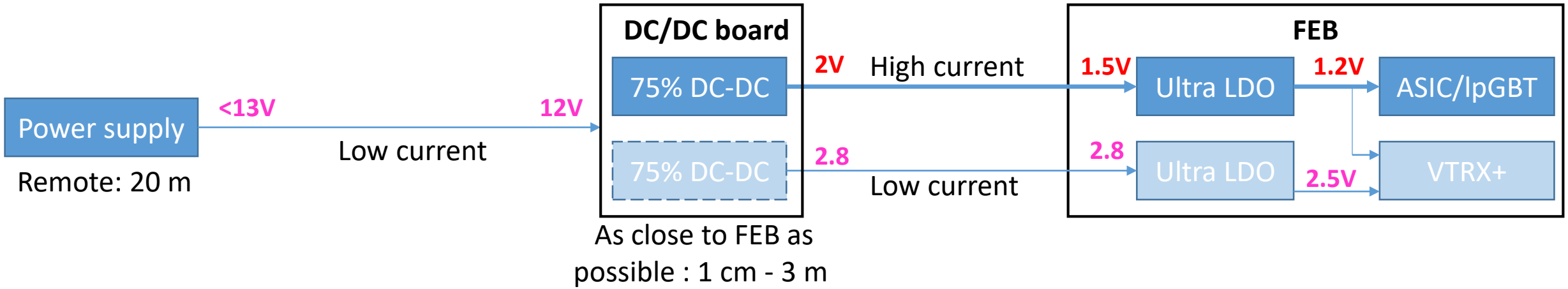
- Raw power budget with minimal margin : ~6.8 W
  - → 27 mW / ch
  - → 1.5V – 6.7 W
  - → 2.8V – 0.2W
- Assume 8.5 W for safety : 25% extra
  - → 33 mW / ch
  - → 1.5 V – 5.6 A
  - → 2.8 V – 90 mA
- Where to place DC/DC converters ?

FEB components and their power consumption

Component	Vin V	Current mA	Power mW	Comment
Salsa 1	1.2	1 000	1 200	15 mW/ch
Salsa 2		1 000	1 200	
LDO Salsa 1-2	1.5	2 000	600	Can use 2 LDOs to avoid hotspot
Salsa 3	1.2	1 000	1 200	15 mW/ch
Salsa 4		1 000	1 200	
LDO Salsa 3-4	1.5	2 000	600	Can use 2 LDOs to avoid hotspot
lpGBT	1.2	420	500	Probably 25% overestimated
LDO lpGBT/VTRX+	1.5	440	130	
VTRX+	1.2	20	25	
	2.5	70	175	
LDO VTRX+	2.8	70	20	

FEB power distribution

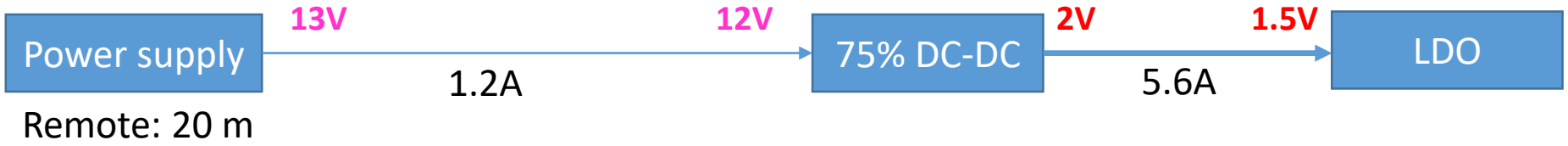
- DC/DC-based LV distribution: to be magnetic field tolerant
  - → Remote power supply distributes 12V with a low voltage drop over ~20 m cables
    - Say less than 1V
  - → Low cross-section power cables
    - The lower the drop the lower the power dissipation in cables but the large is their cross-section



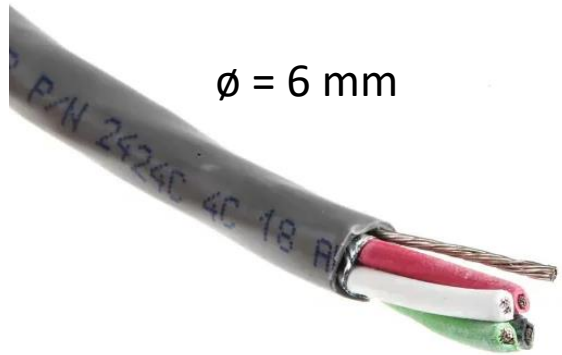
- DC/DC regulators
  - → Might be bulky and a source of EMI
    - Space + extra material for shielding
  - → Distribute high current for 1.2V power
    - Should be close to FEBs
      - Avoid significant power drop and power dissipation in cables
      - Avoid pickup noise and ground-loops

LV cables from power supply to DC/DC regulators

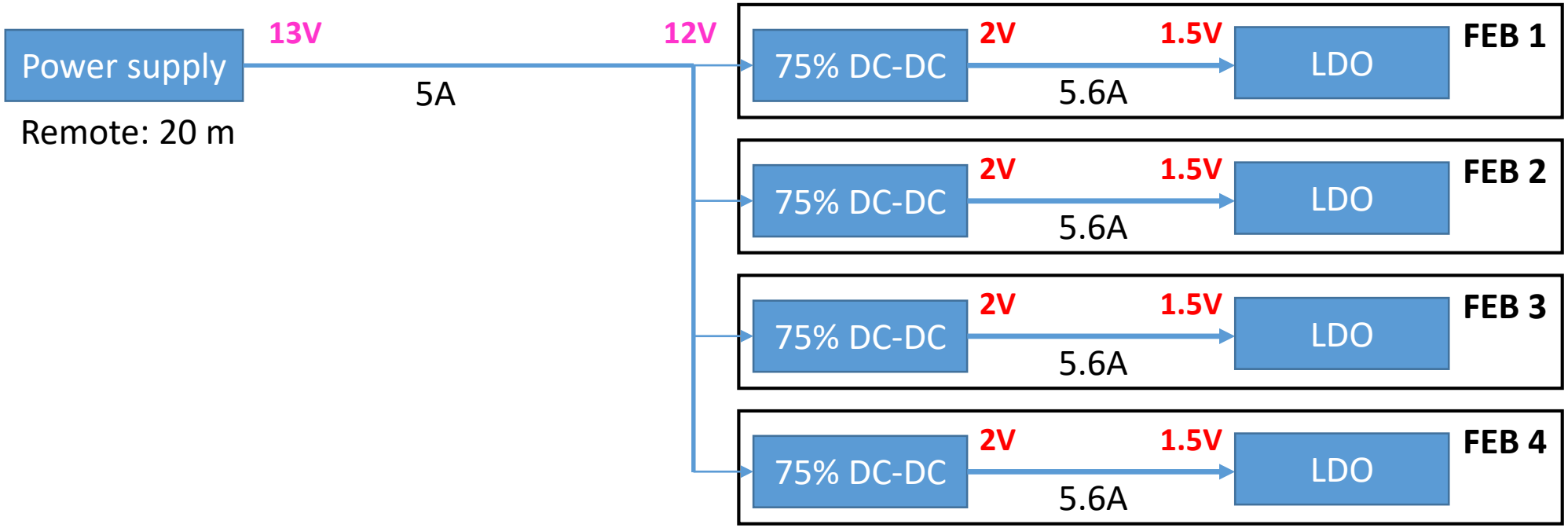
- Assumptions:
  - → Remote LV power supply 20 m away
  - → 1V voltage from between LVPS and DC/DC regulators
    - 13V LVPS output voltage for 12V DC/DC input
  - → 75% DC/DC efficiency
    - 1.2 A over LVPS cables



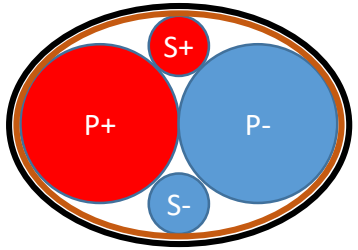
- LVPS power : 15 W / FEB
  - → 60 mW / channel
    - Remember : 15 mW / channel for Salsa !
  - → Power dissipation (loss) over LVPS cables : 1.2 W
- LVPS cables cross-section 0.8 mm^2 or 18 AWG
  - → Cable harness with two power cables and two sense wires
  - → Alpha Wire 2424C : commercial harness including shield and coating : ø = 6 mm
- Reminder : there are 160 CyMBaL FEBs



A power harness per CyMBaL detector module : 4 FEBs



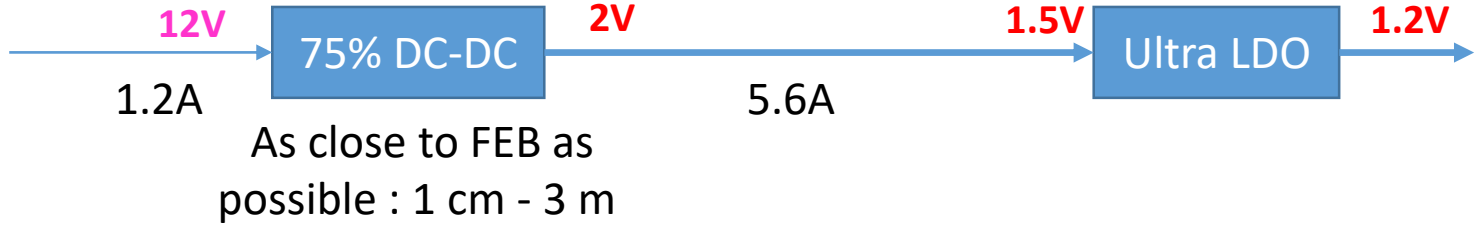
- Reasonable assumption for LVPS power cable cross-section : 12 AWG or 3.3 mm^2
  - → Cable harness with two power cables and two 0.5 mm^2 sense wires
  - → Harness ø = 4.5 mm including shield and coating



- Reminder : 32 LV power harnesses for 32 CyMBaL detector modules

LV cables from DC/DC regulators to LDO regulators

- Assume 0.5V voltage from between DC/DC and LDO regulators
  - → Reminder : no remote sense regulation
  - → 2V DC/DC output voltage for 1.5V LDO input
  - → 2.8W power dissipation (loss)



Cable cross-section vs DC/DC-LDO distance

DC/DC-LDO Distance	Cross section		Harness + 2.5V cabs
cm	mm^2	AWG	Ø mm
30	0.1	26	4.6
50	0.2	24	5
100	0.4	20	5.4
200	0.8	18	6
300	1.2	16	

Alpha Wire
3464C

6328

2414C

2424C

- Reminder : there are 640 MPGD FEBs with tailored power cable Assemblies
- If possible, having DC/DC board next to FEB is preferred

FEB organization ?

- Understand if a daughter card hosting lpGBT and VTRX+ can suite all MPGDs
  - → Placing lpGBT on FEB makes it high-density high-speed grade PCB
    - 10 Gbit/s link speed
    - 0.5 mm pitch 289-ball (17x17) BGA
  - → Pros
    - Production of a large number communication cards common to MPGDs
    - Form-factor adapted low complexity “cheap” FEBs
  - → Cons
    - More types of PCBs to produce and maintain
- Understand if a DC/DC power mezzanine can fit all MPGDs
  - → Pros
    - Avoids LV cables, ground loops, improves regulation
  - → Cons
    - Extra material due to air core and shield