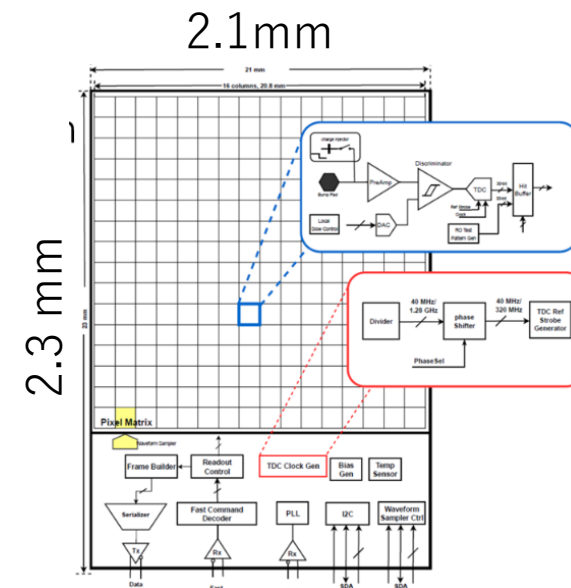
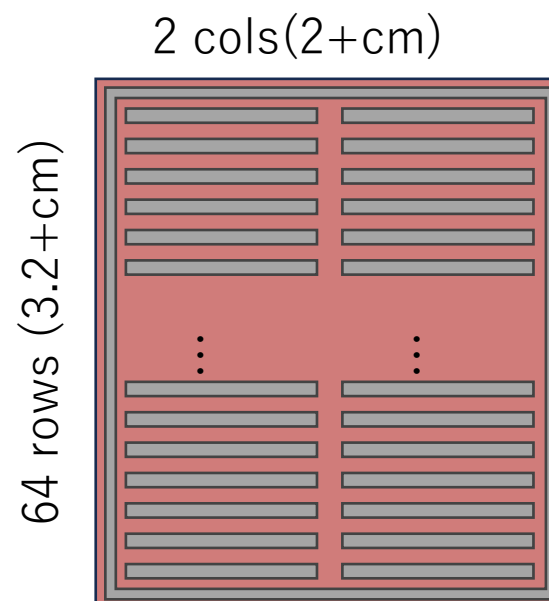
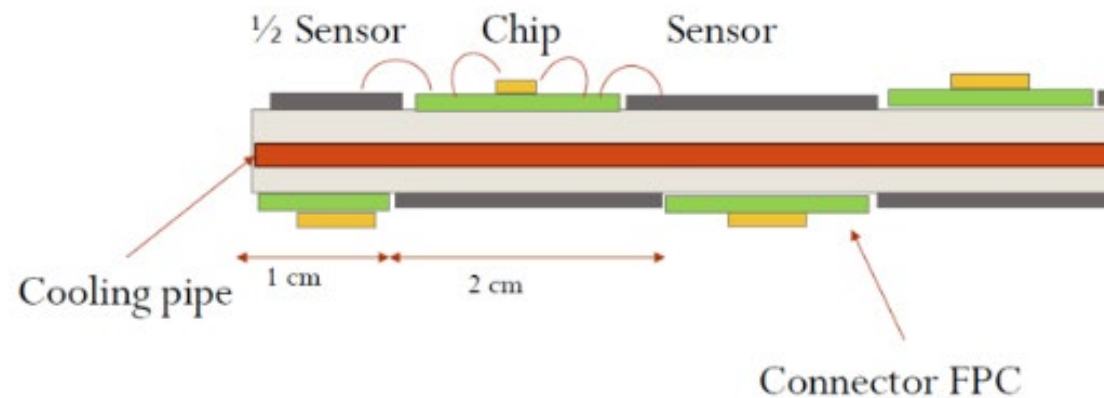


FPC設計の試み2

蜂谷 崇

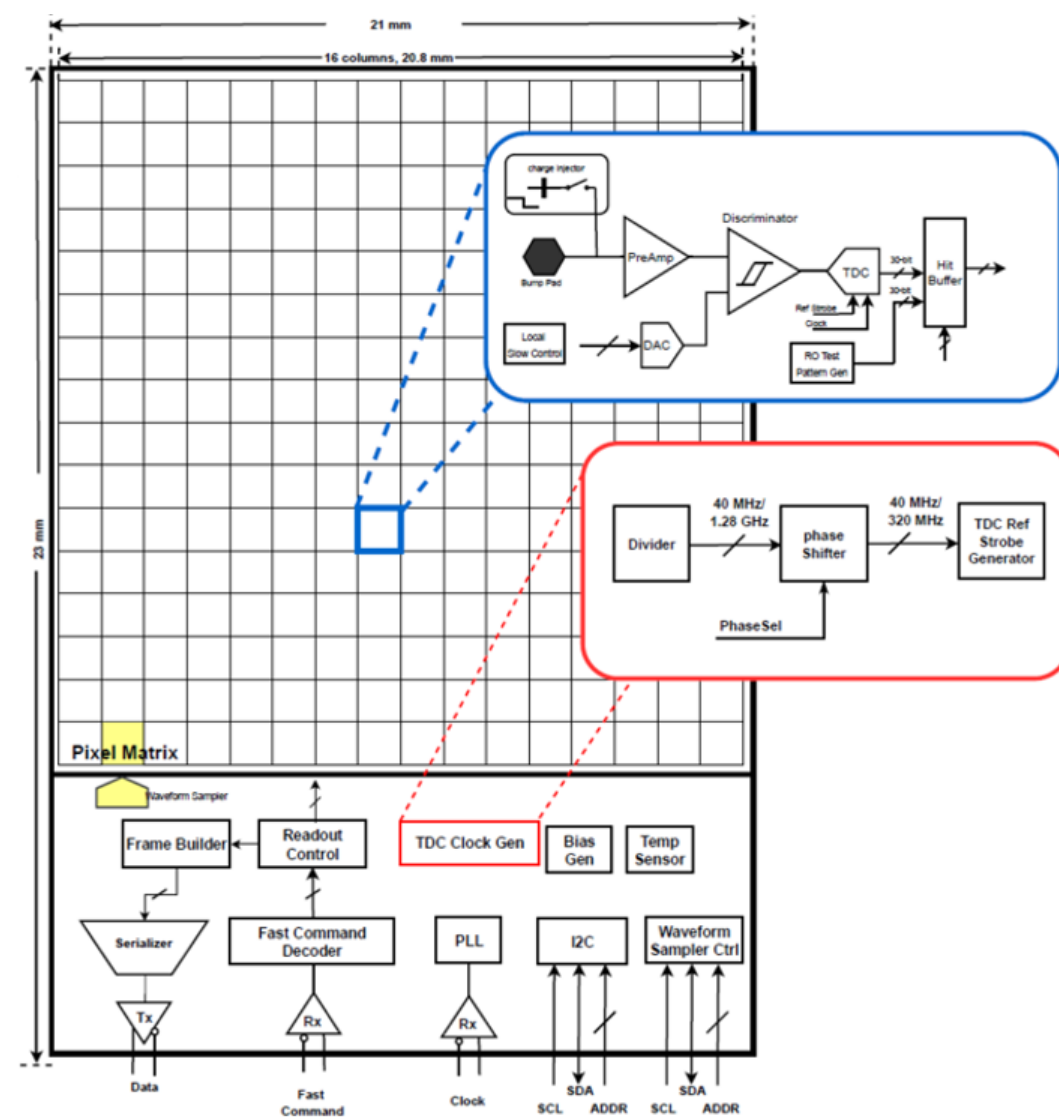
Basic information

- BTOF Ladder structure
 - Sensor/ASIC on FPC are put at both front and back sides
 - 2 FPCs are necessary
- Sensor dimension
 - 64x2 strips as unit = 3.2 x 2 cm²
 - Strip size : 0.5mm x 1cm
- ASIC: ETROC2 as 1st candidate
 - This is for CMS-pad-LGAD)
 - Size : 21x23mm²
 - Analog inputs : 128 signals
 - Connected to 16x16 pixels on a sensor by bump bonding
- More ETROC2 info necessary for FPC design



More ETROC2 info

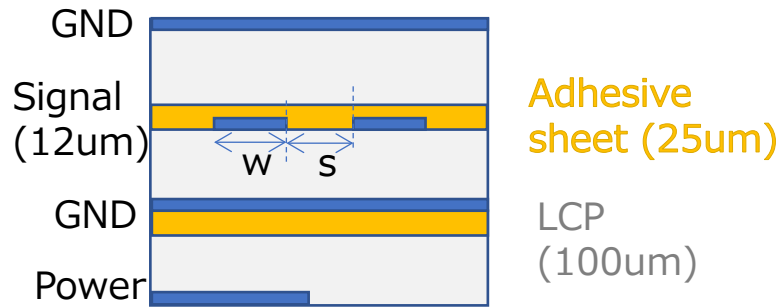
- Size : 21x23mm² since 2D for the pixels
 - I/O part is placed at bottom
- Npads : 124 for wire bonding
 - Digital lines: 18 lines → ~10 or 11 lines
 - Tx: DataOut (LVDS) x 2 → DataOut (LVDS) x 1 p2p
 - Rx: *CLK40 (LVDS)* → *p2p*
 - Rx: *FastCom (LVDS)* → *bus w/ 2 or 3 chips (not p2p)*
 - Rx: **I2C (2 lines, SCK, SDA)** → *bus w/ 15~20 chips*
 - Rx: I2C addr (5bits) → *5 or 6 bits (depending on FPC conf.)*
 - Rx: **RSTn (1line)** → **bus for all chips**
 - Rx: CLK1280 (LVDS) : debug → not needed
 - Analog : 1 line (Vtemp) → needed
 - Power/GND/others : **105 lines**
 - No connection of waveform sampling part assumed
- 130 cm FPC = 32 or 33 sens/side (x2 FPCside x 2cm/sens)
 - **32 or 33** ASICs are necessary
 - If 150cm FPC, ~40 sens
- If 33 ASIC's are in a side, 33 x 11= 366 lines
 - 122 lines for INTT (3times more than INTT)



INTTのFPCとの比較

- INTT 長尺FPC

- 130 & 130um
- 124 lines / layer w/ GND sandwiched



- BTOF: 366 lines

-> 3 signal layers +

at least 4 GND/ power layers

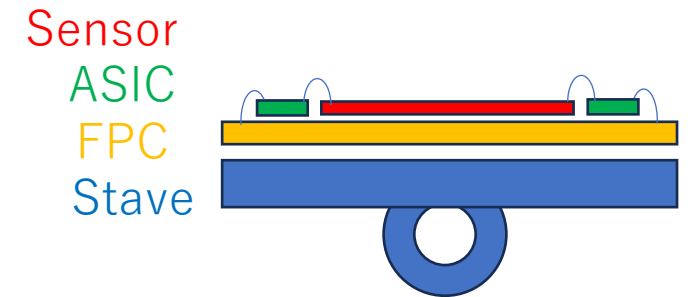
X = 1.2%, 厚み0.8mm

- INTT HDI (ただし最長50cm)

- 50um & 50um (100um/line)
- 7層、2 sig layers

2GND + A/D power + Bias + 3 signal

- 350 lines / layer (3.5cm幅に収める)が可能? 計算上

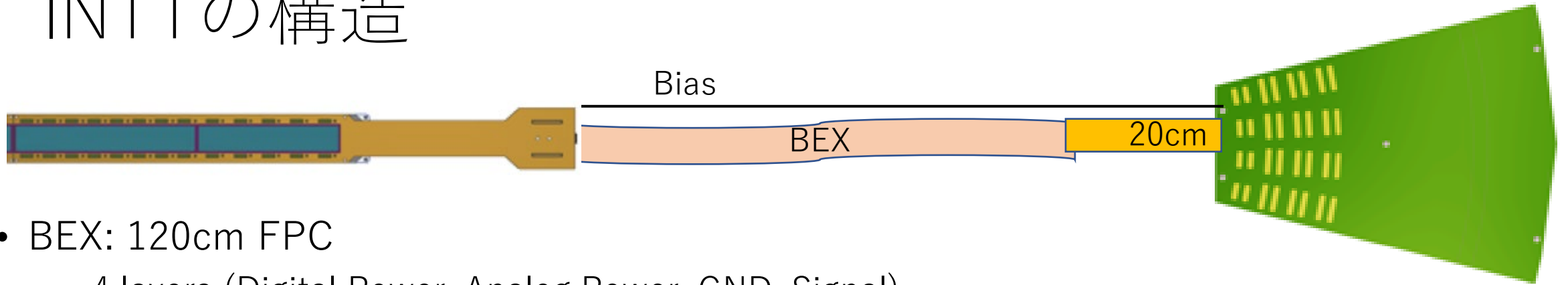


- BTOF : 366 lines

-> 2 layers at least 3 GND/PW layers, probably more

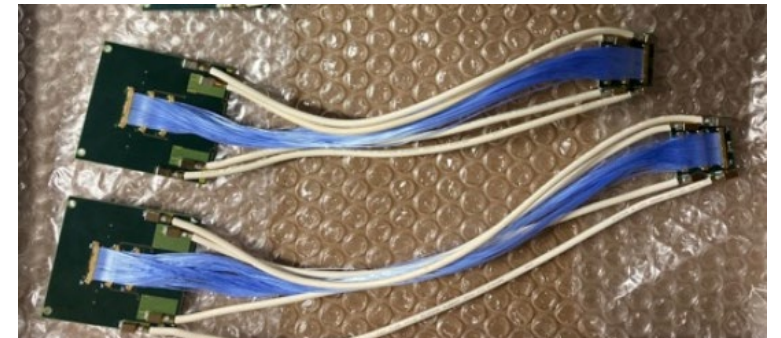
X=1%, 厚み0.6mm

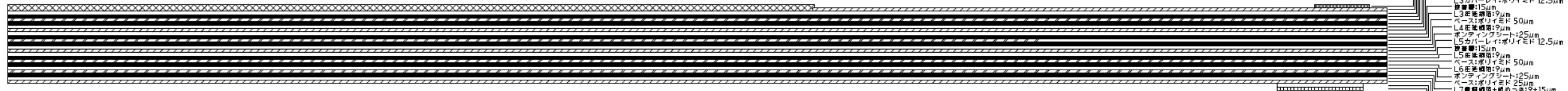
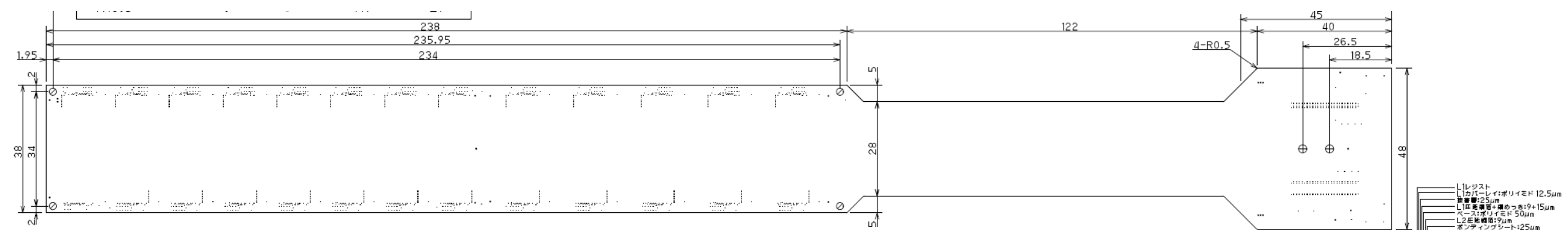
INTTの構造



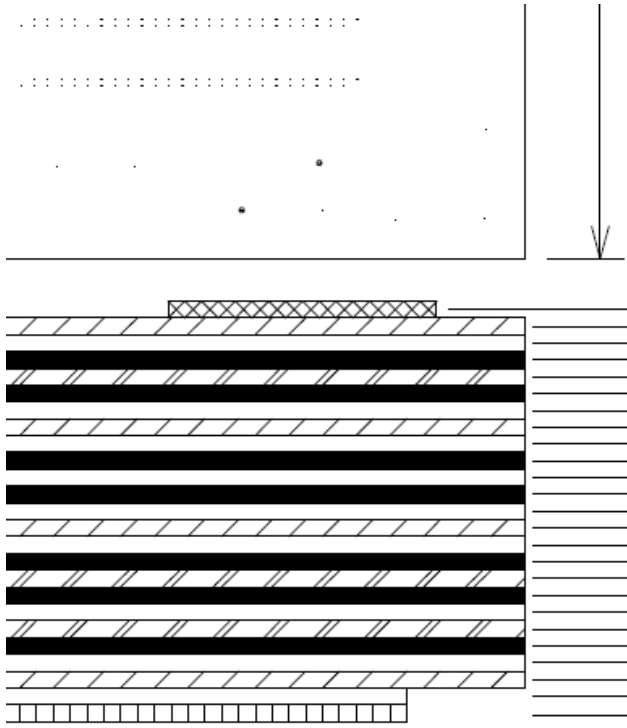
- BEX: 120cm FPC
 - 4 layers (Digital Power, Analog Power, GND, Signal)
 - Signal layer contains 62 LVDS pairs)
 - Signal line/space : 130um/130um
- Bias cable
 - 2 Coax for sensor A/B
- Micro-Coax (20cm)
 - Curving path
- Half ladder (40cm)
 - 26 ASIC : each ASIC has 2 data outputs (2 LVDS pairs)
 - 7 layers
 - Analog, Digital, Bias, GND, signal x 2
 - Signal layer : line/space 50um/50um

Micro-Coax





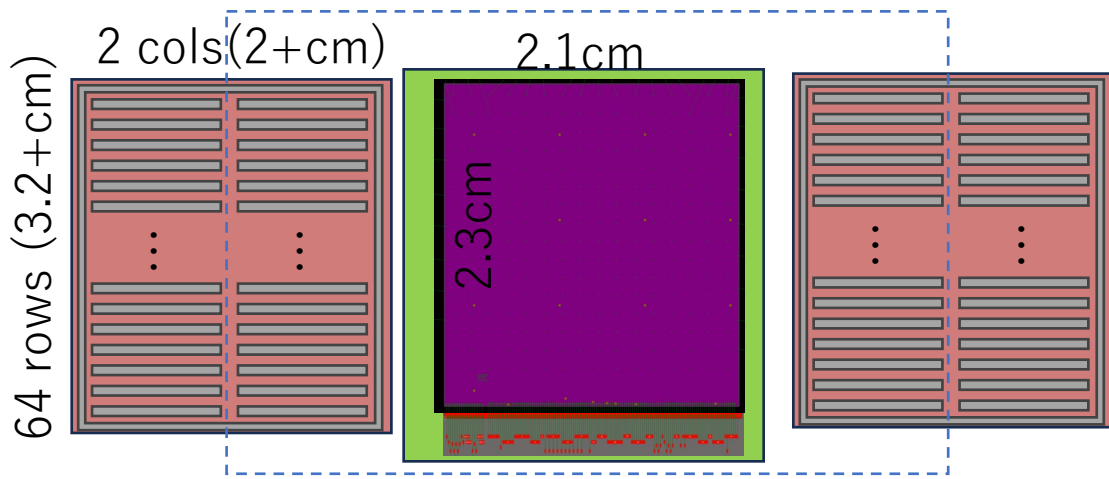
- L1レジスト
- L1カバーレイ:ポリイミド 12.5 μ m
- 接着層:25 μ m
- L1圧延銅箔+銅めっき:9+15 μ m
- ベース:ポリイミド 50 μ m
- L2圧延銅箔:9 μ m
- ボンディングシート:25 μ m
- L3カバーレイ:ポリイミド 12.5 μ m
- 接着層:15 μ m
- L3圧延銅箔:9 μ m
- ベース:ポリイミド 50 μ m
- L4圧延銅箔:9 μ m
- ボンディングシート:25 μ m
- L5カバーレイ:ポリイミド 12.5 μ m
- 接着層:15 μ m
- L5圧延銅箔:9 μ m
- ベース:ポリイミド 50 μ m
- L6圧延銅箔:9 μ m
- ボンディングシート:25 μ m
- ベース:ポリイミド 25 μ m
- L7電解銅箔+銅めっき:9+15 μ m
- 接着層:25 μ m
- L7カバーレイ:ポリイミド 12.5 μ m
- 接着剤:熱硬化性接着剤 40 μ m
- L7補強板:FR-4 1000 μ m



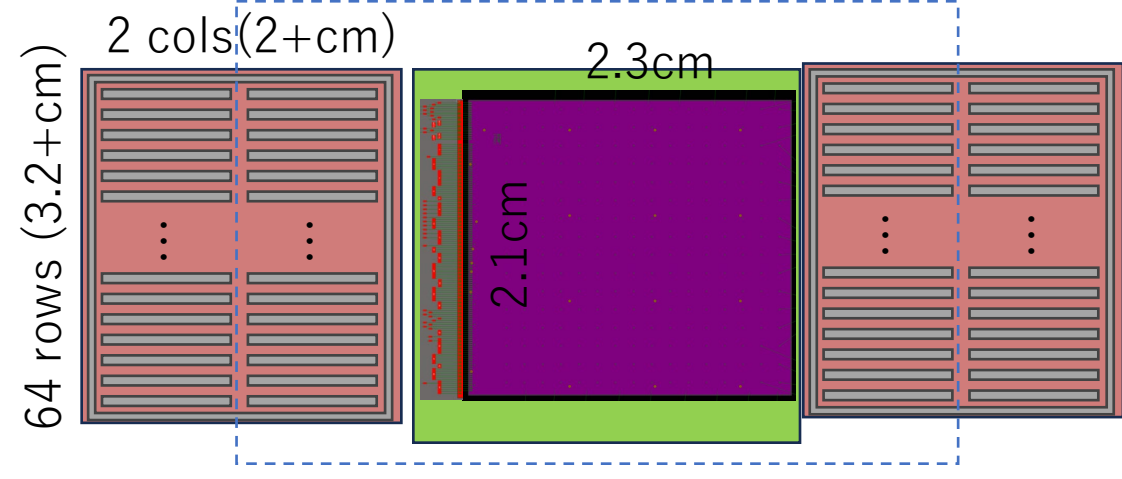
- L1レジスト
- L1カバーレイ:ポリイミド 12.5 μ m
- 接着層:25 μ m
- L1圧延銅箔+銅めっき:9+15 μ m
- ベース:ポリイミド 50 μ m
- L2圧延銅箔:9 μ m
- ボンディングシート:25 μ m
- L3カバーレイ:ポリイミド 12.5 μ m
- 接着層:15 μ m
- L3圧延銅箔:9 μ m
- ベース:ポリイミド 50 μ m
- L4圧延銅箔:9 μ m
- ボンディングシート:25 μ m
- L5カバーレイ:ポリイミド 12.5 μ m
- 接着層:15 μ m
- L5圧延銅箔:9 μ m
- ベース:ポリイミド 50 μ m
- L6圧延銅箔:9 μ m
- ボンディングシート:25 μ m
- ベース:ポリイミド 25 μ m
- L7電解銅箔+銅めっき:9+15 μ m
- 接着層:25 μ m
- L7カバーレイ:ポリイミド 12.5 μ m
- 接着剤:熱硬化性接着剤 40 μ m
- L7補強板:FR-4 1000 μ m

ASIC Layout as example

ASIC vertical placement



ASIC horizontal placement



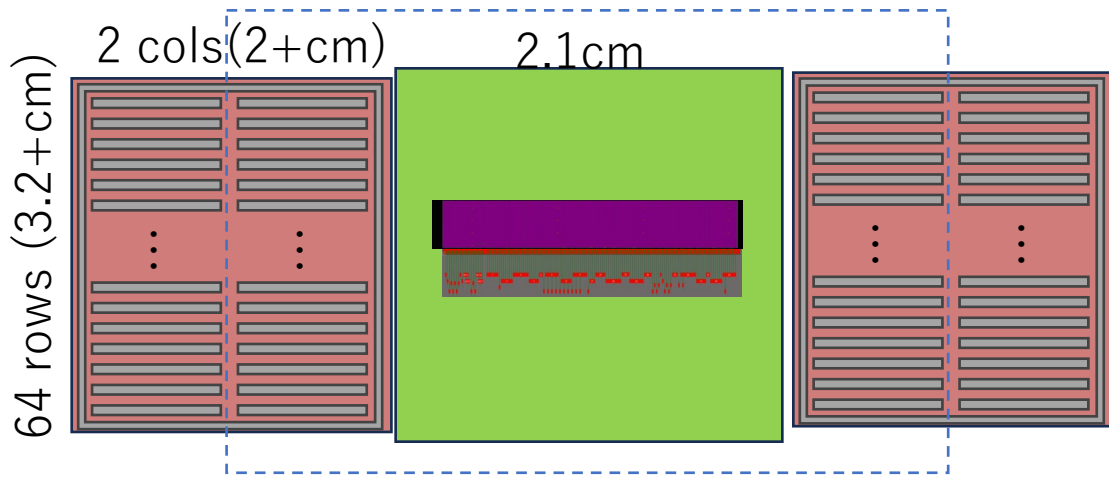
- Signal lines are placed horizontally in FPC
 - Which placement are appropriate for us?



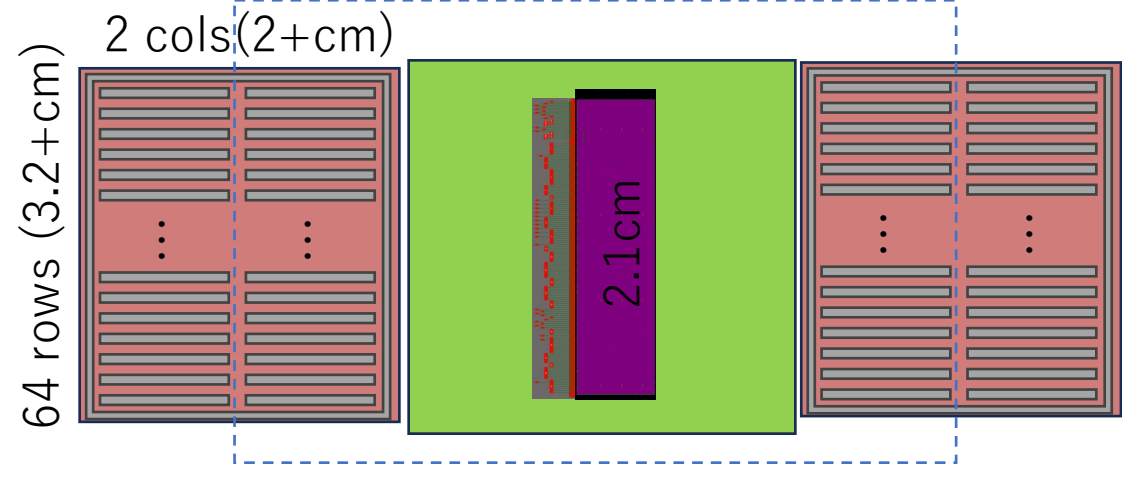
FPCの配線としては、左側の配置が良さそう

ASIC Layout as example 2

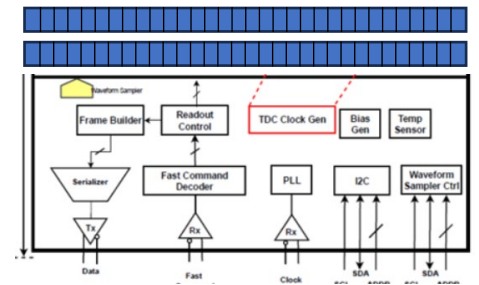
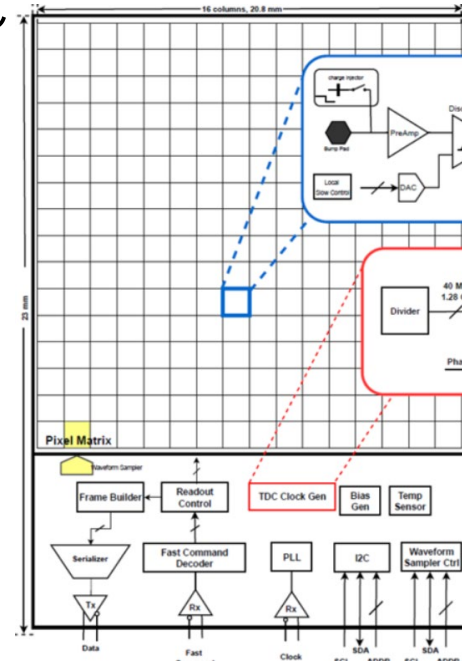
ASIC vertical placement



ASIC horizontal placement

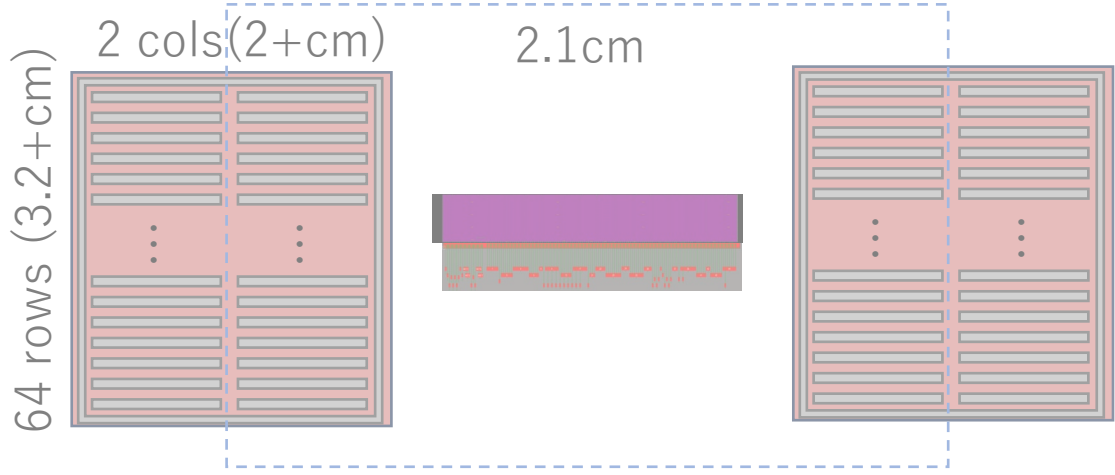


- Signal lines are placed horizontally in FPC
 - Which placement are appropriate for us?
- ASIC size might get shorter
- ASICのデザインは進んでいない
- Interposerのデザインは進んでいない

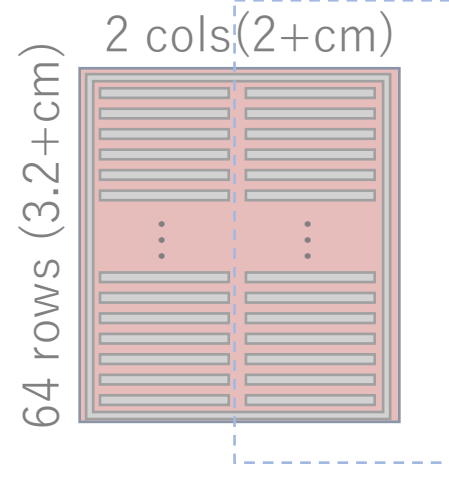


ASIC Layout as example 3

ASIC vertical placement



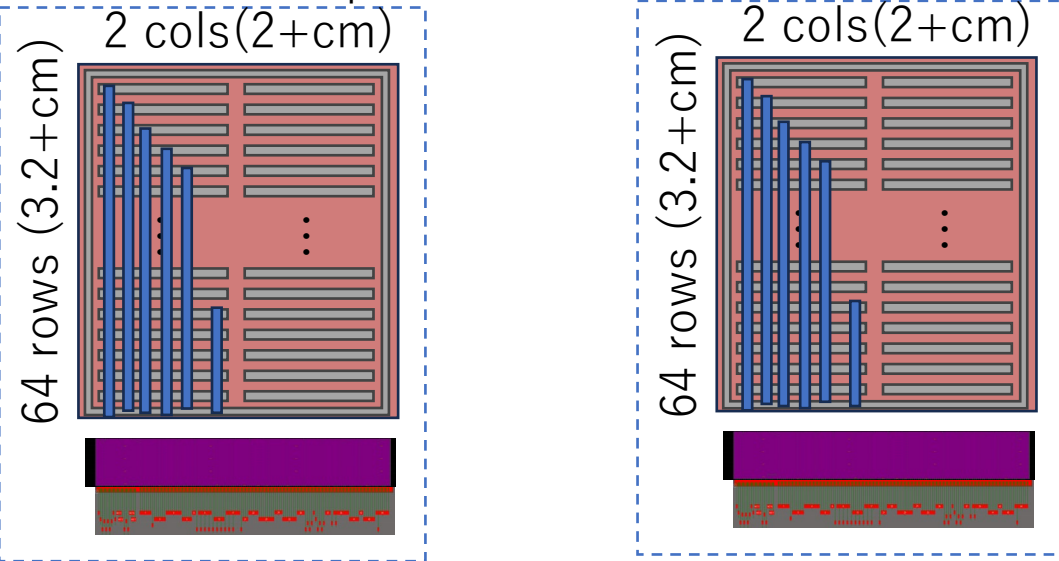
ASIC horizontal placement



N shaped electrodes by double metal on INTT sensor



ASIC bottom placement



- Bottom placement

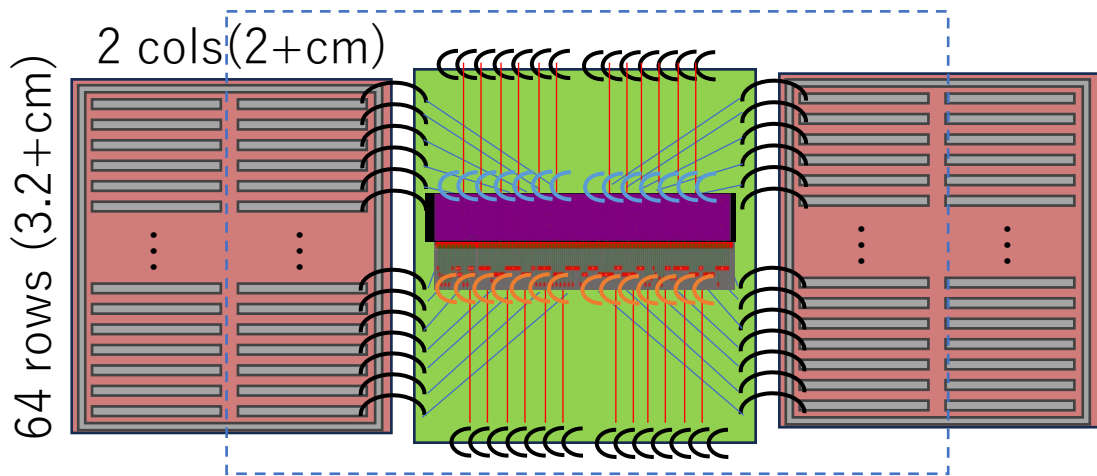
- Double metal technology
 - Standard for nominal Si (INTT used)
- Easy to make an unit module

- ミーティング時のコメント

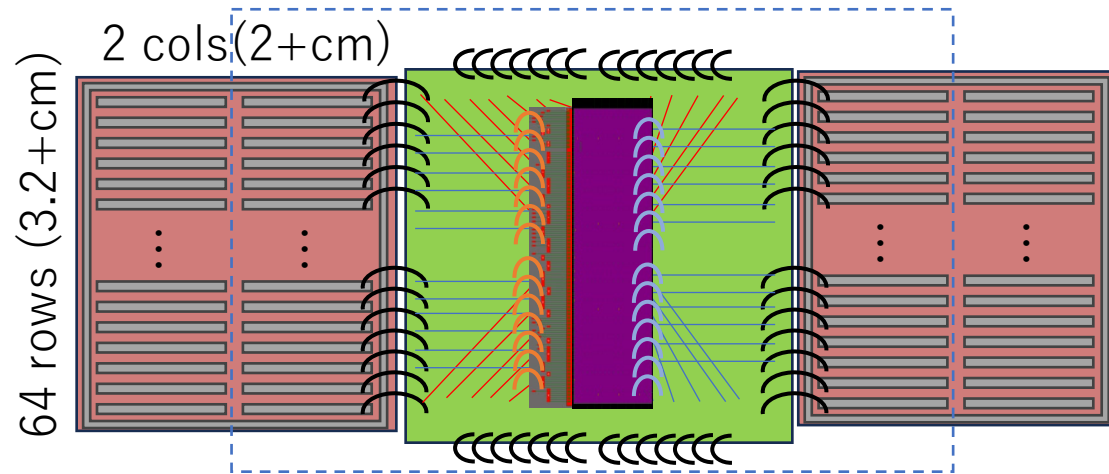
- ダブルメタルはCh毎に配線長が異なり、時間分解能が悪くなる。
- 蜂谷コメ： 配線長はインターポーザとチップのデザインによる部分も大きい。 配線長による分解能の悪化度合いはStudyが必要

ASIC Layout as example 2

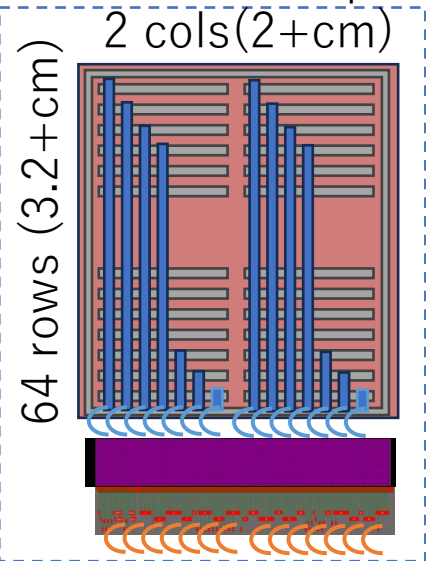
ASIC vertical placement



ASIC horizontal placement



ASIC bottom placement



- インターポーズがある場合
 - 多層基板が必要
 - 内部の配線長はCh毎に異なる。
 - FPCかRigidか、まだ決まっていない。
- インターポーズが無い場合、
 - WireBondingは単純になる。
 - その分FPCが複雑化？ 要検討


Summary

- ETROC2 has many connections (124) including signals, power, and GND
- Questions for design
 - Which lines are in parallel ?
 - What size (dimension) of ASIC (ETROC2) for us?
 - How does ASIC is placed?
 - Furthermore
 - How signal lines are placed in FPC ?
 - Complicated routing of the signal lines are not good for the long FPC.
 - Connecting some short FPC to make long FPC is possible option (as shown by Simone last week)

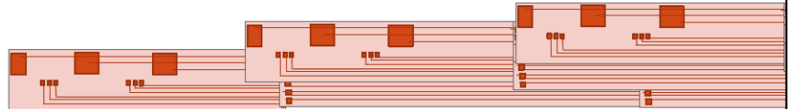
Simone's slide last week

FPC idea


- FPCs are spTAB bonded to be extended so it's flush



- Flex are stacked and glued on the stove one on top of the other



- Side view



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