FPCs for ePIC SVT Disks

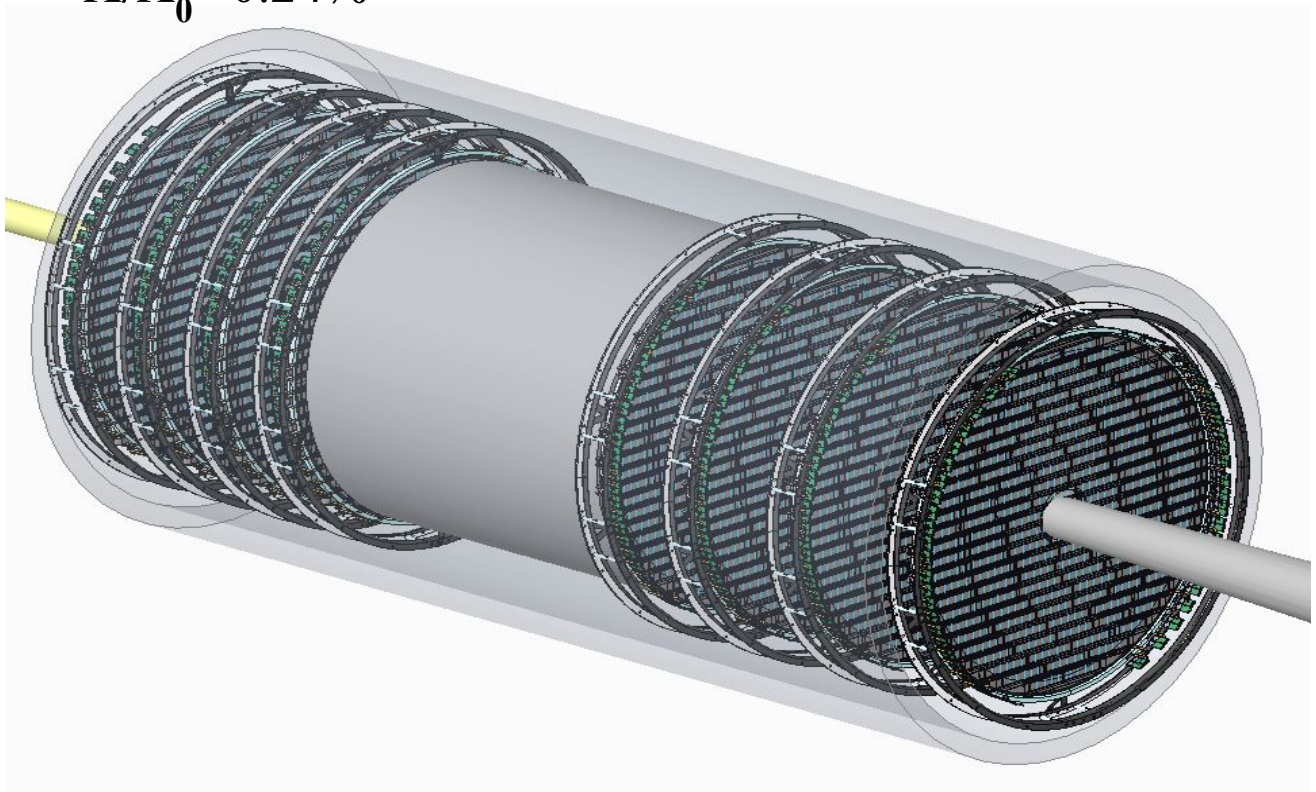
Zhenyu Ye

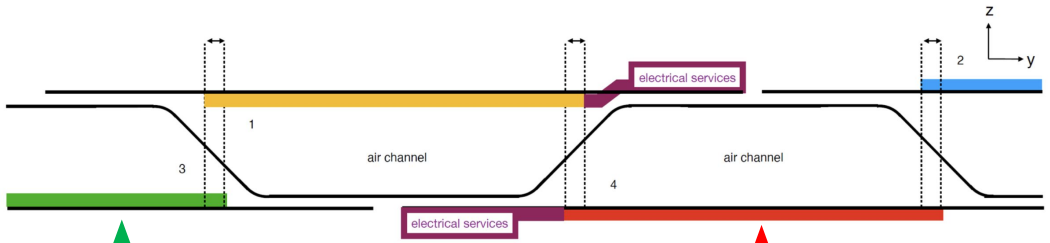
Lawrence Berkeley National Laboratory

9/11/2025

ePIC SVT Disks

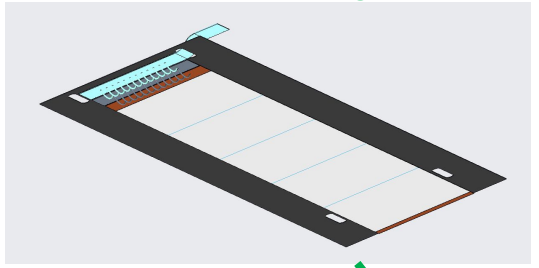
- **EIC Large-Area Sensor** with design based on ITS3 MOSAIX, mounted on low-mass CF support structure with integrated air cooling
- **AncASIC** provide negative sensor bias voltage, serial power and slow control
- **Outer radius** ranging from 24 to 40 cm
- **X/X_0** ~0.24%

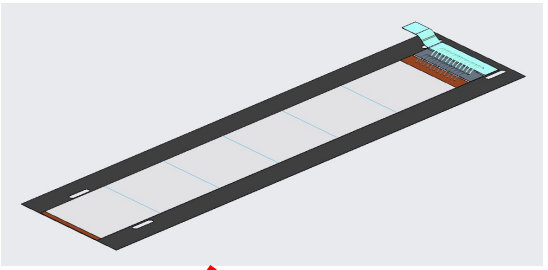


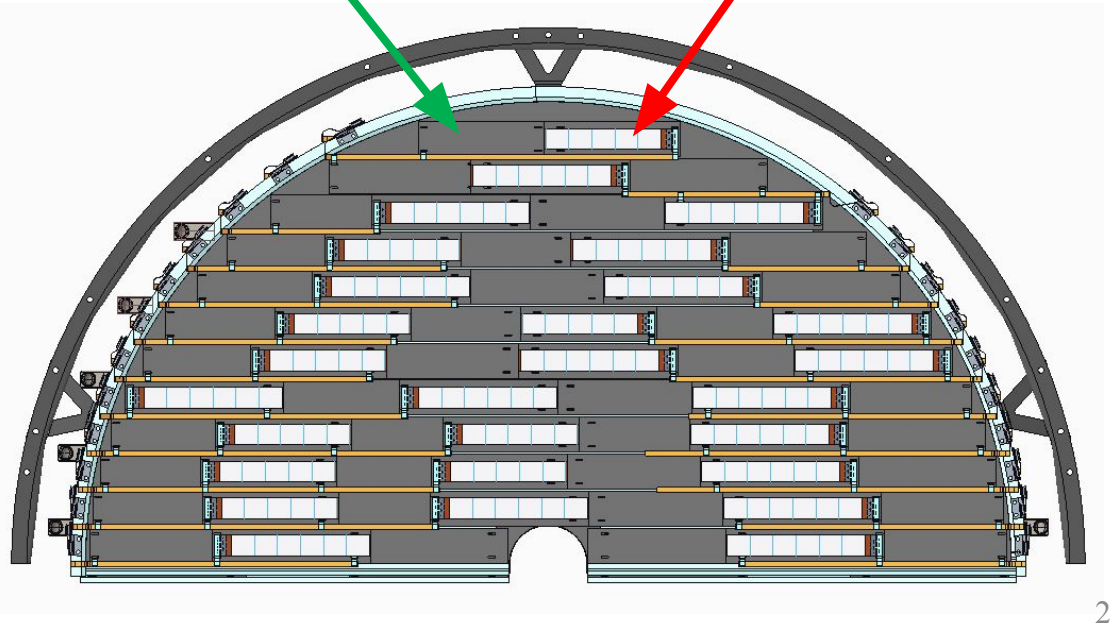


Sensor Inward Facing Module

Sensor Outward Facing Module



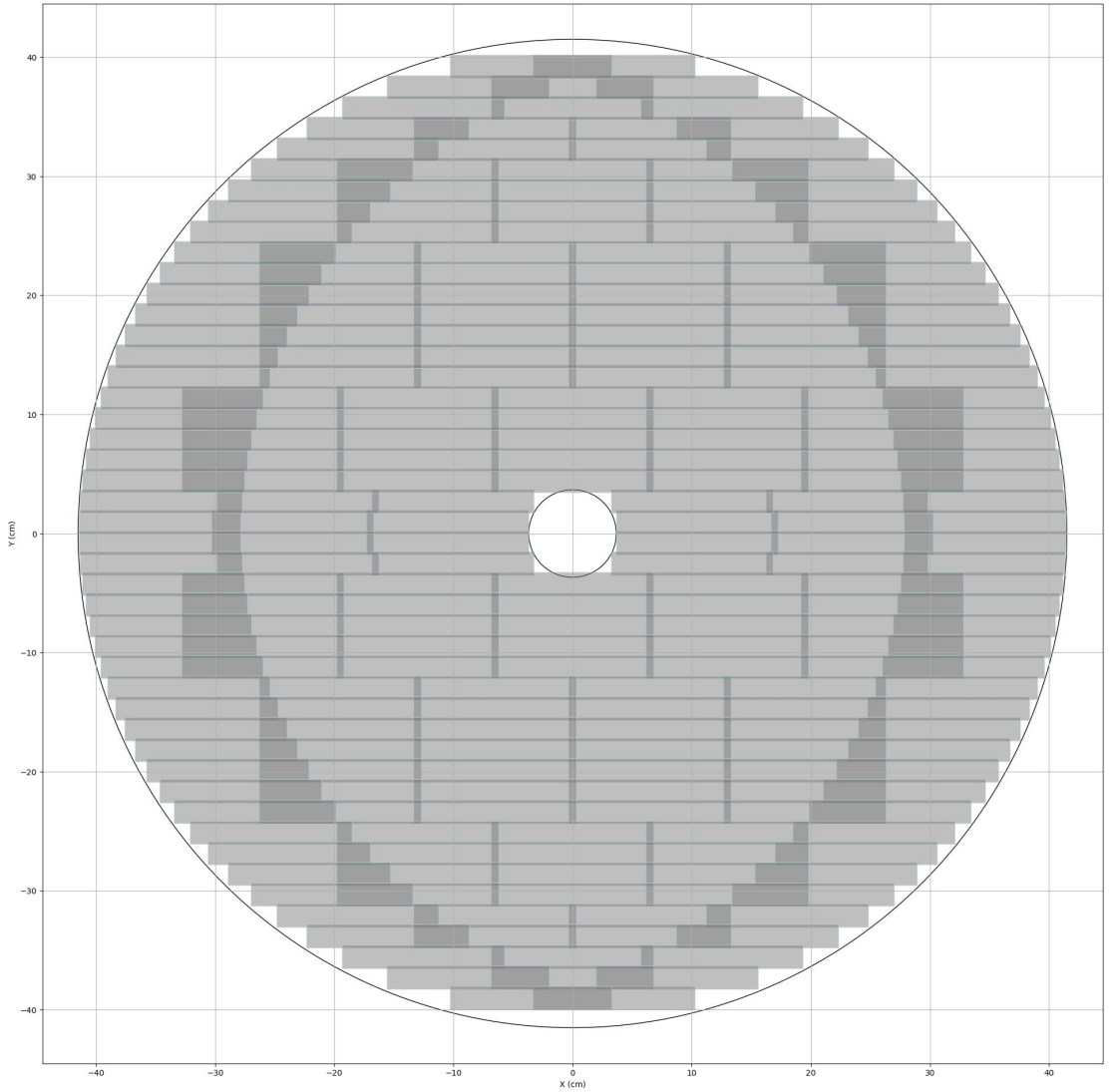




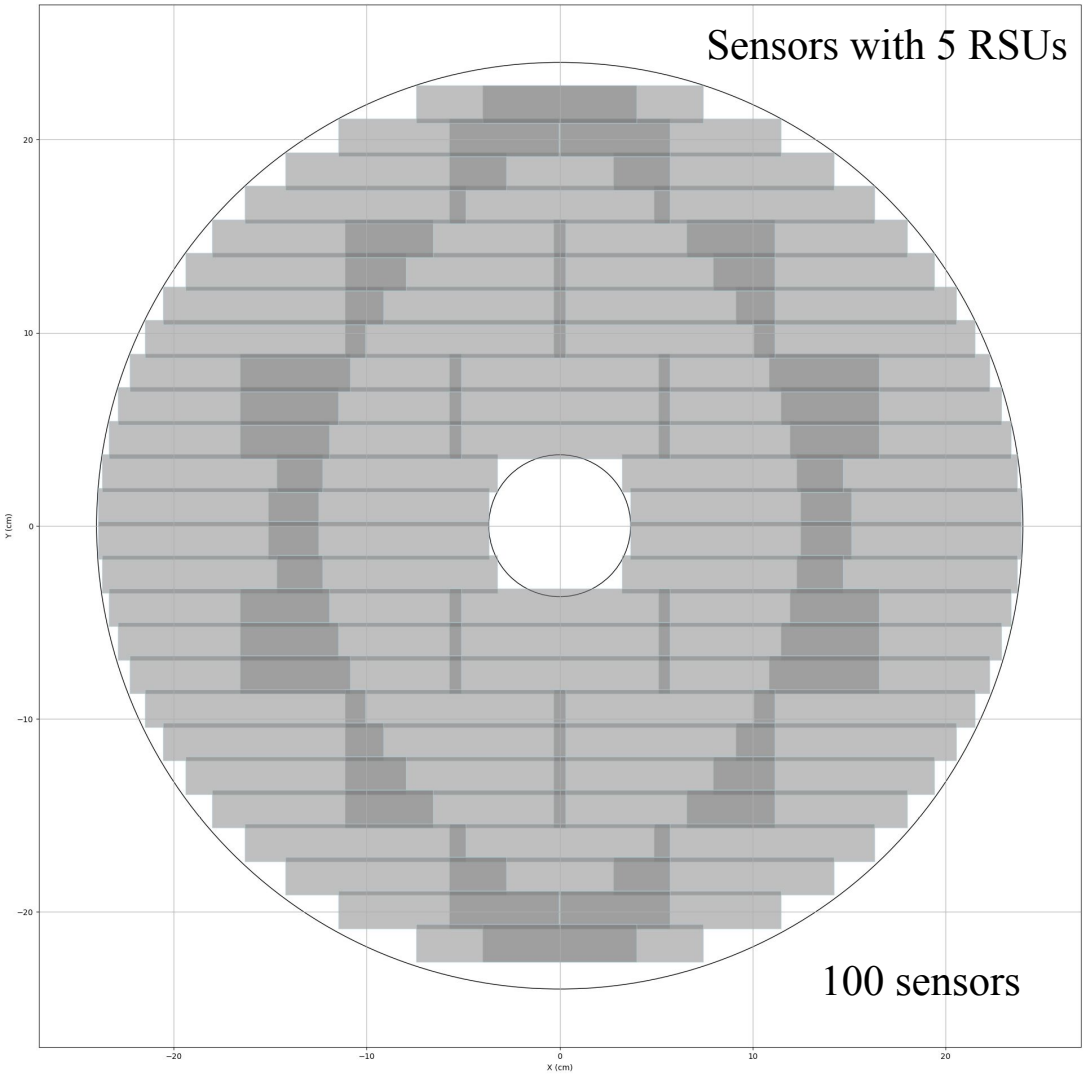
ePIC SVT Disks

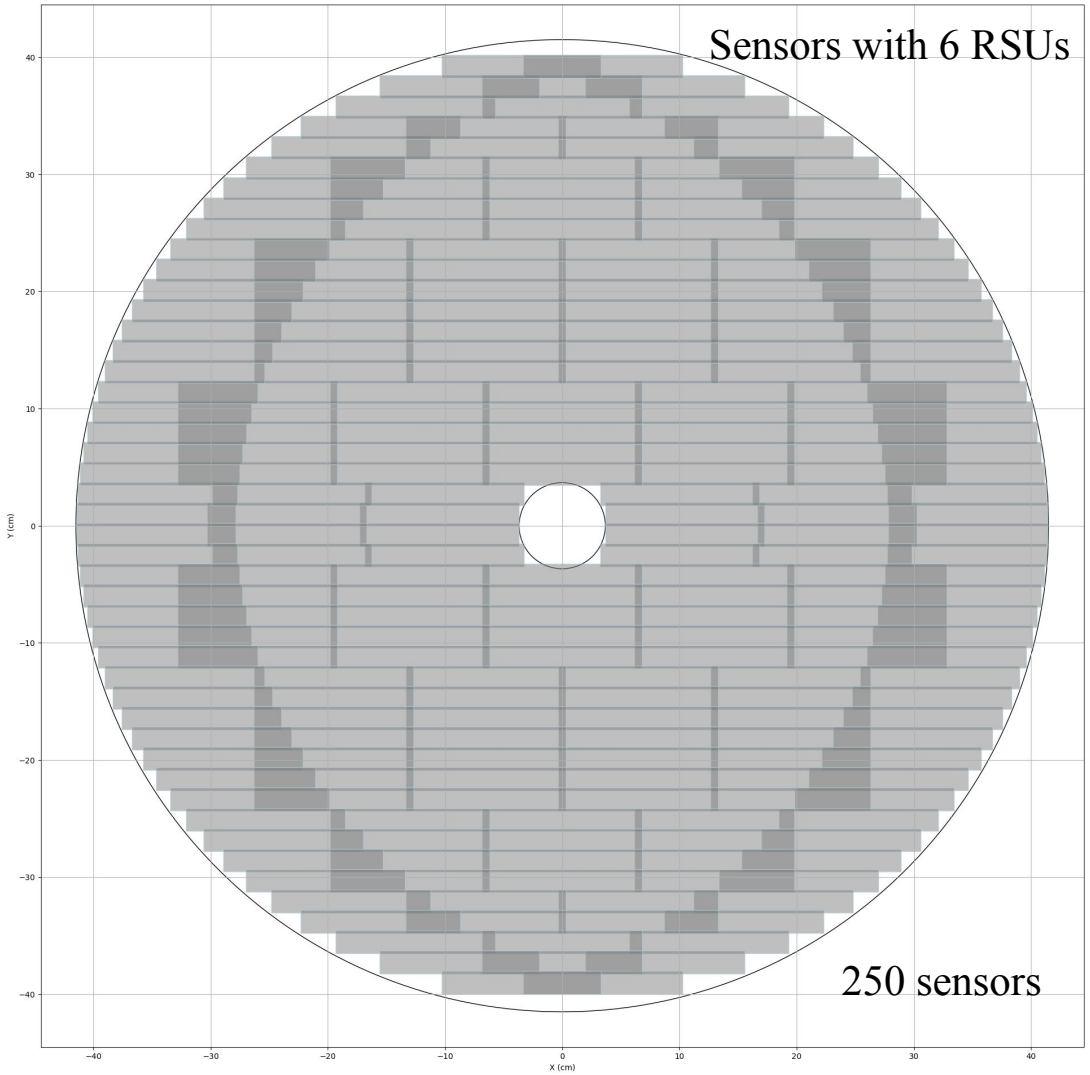
Sensor placement strategy for disks: minimum overlap in the inner region, maximum in the outer region; symmetric in x if possible; LEC at larger radius than REC.

- For rows covered by the beam pipe, start filling the first sensor at $x=\sqrt{(R_{in}^2-y^2)}$, so that the edge of the sensor is the closest possible to the beam pipe.
- Place the other sensors with an overlap of 6 mm to the previous one to avoid gaps covered by active sensor areas.
- Stop when the last sensor would be outside of the disk. Place the last sensor at $x=\sqrt{[R_{out}^2-(y+\text{sensor height})^2]}$-sensor length, so that the edge of the sensor is at the outer radius of the disk.
- The sensors at the edge of the disks will connect via an edge FPC to the corresponding FPC interface board (FIB). The other sensors will connect via bridge and main FPCs to the FIB (see page 10&11).
- The length of the main FPC may need to vary depending on y.



ePIC SVT Disks - ED0/HD0, ED1/HD1

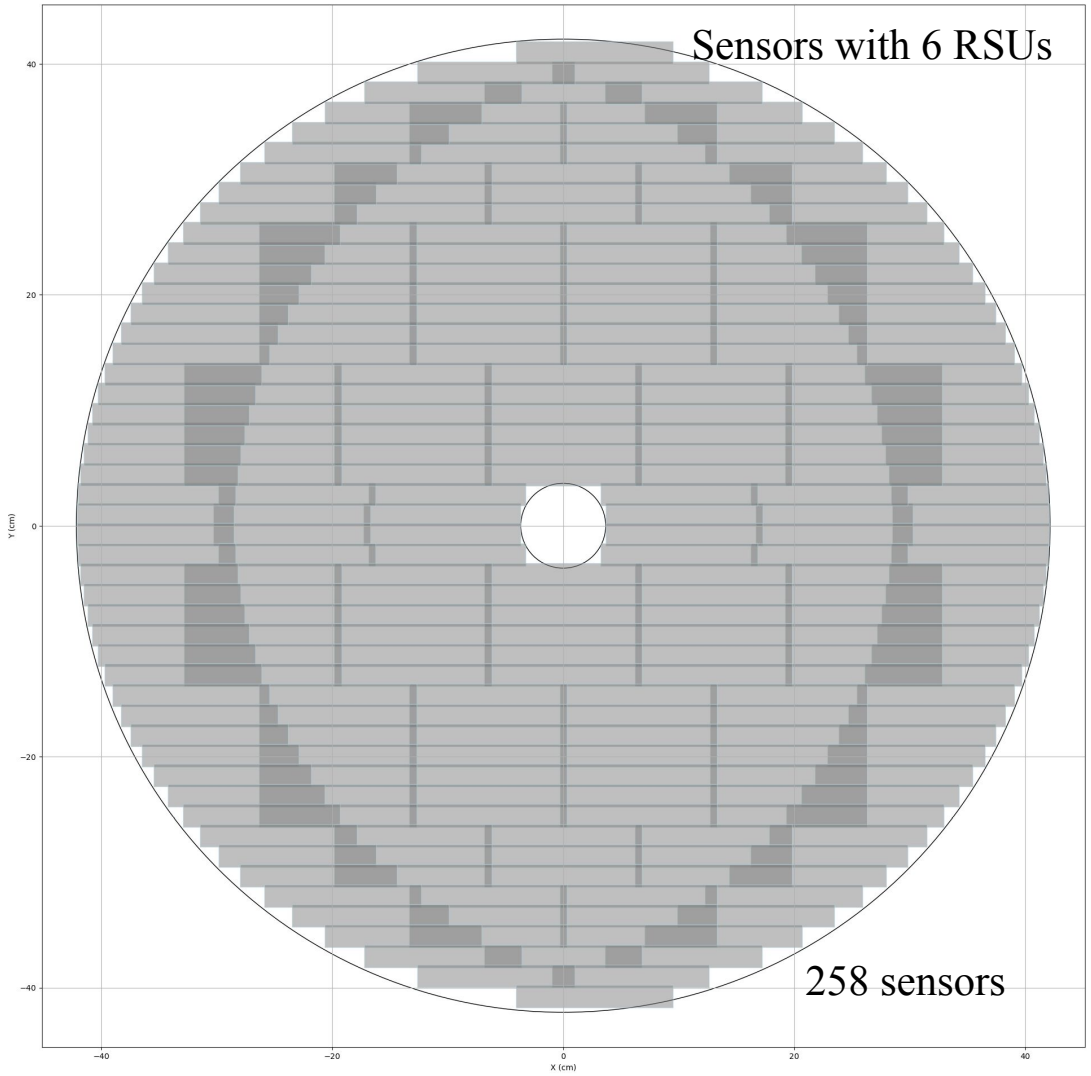




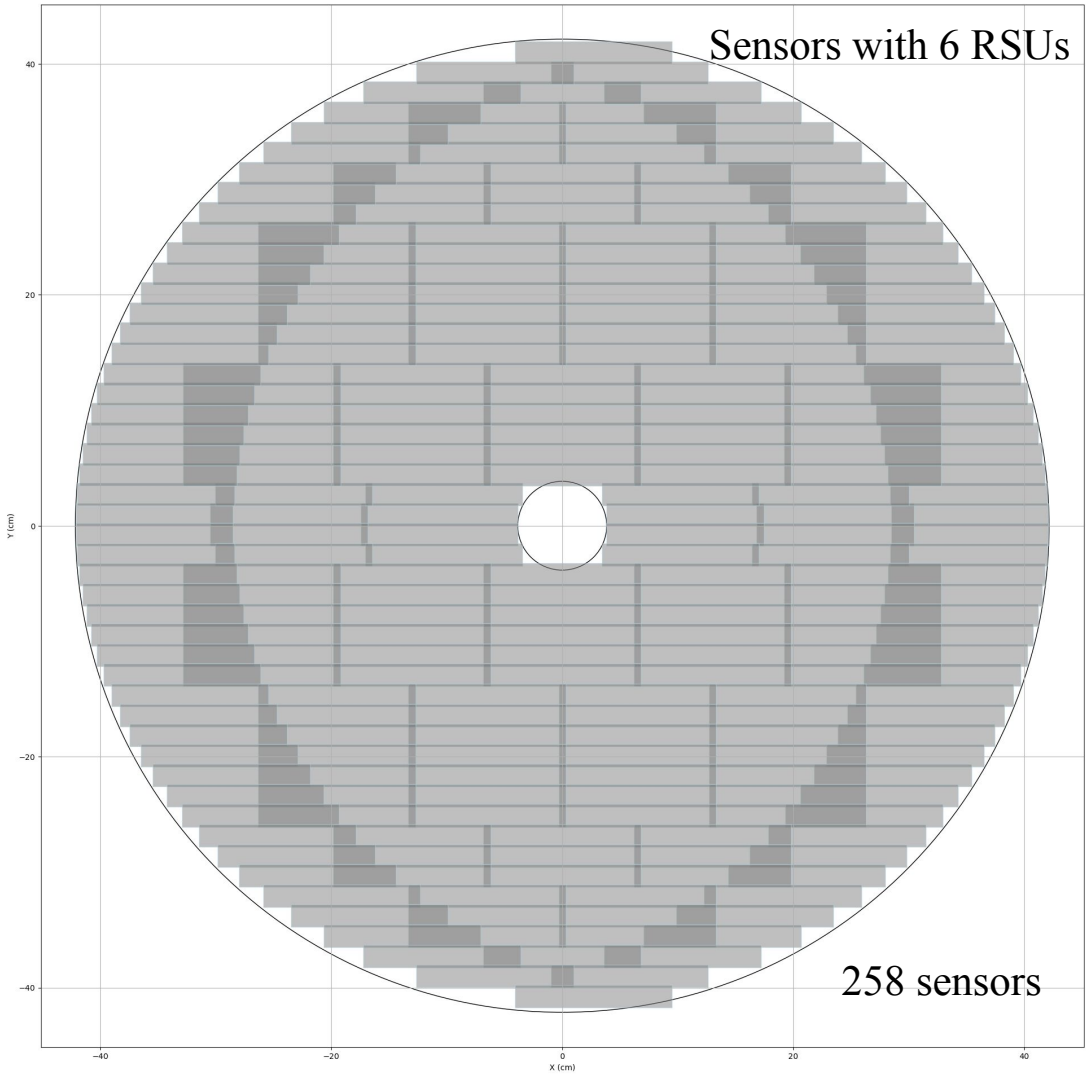
Region	Disk	|z| (mm)	Inner radius (mm)	Outer radius (mm)	X/X0
EE/HE	ED0/HD0	250	36.76	240	0.24%

Region	Disk	|z| (mm)	Inner radius (mm)	Outer radius (mm)	X/X0
EE/HE	ED1/HD1	450	36.76	415	0.24%

ePIC SVT Disks - ED2/HD2

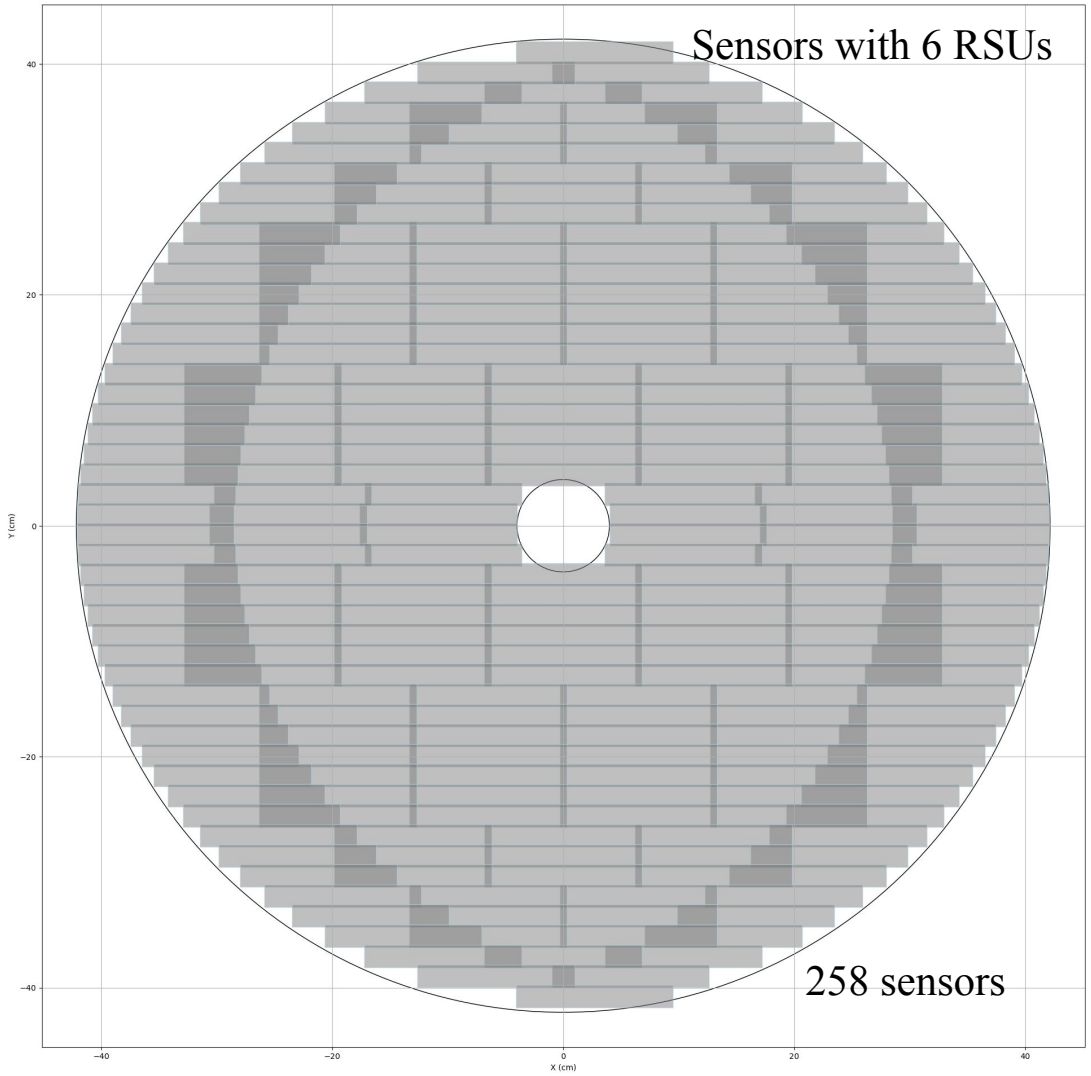


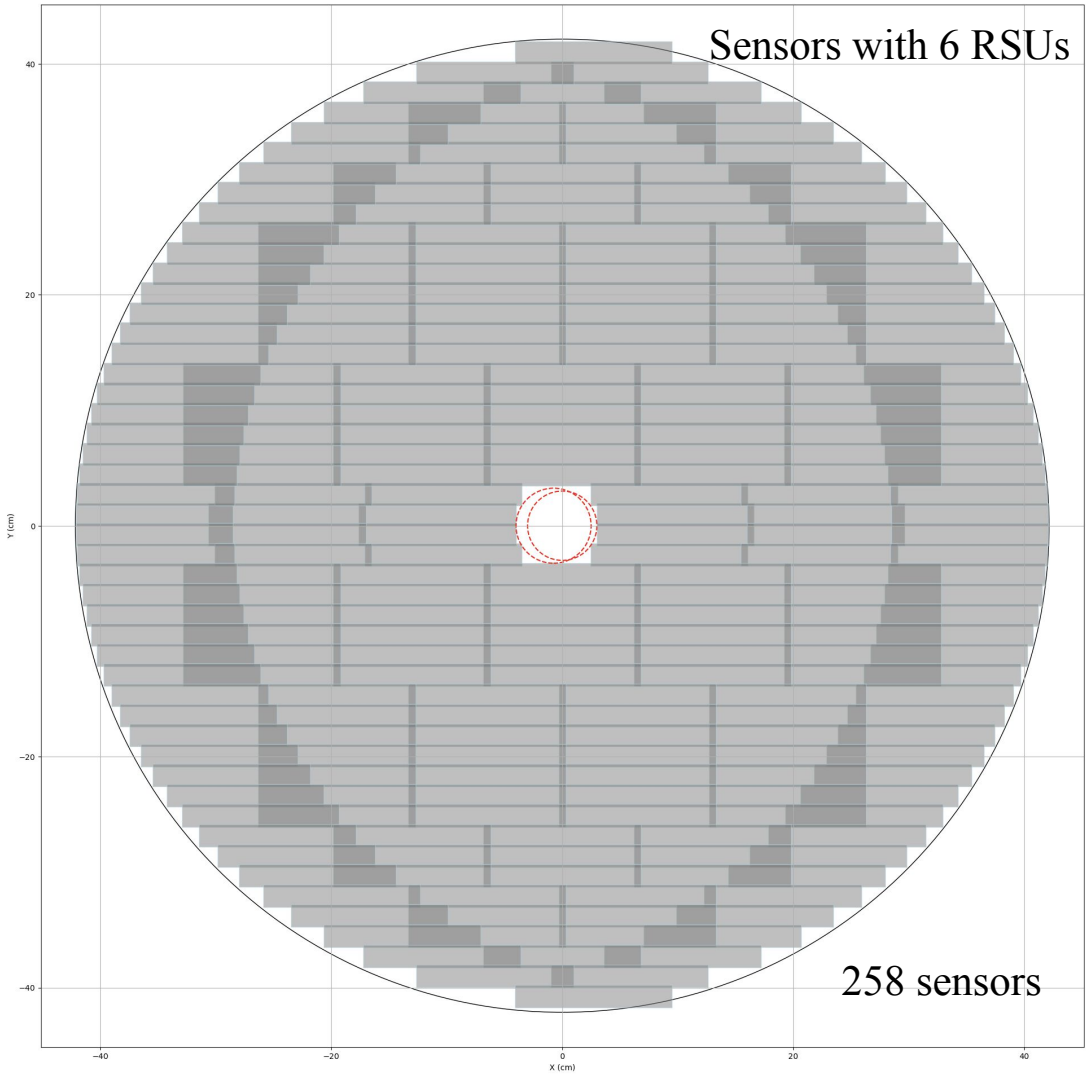
Region	Disk	z (mm)	Inner radius (mm)	Outer radius (mm)	X/X0
EE	ED2	-650	36.76	421.4	0.24%



Region	Disk	z (mm)	Inner radius (mm)	Outer radius (mm)	X/X0
HE	HD2	700	38.46	421.4	0.24%

ePIC SVT Disks - ED3/HD3

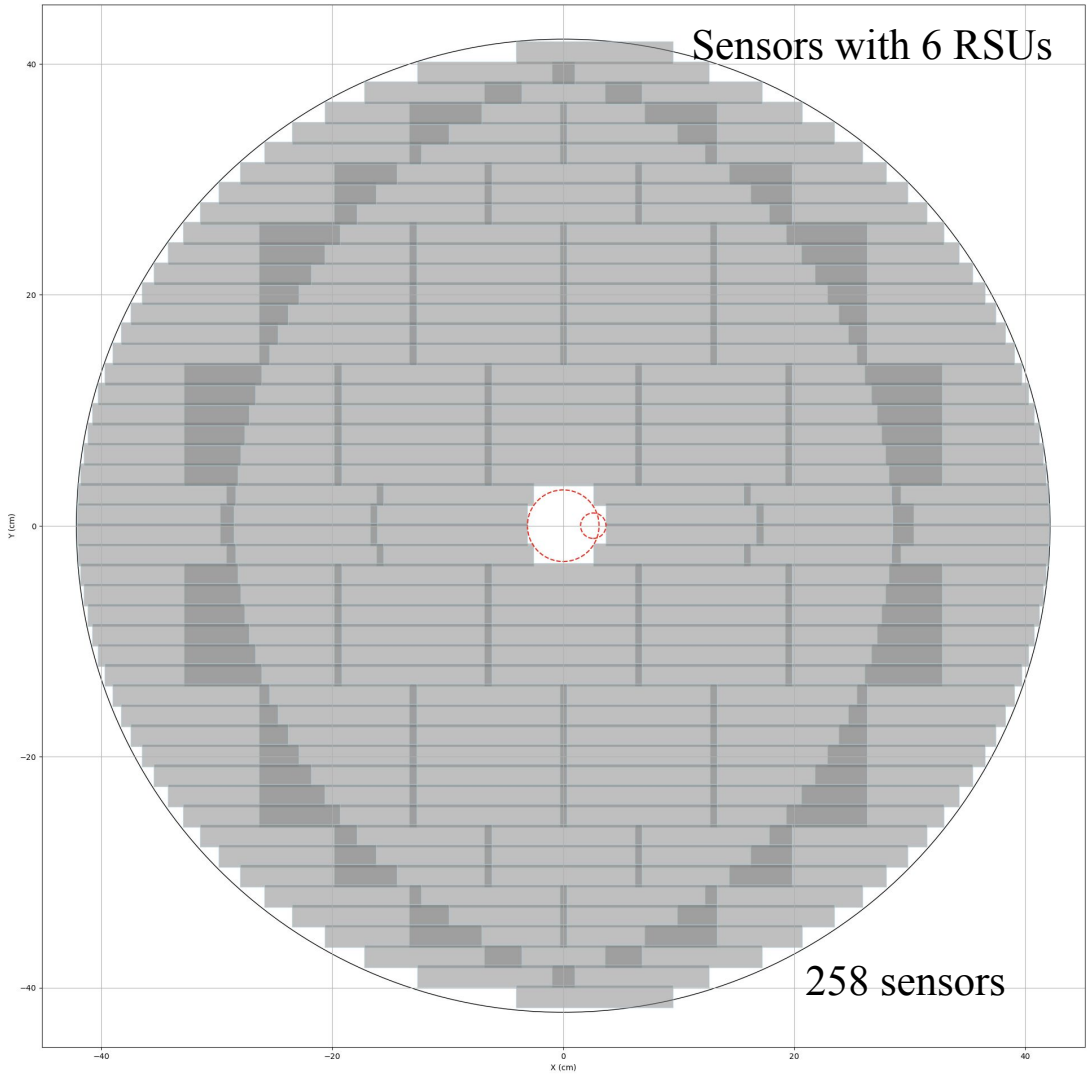




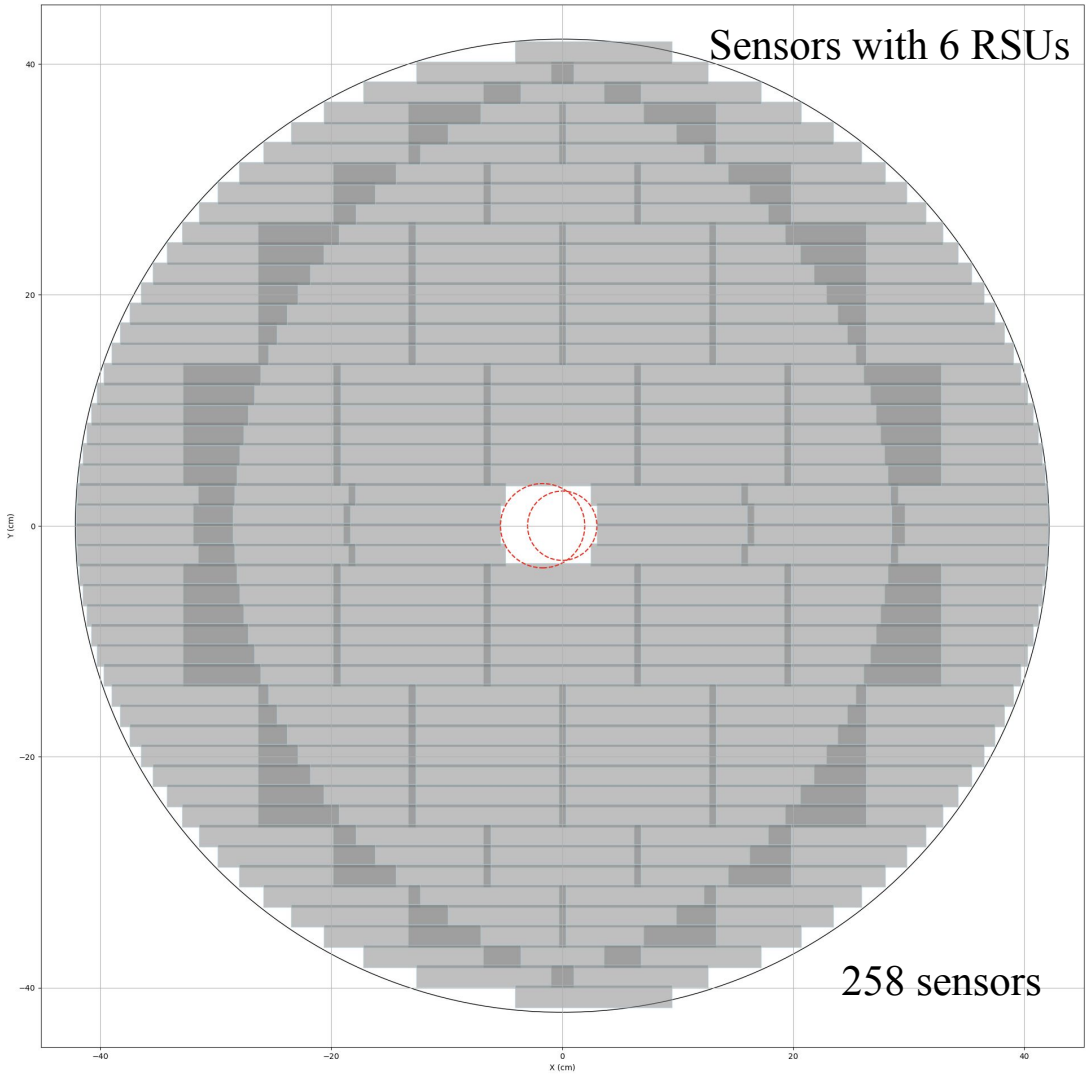
Region	Disk	z (mm)	Inner radius (mm)	Outer radius (mm)	X/X0
EE	ED3	-850	40.0	421.4	0.24%

Region	Disk	z (mm)	Inner radius (mm)	Outer radius (mm)	X/X0
HE	HD3	1000	30.0 @ C=(0,0) 32.5 @ C=(-7.5,0)	421.4	0.24%

ePIC SVT Disks - ED4/HD4

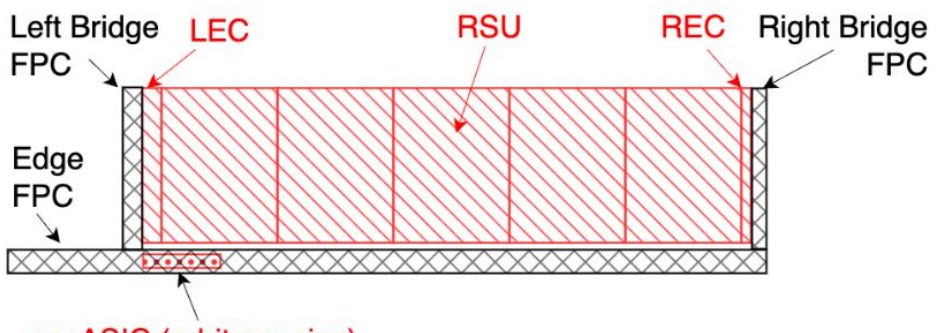


Region	Disk	z (mm)	Inner radius (mm)	Outer radius (mm)	X/X0
EE	ED4	-1050	31.0 @ C=(0,0) 11.0 @ C=(26,0)	421.4	0.24%



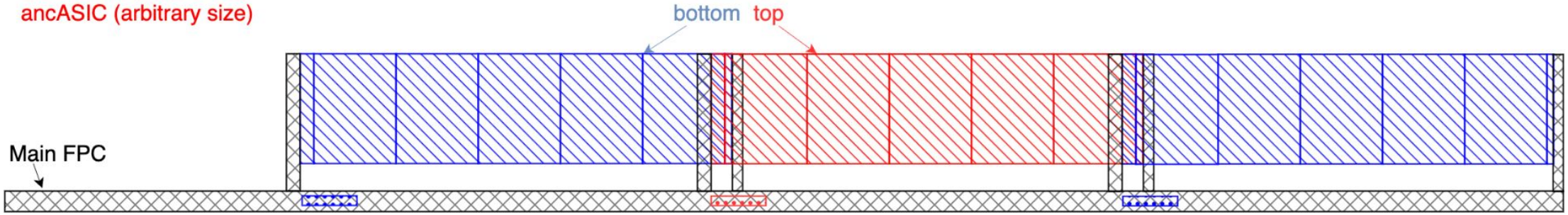
Region	Disk	z (mm)	Inner radius (mm)	Outer radius (mm)	X/X0
HE	HD4	1350	30.0 @ C=(0,0) 36.5 @ C=(-17,0)	421.4	0.24%

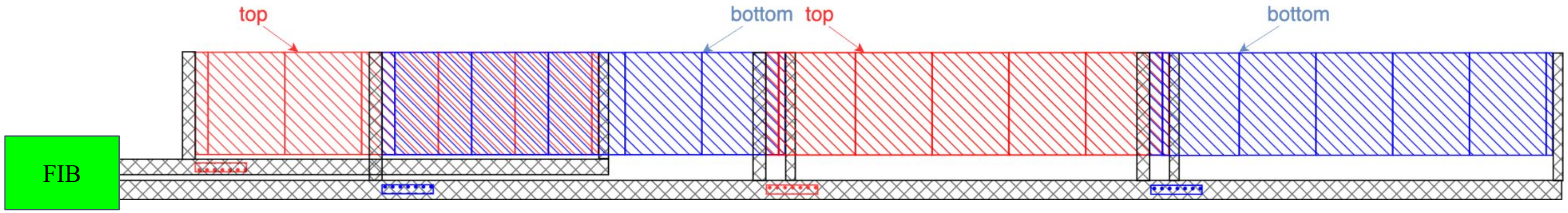
EIC-LAS Assembly for SVT Disks



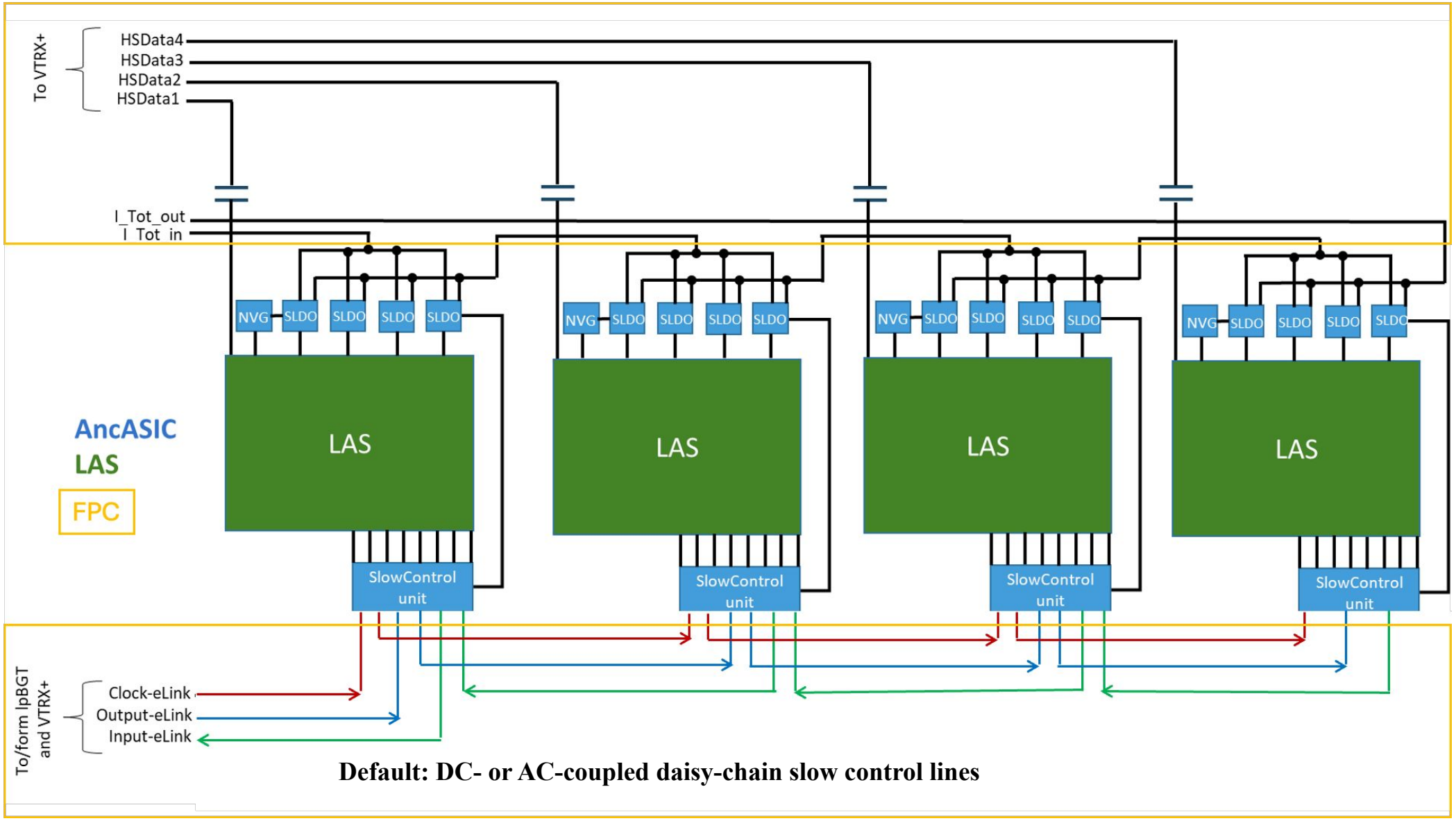
Left and right Bridge FPCs will connect to an EIC-LAS, and Main or Edge FPC.
A Main FPC will connect to FIB, up to 3 AncASICs and 3 pairs of Bridge FPCs.
An Edge FPC will connect to FIB, 1 AncASIC and 1 pair of Bridge FPCs.
AncASICs connected to Main and Edge FPCs on the same FIB will form a serial power current loop to maximize serial power efficiency.

Main FPC length <= ~40 cm, bridge FPC length ~30 mm



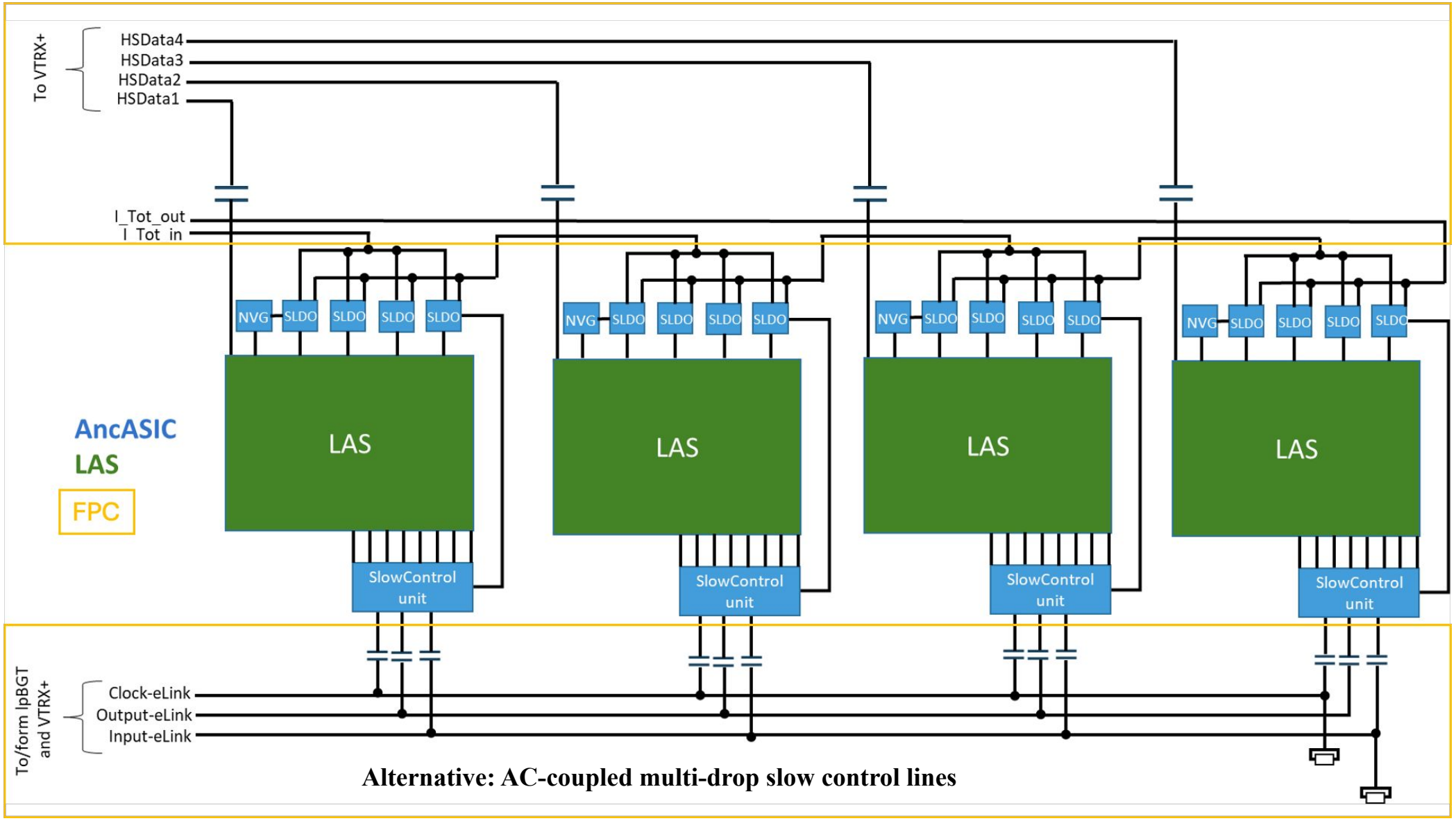


SVT Disks with EIC-LAS+AncASIC



Default: DC- or AC-coupled daisy-chain slow control lines

SVT Disks with EIC-LAS+AncASIC



Alternative: AC-coupled multi-drop slow control lines

SVT Disks with EIC-LAS+AncASIC

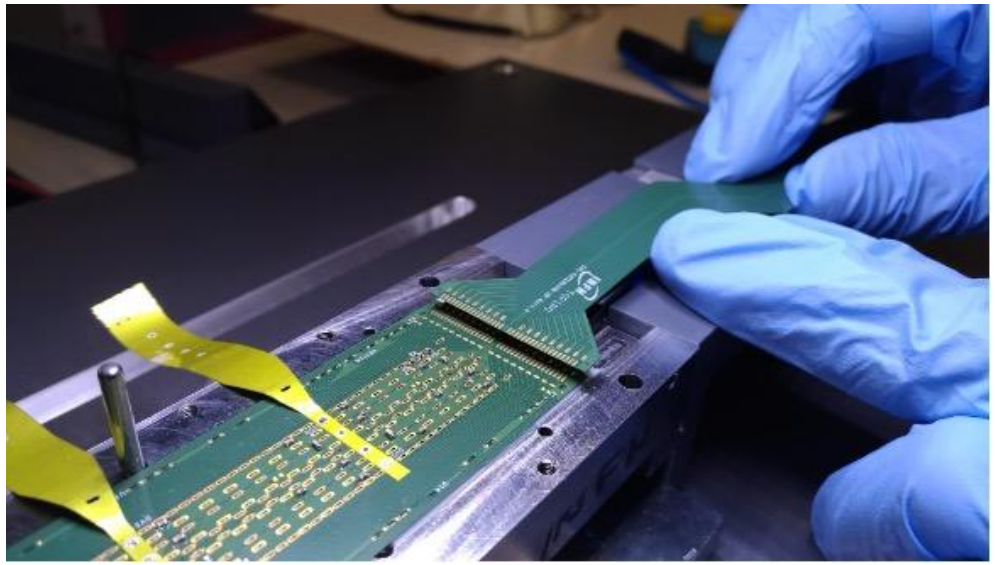
Signal	Rate	Comment	Type	Main FPC	Edge FPC	Left Bridge FPC	Right Bridge FPC
Power	N/A	DC power current from FIB to AncASIC	DC	Y	Y	Y	Y
SC_clk	40/160/320 MHz	Clock from lpGBT on FIB to AncASIC	AC/DC	Y	Y	Y	N
SC_in	40/160/320 Mbps	SC signals from lpGBT on FIB to AncASIC	AC/DC	Y	Y	Y	N
SC_out	40/160/320 Mbps	SC signals from AncASIC to lpGBT on FIB	AC/DC	Y	Y	Y	N
HS data	5.12/10.24 Gbps	HS data from EIC-LAS to VTRX+ on FIB	AC	Y	Y	Y	N
GCLK	160/320 MHz	Global clock from AncASIC to EIC-LAS	DC	No	Y	Y	N
SYNC GRSTB	N/A	SYNC/RESET from AncASIC to EIC-LAS	DC	No	Y	Y	N
SRVWR SCWR	5-10 Mbps	SC signals from AncASIC to EIC-LAS	DC	No	Y	Y	N
SRVRD SCRD	5-10 Mbps	SC signals from EIC-LAS to AncASIC	DC	No	Y	Y	N

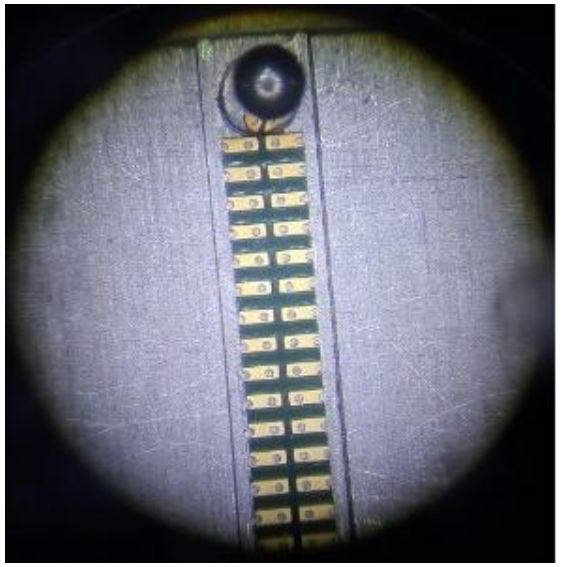
Electrical Interface Interconnects

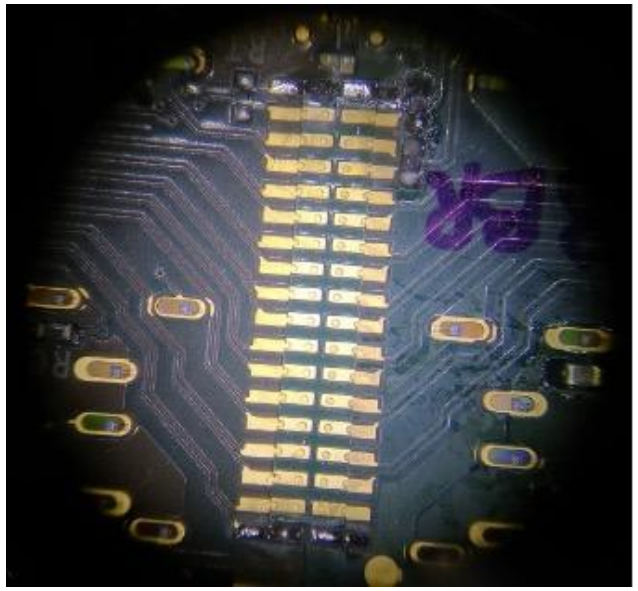
	FIB	Main/Edge FPC	Bridge FPC	AncASIC	EIC-LAS
FIB		Connector	N/A	N/A	N/A
Main/Edge FPC	Connector		**soldering**, wire/TAB-bonding	wire-bonding TAB-bonding	N/A
Bridge FPC	N/A	**soldering**, wire/TAB-bonding		N/A	**wire-bonding** TAB-bonding
AncASIC	N/A	wire-bonding TAB-bonding	N/A		N/A
EIC-LAS	N/A	N/A	**wire-bonding** TAB-bonding	N/A	

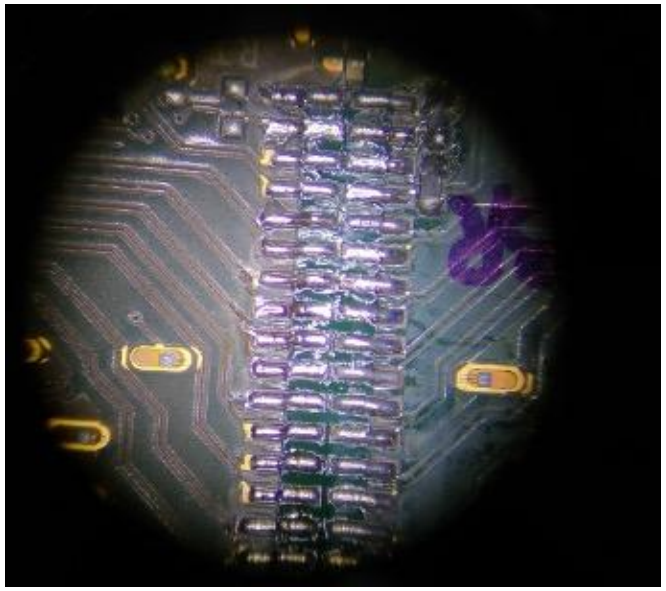
bold: preferred option

ALICE ITS2 FPC-to-FPC Soldering





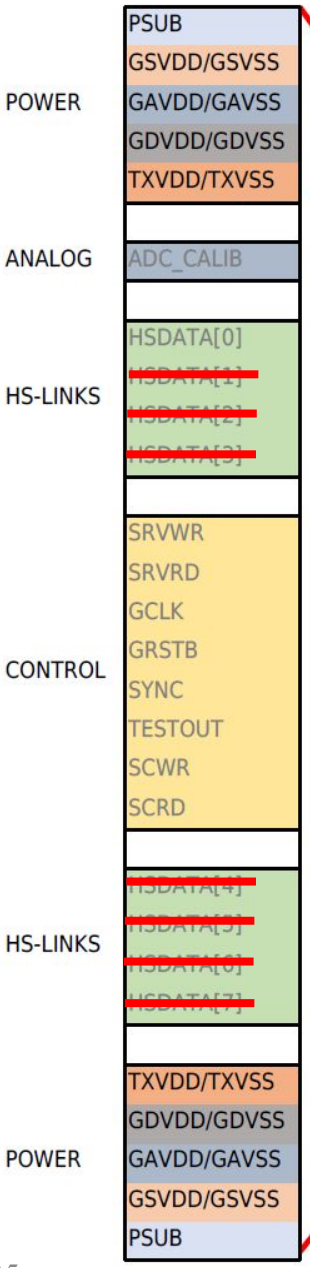




Summary and Plan

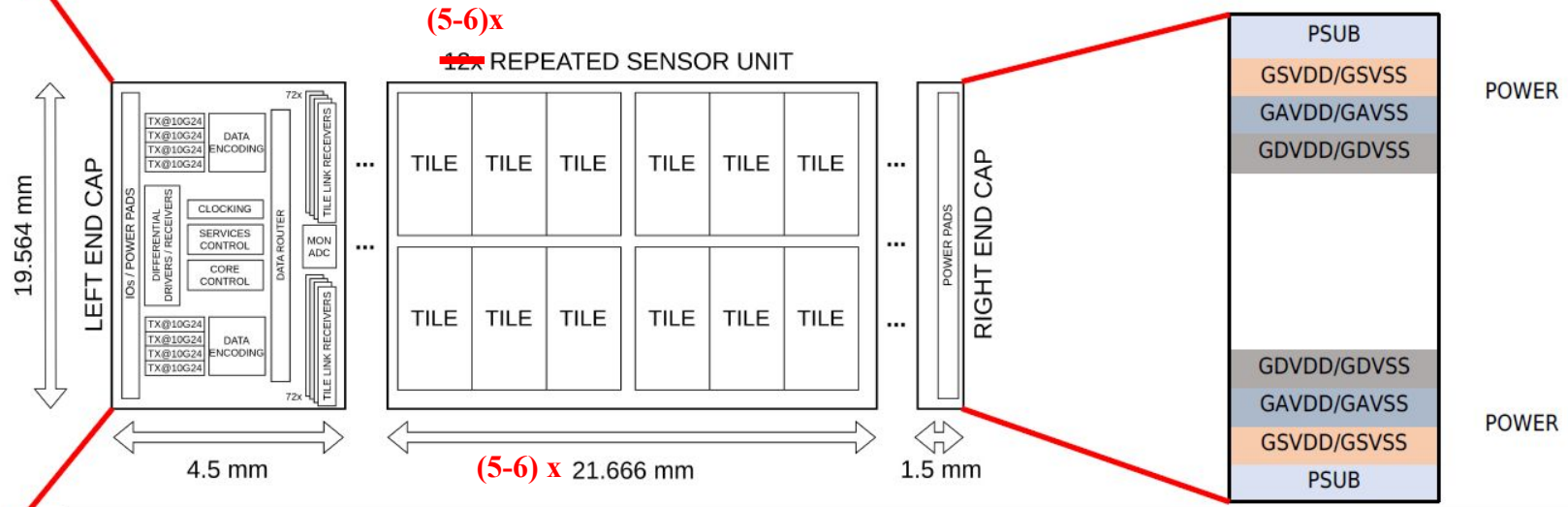
- Goals by LBL for SVT disk FPCs:
  - investigate how to interconnect different components - can learn from OB experience with LTU FPCs
  - validate power/signal integrity - can largely rely on OB studies on LTU FPCs
  - investigate connecting main and bridge FPCs by soldering
  - investigate connecting main and edge FPCs to FIB by connectors
  - investigate thermal and mechanical properties of the FPCs
  - develop relevant tooling and procedure for SVT module and disk assembly

EIC-LAS



Supply	Typical (mA)	Max (mA)
PSUB (-1.2V)		
GSVDD/GSVSS (1.2V/0V)	40	60
GAVDD/GSVSS (1.2V/0V)	170	270
GDVDD/GDVSS (1.2V/0V)	526	816
TXVDD/TXSVSS (1.8V/0V)	200	300

Signal	Frequency
GCLK	40/160/320 MHz
SYNC	N/A
GRSTB	N/A
SRVWR/RD	5-10 Mbps
SCWR/RD	5-10 Mbps
HSDATA0	5.12/10.24 Gbps

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GSVDD/GSVSS  : Global Services domain (1.2V/0V), always-on, used for on-chip services
GAVDD/GAVSS  : Global Analog domain (1.2V/0V)
GDVDD/GDVSS  : Global Digital domain (1.2V/0V)
TXVDD/TXVSS  : Serializer domain (1.8V/0V), only used for serializers
PSUB         : Substrate bias (-1.2V .. 0V), used for substrate biasing
Control pads : Powered by the services domain
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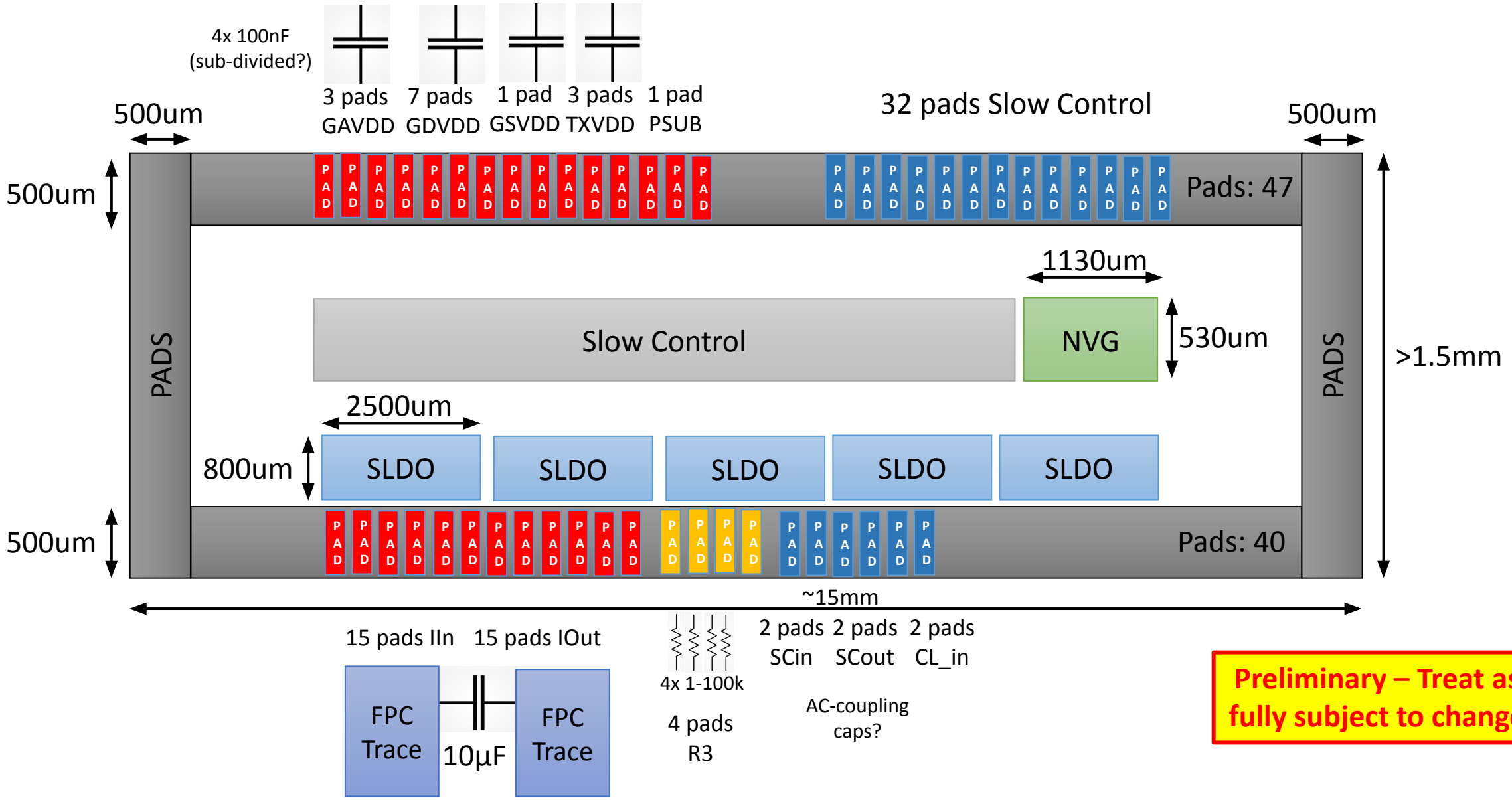
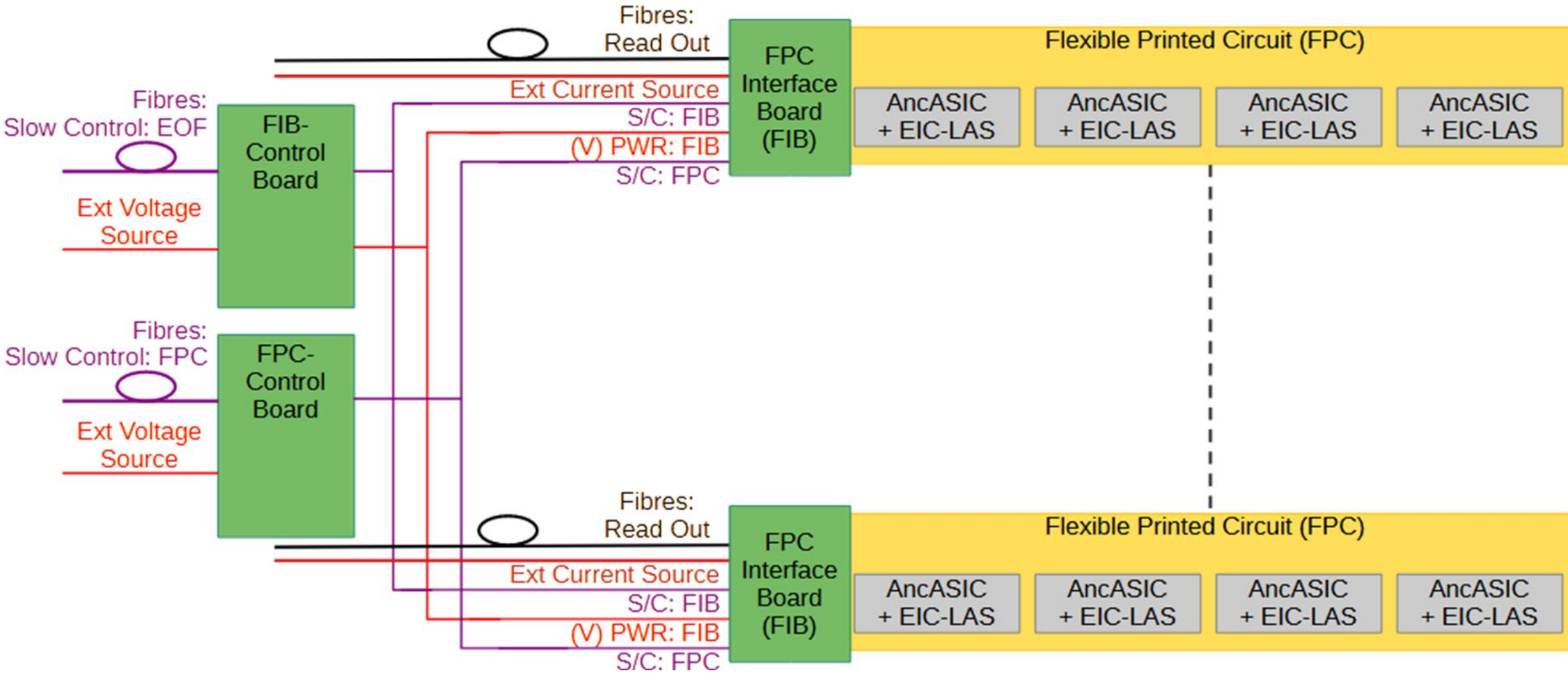
AncASIC



Preliminary – Treat as fully subject to change

SVT Disks with EIC-LAS+AncASIC



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