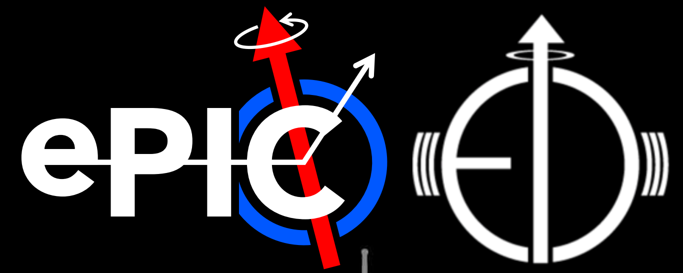
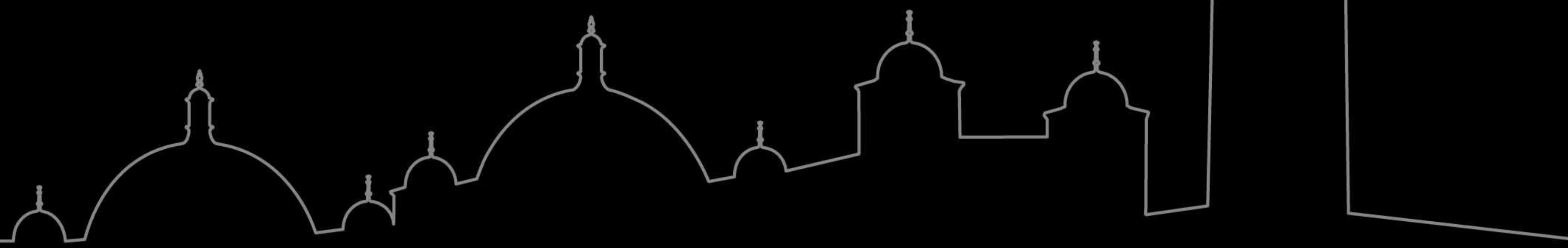


ePIC SVT FPC, ancillary ASIC placement, and bonding

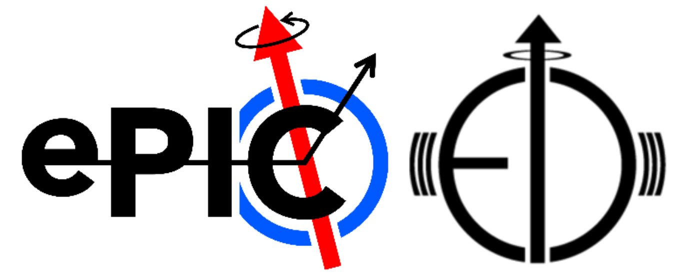
James Glover & Eve Tse

ePIC SVT DSC Meeting

Tue, 26th November 2024

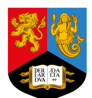


Previous FPC Bonding Discussions



- Bond discussions previously held at WP3 (Electrical Interfaces) and UK meetings:
  https://indico.bnl.gov/event/23952/#3-prototyping-ob-fpc
- These have compared the FPC bond options:
  - spTAB – LTU's recommended bond technique.
  - Wire bonding – likely to be required for EIC-LAS (inherited from MOSAIX).
- Current baseline is to use just one bond method between bridge FPC (b-FPC) and chips*.
  - If LAS requires wire bonding, this is preferred for AncASIC also.

* (EIC-LAS or AncASIC).



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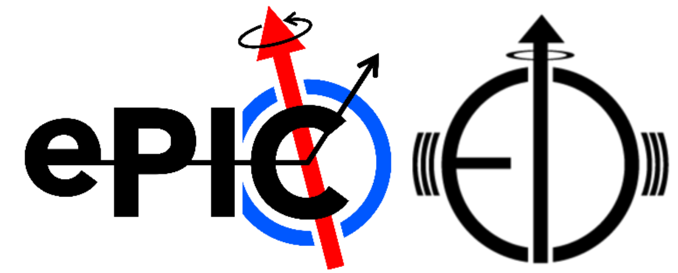
FPC – 2 layer circuit

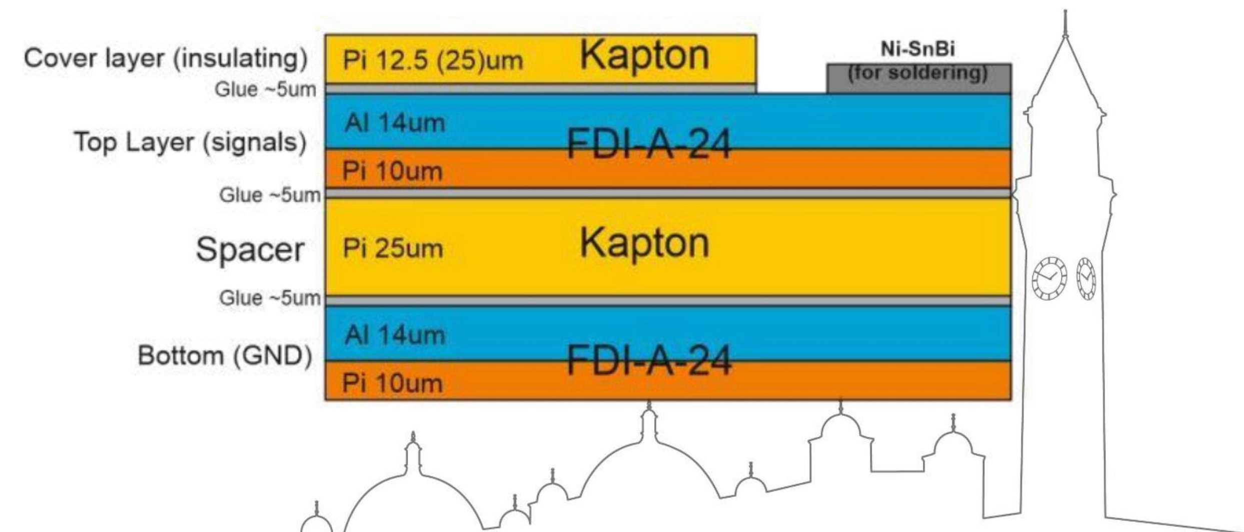


The FPCs (of the OB and discs) are only to have 2 conductor layers.

- No option for overlapping tracks.

For connections between AncASIC and EIC-LAS:

- FPC can be used as pitch adaptor.
- FPC can't be a redistribution layer.
- ∴ AncASIC pads need to mirror EIC-LAS (MOSAIX) pads.



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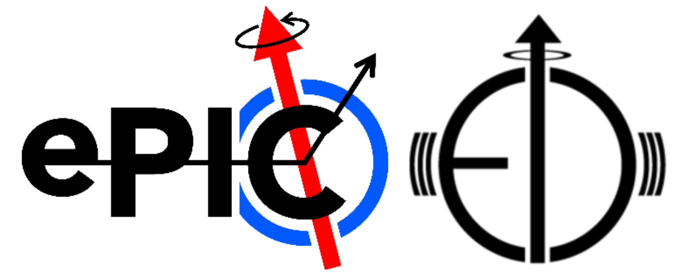
FPC as a pitch adaptor



- EIC-LAS and AncASIC are different widths.
- # of bond pads are similar.
- ∴ pad pitch must differ.
- FPC traces are used to change pitches.
- Wire bonds stay parallel.

EIC-LAS

FPC trace

Bond wire

Bond pad

AncASIC

b-FPC

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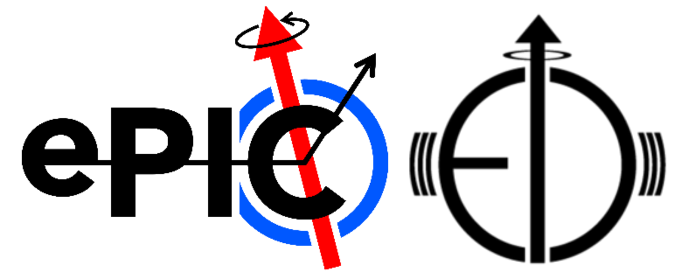
Number of bond pads on MOSAIX



- Currently this has not been made public.
- This could be because ITS3 are still finalising the MOSAIX design and pads may still change.
- Test PCBs are being designed for the full MOSAIX chip, a near final pad layout should exist.
- Best guess is between 80 and 150 bond pads
- At a pad pitch of 100 μm*, this is a pad array length between 8 and 15 mm.
  - This is half the pitch currently on the prototype FPC*.

* 50 μm pad, 50 μm gap (assumed minimum for 25 μm bond wire).

* 70 μm trace width, 130 μm gap.

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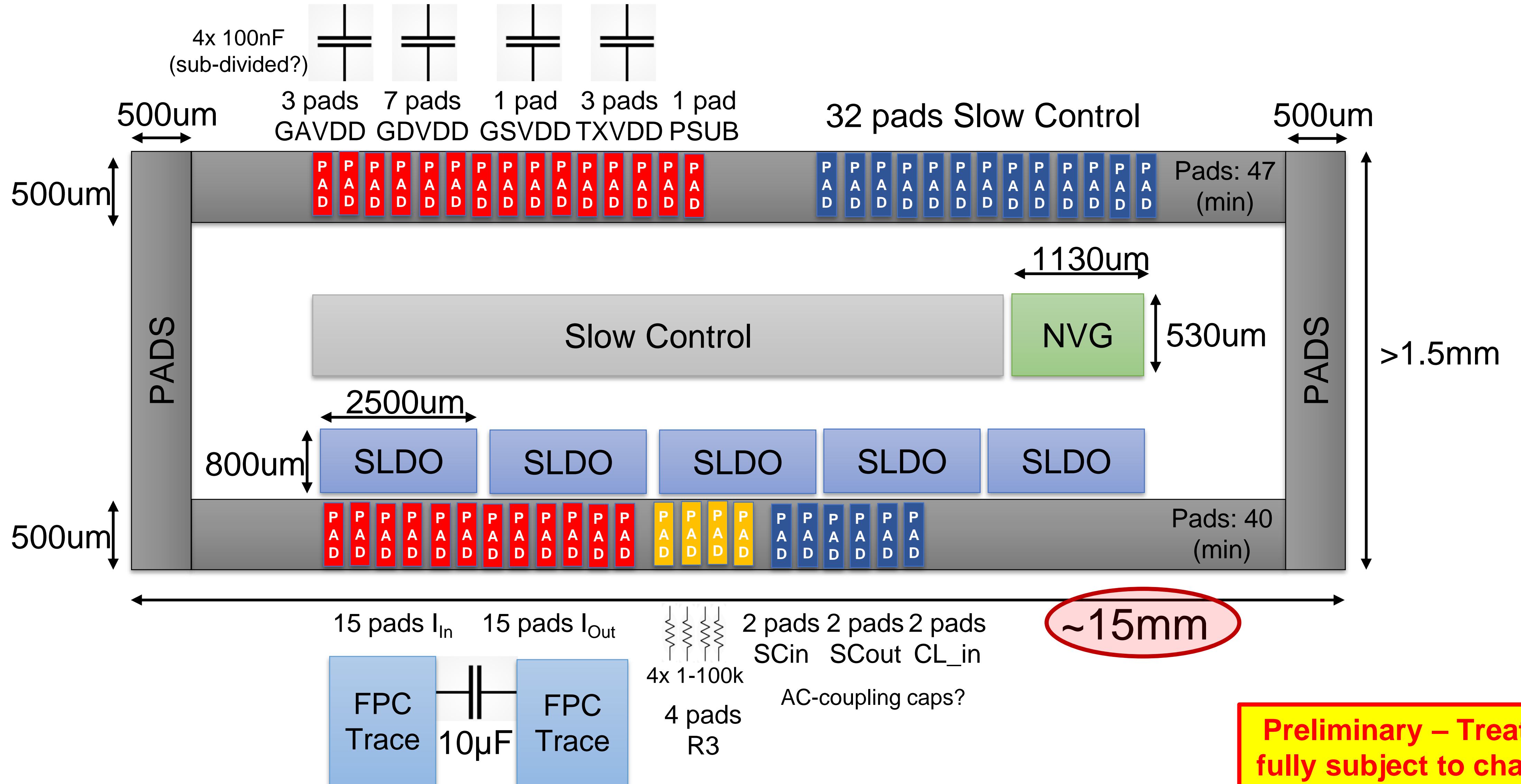
AncASIC Size and Pads

From Iain Sedgwick (STFC): https://indico.cern.ch/event/1463541/contributions/6226081



Preliminary – Treat as fully subject to change

AncASIC Size and Pads

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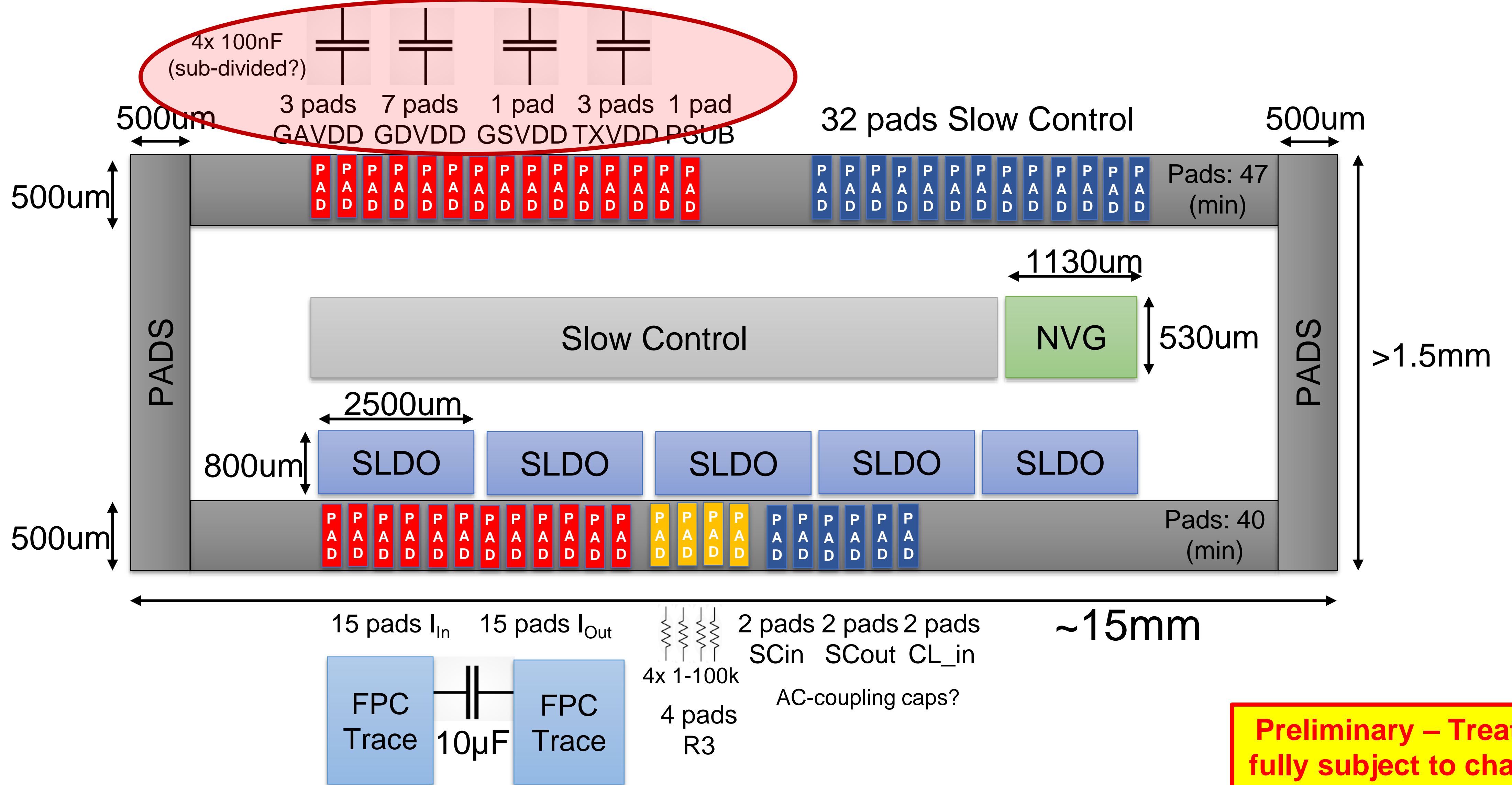
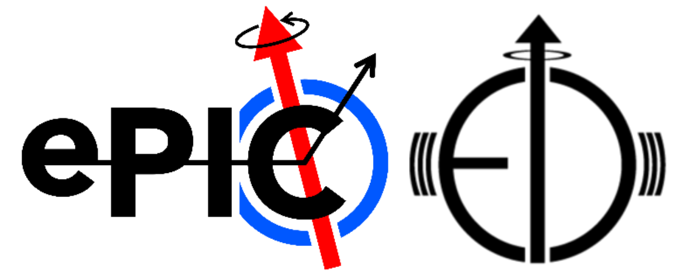


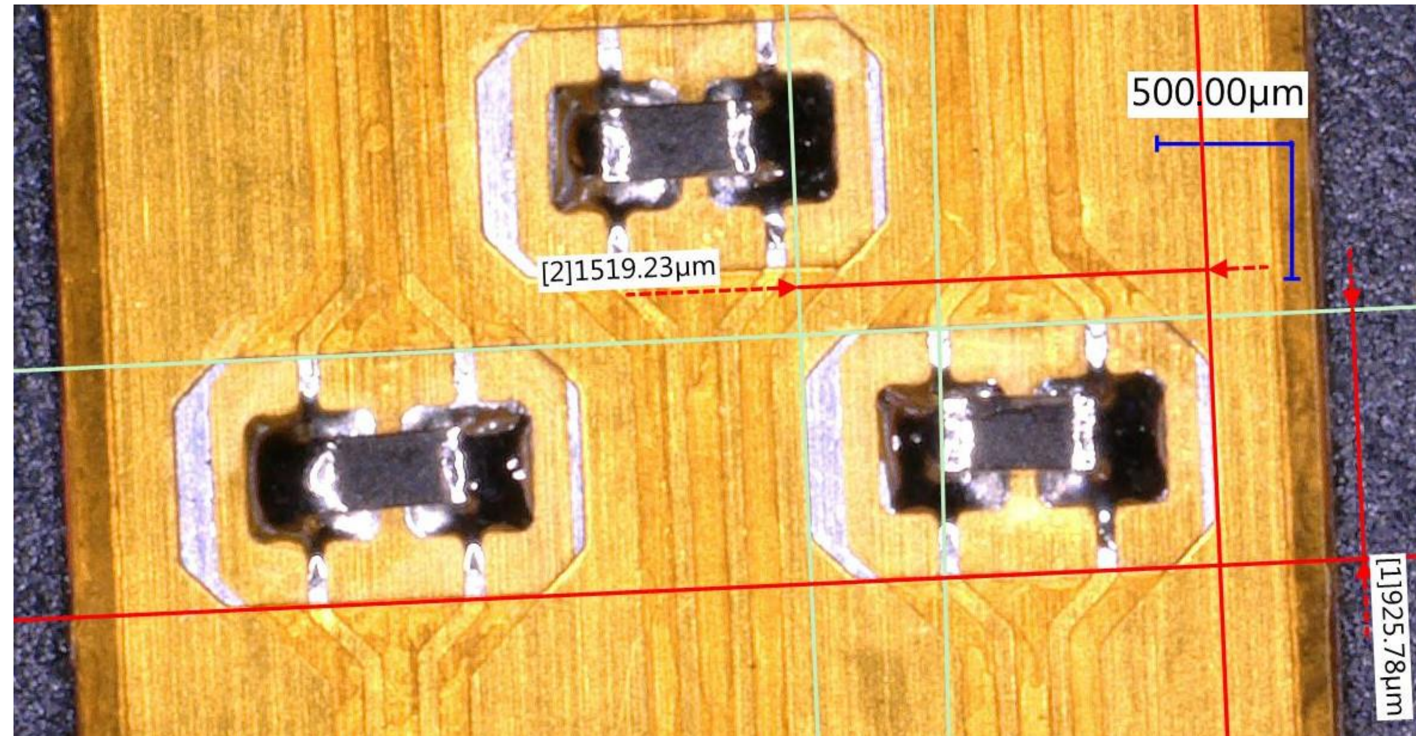
Preliminary – Treat as fully subject to change

Caps between AncASIC & LAS



Example from LTU-made prototype FPC.

- On FPC components: 0201 (imperial).
- Sit within a 1 × 1.5 mm window.
- Exact position on b-FPC depends on location of (MOSAIX) pads for the power domains.
    - Number of caps needed is still to be determined.



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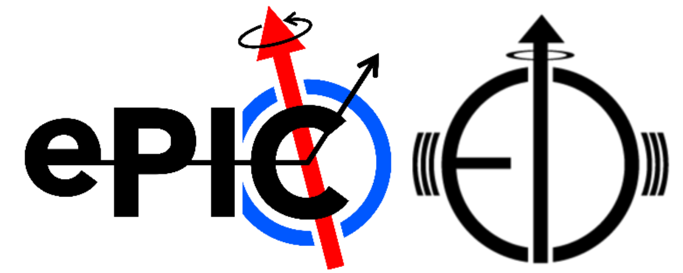
Wire bond spacing



Assumed 25 µm bond wire on a 50 µm bond pad.

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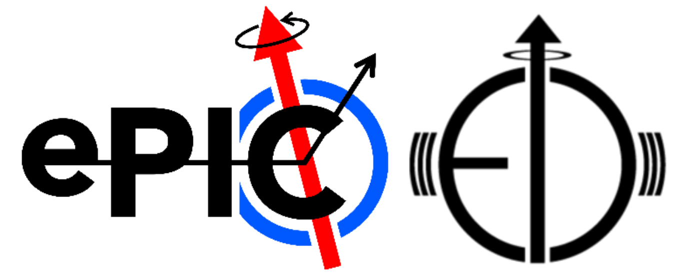
Wire bond spacing



Assumed 25 µm bond wire on a 50 µm bond pad.

Bond pad

AncASIC

Cap

EIC-LAS

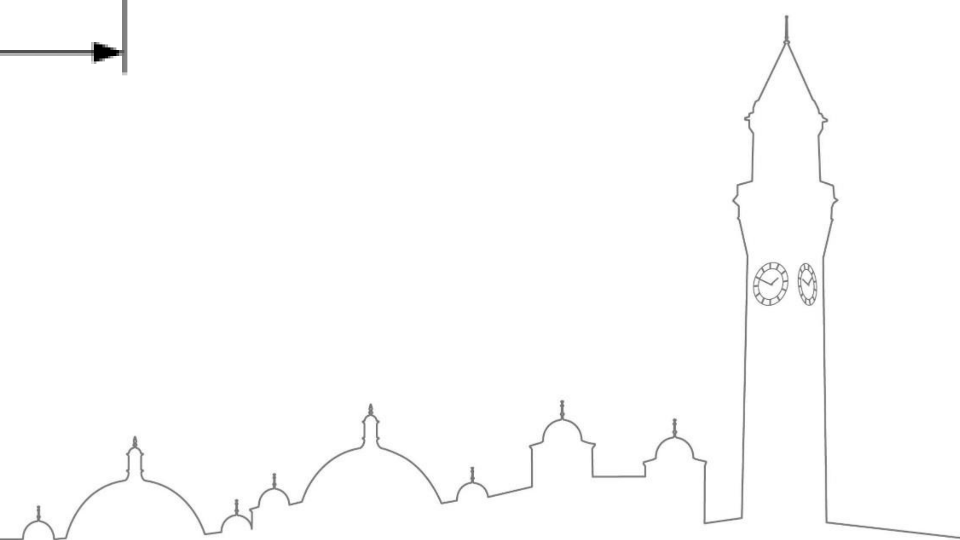
300 µm

300 µm

50 µm

2,300 µm

Bridge FPC



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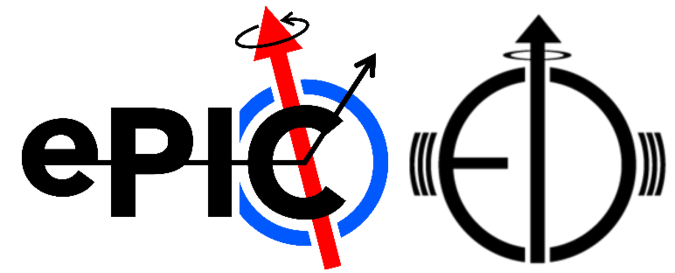
Data lines are not part of AncASIC



At least one data trace will need to be run under the AncASIC.

EIC-LAS

FPC trace

Bond wire

Bond pad

AncASIC

Data trace

b-FPC

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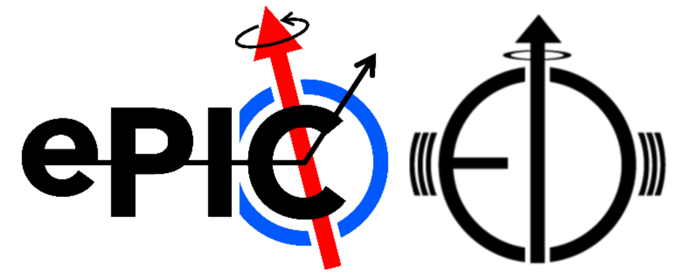
Traces also come into AncASIC



Power and slow control traces also need to come into the AncASIC from the main FPC (m-FPC).

- Power will require many pads!
- S-LDOs also need additional pads for configuration resistors.

EIC-LAS

b-FPC trace

Bond wire

Data trace

Bond pad

AncASIC

Traces to m-FPC (few mm)

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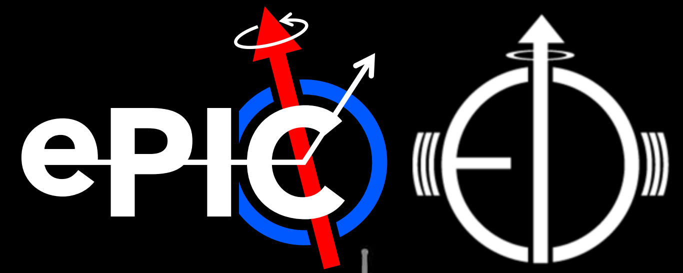
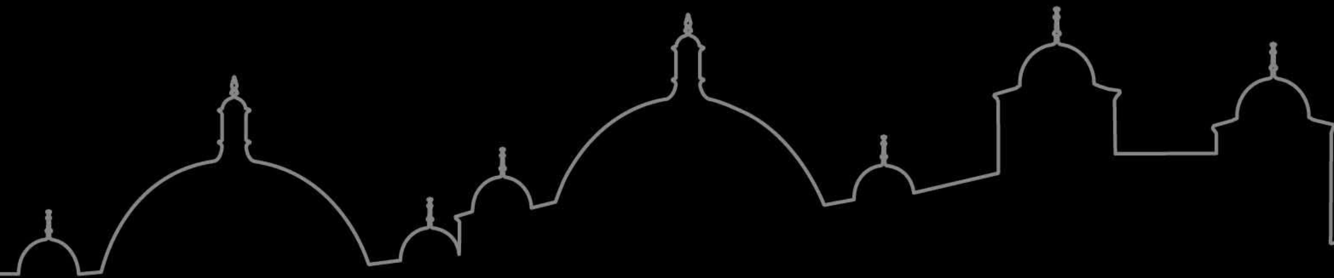


Thank you very much!

(Especially to I. Tymchuk & others @ LTU, M. Borri, A. Hill, I. Sedgewick, G. Viehhauser)

Any questions?



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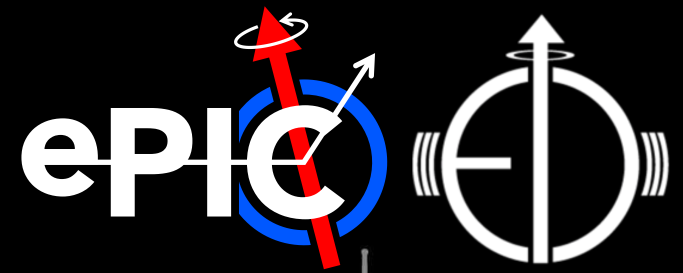
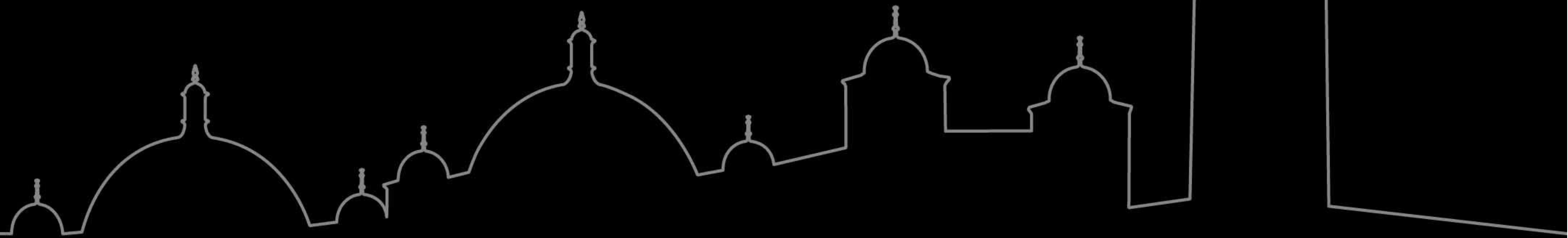
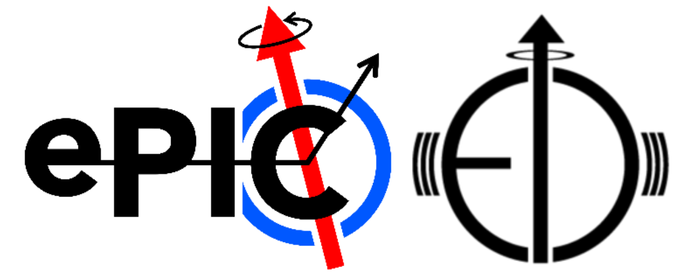


Additional (support) slides



45° wire-feed



Assumed 25 μm bond wire on a 50 μm bond pad.

Bond pad

Bridge FPC

AncASIC

Wedge tool

45°

Cap

EIC-LAS

300 μm

300 μm

50 μm

300 μm

50 μm

300 μm

1,000 μm

300 μm

50 μm

300 μm

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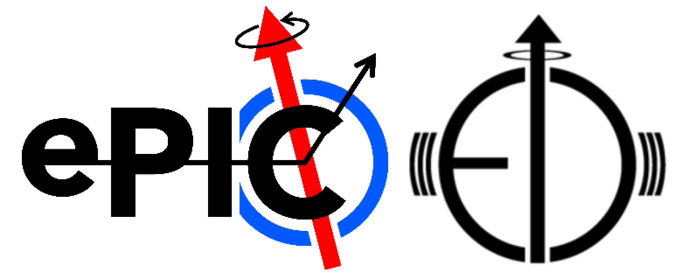
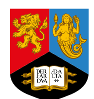
Connections needed



- The AncASIC is needed for the powering and slow controls.
- Data can be readout from EIC-LAS directly.

Element	Power	Data	Slow Controls
EIC-LAS	✓	✓	✓
AncASIC	✓	✗ *	✓
FPC	✓	✓	✓

* Adding data connections to the AncASIC would just be a passthrough (EIC-LAS to AncASIC to FPC). Why add the extra connection point (point of failure)? However, it is only 1 channel (2 pads/traces).



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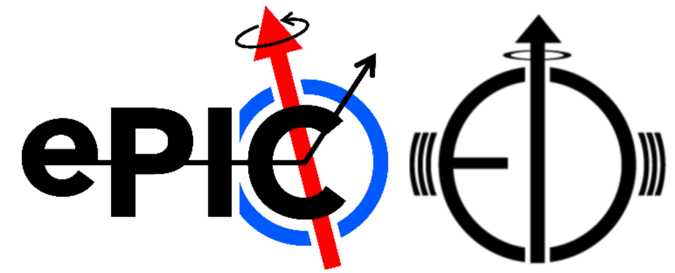
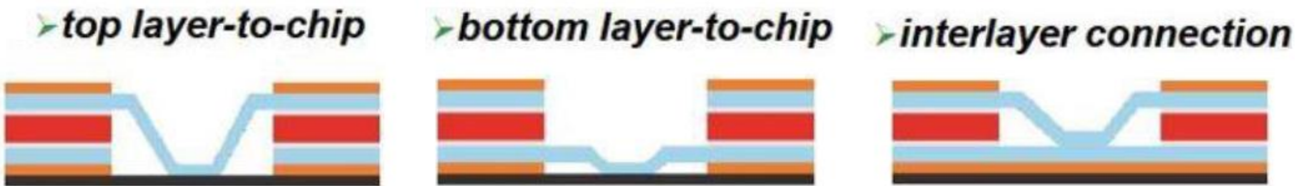
spTAB vs wire bonding



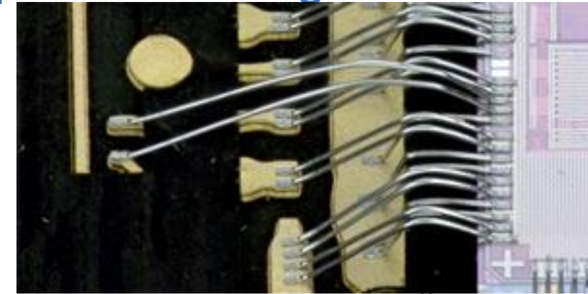
spTAB

- FPC traces have opening in support at bond locations.
- Aluminium trace (of FPC) is directly welded to a pad on the chip*.
- Foil width: ~70 μm.
- Best when FPC is above the chip*.
- Recommended by LTU.
  - Wire bonding to FPC is possible.



Wire bonding

- Wire connection between pads on 2 separate substrates (chip* or FPC).
- Wire width: ~25 μm (15-50 μm)
- Best when FPC is below the chip*.
- The current base-line for the ITS3 MOSAIX chip.
  - spTAB is being considered.



* (EIC-LAS or AncASIC).

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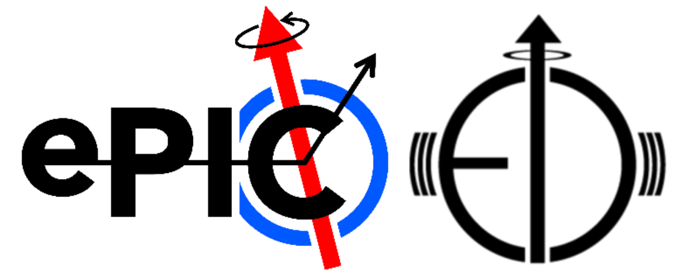
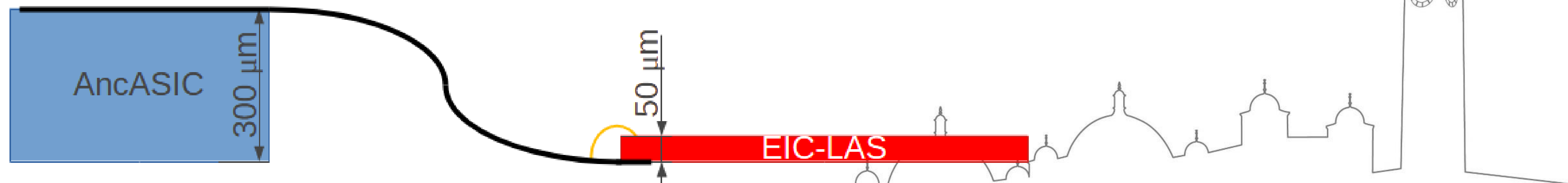
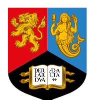
AncASIC vs EIC-LAS



- We are designing the AncASIC – we can dictate pad size, shape, pitch, and location.
- EIC-LAS (based on MOSAIX) will have a pad design dictated by ITS3.
  - If they finalise a pitch too small for spTAB, we will have to wire bond!
- Mixed bonding is possible (spTAB for AncASIC and wire bonds for EIC-LAS), but the FPC would have to bend from top of AncASIC to bottom of EIC-LAS (assumed 300 µm height difference).
- The FPC has a min bend radius of 5 mm, this dictates a 2.5 mm (larger) gap between chips to account for the curve!

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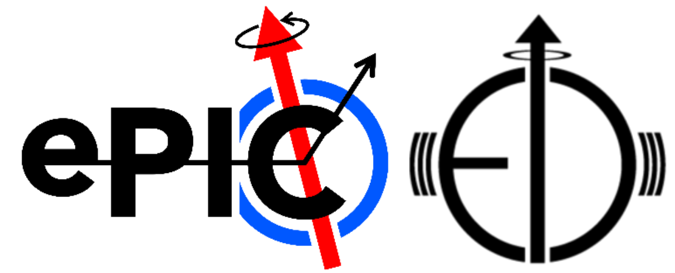
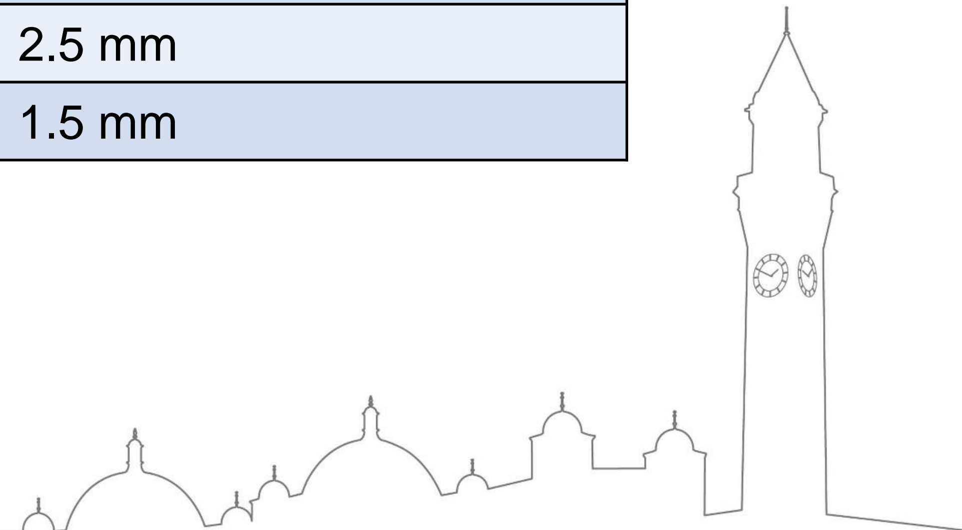
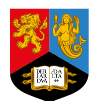
AncASIC thickness



Changing the thickness of the AncASIC would adjust the minimum spacing between AncASIC and EIC-LAS, if mixing spTAB and wire bonding.

AncAISC thickness (µm)	Spacing needed to accommodate 5mm bend radius of FPC
725 (assumed default)	3.8 mm
300 (easily thinned to)	2.5 mm
100 (added complexity)	1.5 mm





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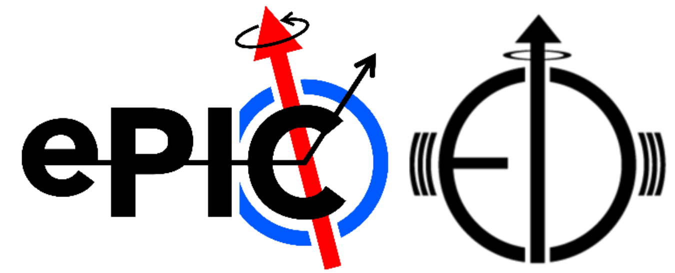
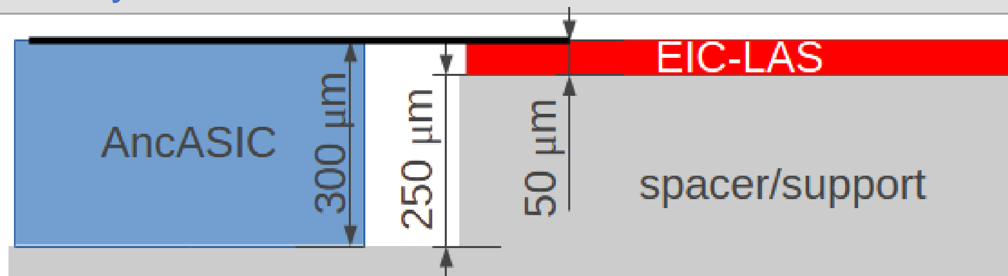
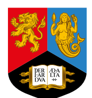
All spTAB



- One bond process would make the production easier.
- To avoid the spacing implication of different surface heights, top of EIC-LAS and AncASIC need to be level.
  - Requires tooling to account for different chip thicknesses.
- Sites (currently) have more expertise with wire bonding.
  - Time needed to change wedge tools in bond machines.
  - Machines (currently) shared with other projects that require wire bonds.
  - A lot of tool changes to accommodate the many projects*.

* May be less of an issue if/when a dedicated bonder is available.

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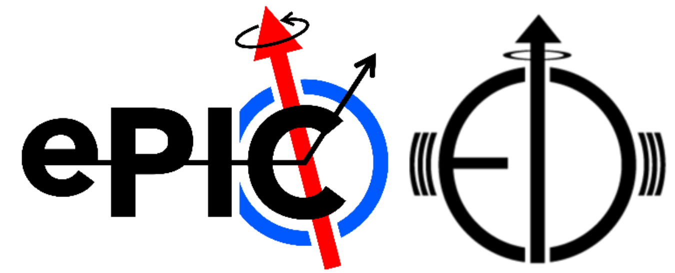
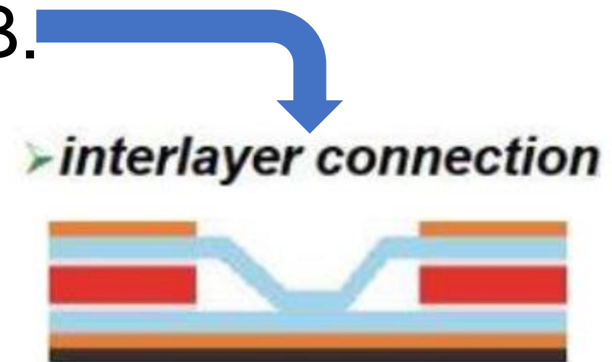
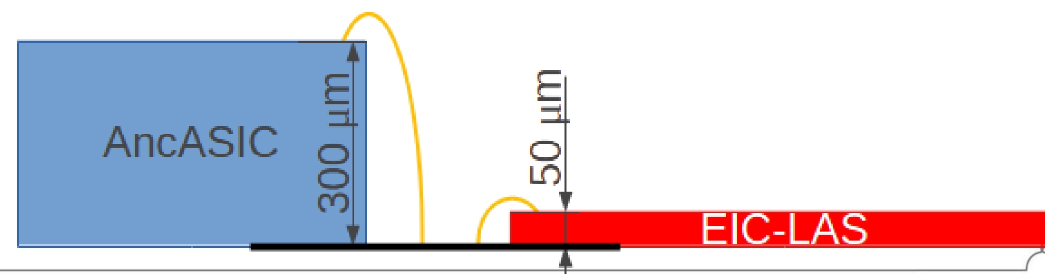
All wire bonds



- One bond process would make the production easier.
- Sites (currently) have more expertise with wire bonding.
  - No time lost due to changing wedge tools in bond machines.
  - Easier to share machines across projects.
- No special tooling required to get surfaces level.
- FPC interlayer connections still need spTAB.
  - Therefore, we would need to request this to be done by LTU.





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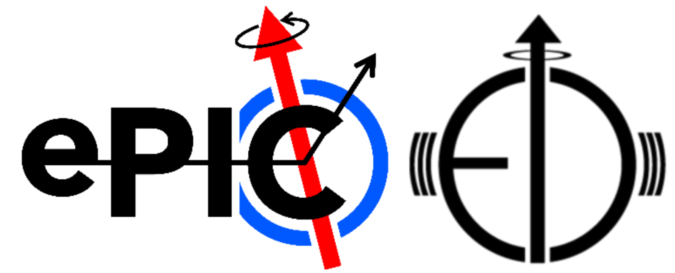
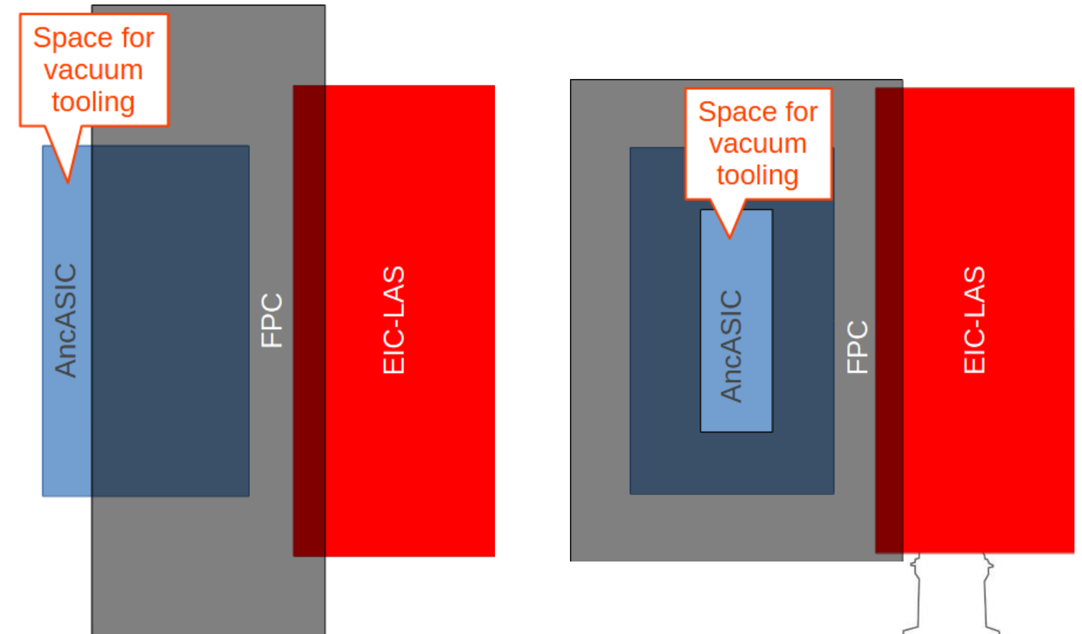
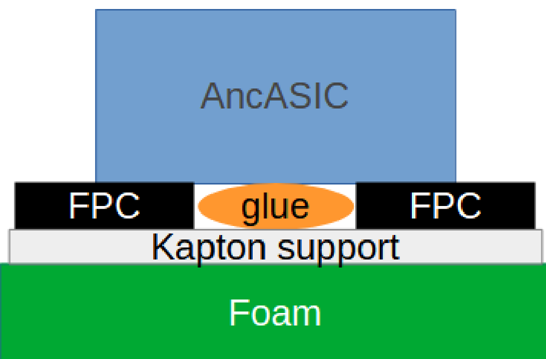
FPC design to fit assembly



Regardless of whether the FPC is above or below the AncASIC, there are still complications.

- FPC above (spTAB) – we need space for vacuum tooling to pick up the AncASIC (opening in FPC or uncovered edge).
  - Relying on bonds to hold AncASIC!





- FPC below (wire bond) – we want good thermal path to carbon foam (conductive glue within opening on FPC).
  - Relying on glues to hold FPC and Kapton!

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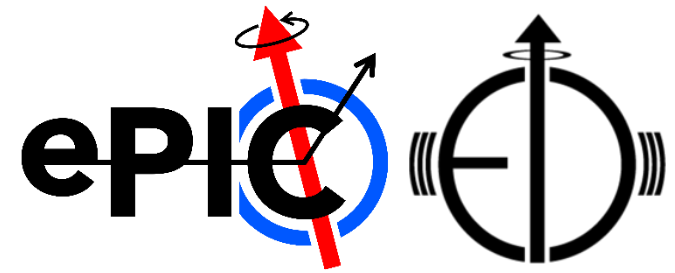
Mixing flat and curved silicon



- Mixing a flat AncASIC on a curved stave adds complexity.
- To build modules flat, there needs to enough tolerance in Kapton support layer and FPC to still follow curvature of stave.
- Can not bond a flat surface to a curved surface.
- We become very dependant to finding the right glues.
  - For structural support, while enabling curvature and a thermal path.
- Assembly sequence is dictated by bond choice.
  - spTAB (FPC above chip), or wire bond (FPC below chip).

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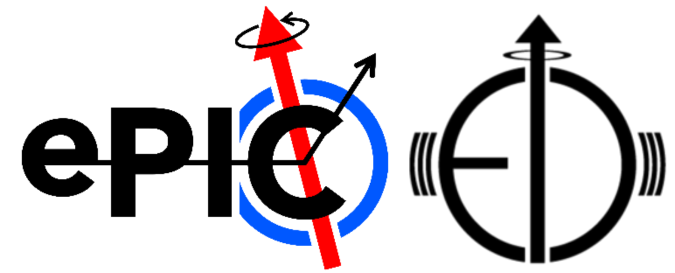
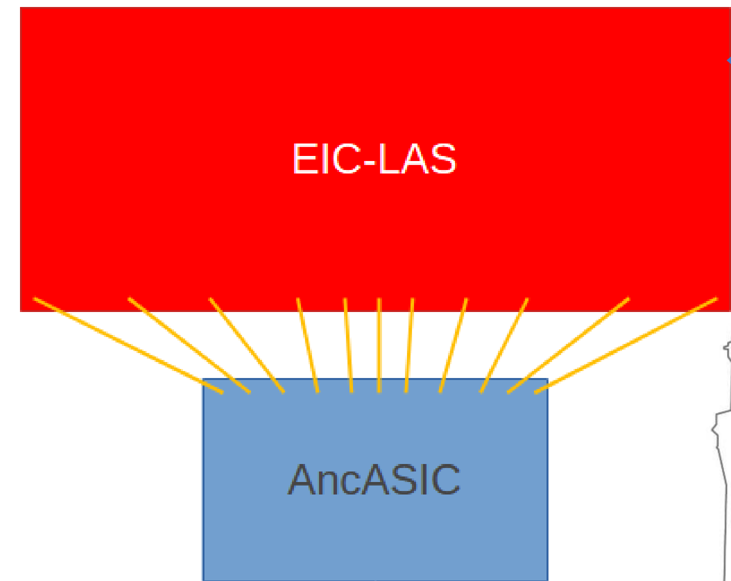
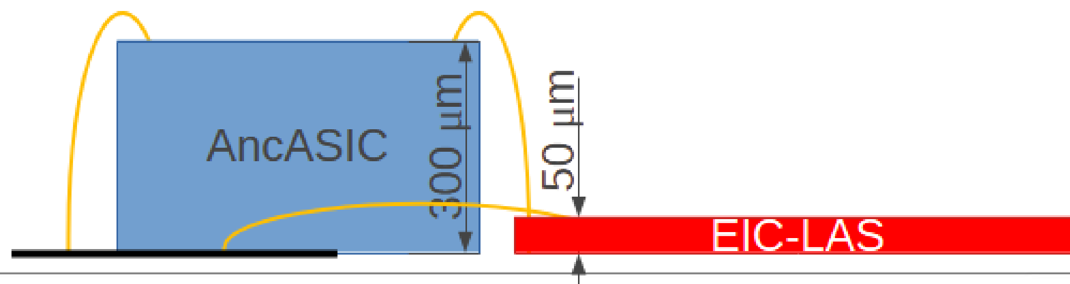
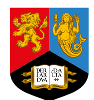
Should we bond chip-chip?



- We could bond directly between AncASIC and EIC-LAS (without interconnects through the FPC) – assuming bond angles fit with different chip widths and predominately on 1 chip edge.
- Data channel would need to be bonded directly to FPC (from EIC-LAS).
- Requires the data channel to be located conveniently (e.g. near to one edge of EIC-LAS.



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