FEBs for ePIC MPGDs

Technical and organizational choices

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MPGD-DSC general meeting

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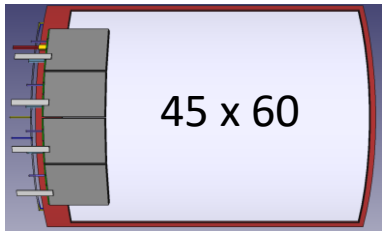
Outlook

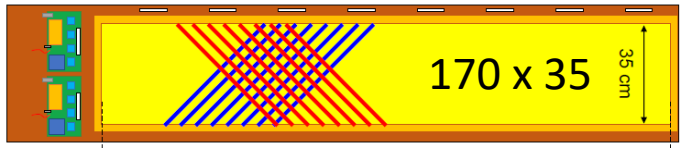
- Considered readout architecture
- Low voltage powering
- Frontend partitioning
- Space constraints
- Summary

Reminder on MPGD sub-systems and channel counts

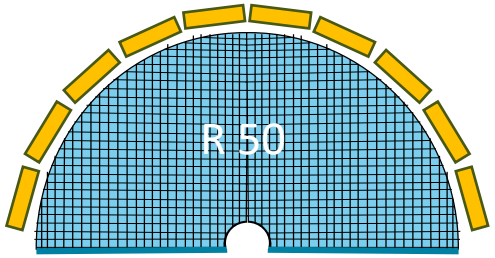
- Cylindrical Micromegas Barrel Layer : CyMBaL : ~30k channels
  - → 32 tiles of 1024 channels each



- µRWELL Barrel Outer Tracker : µRWell-BOT : ~100k channels
  - → 24 modules of 4 096 U-V strips each

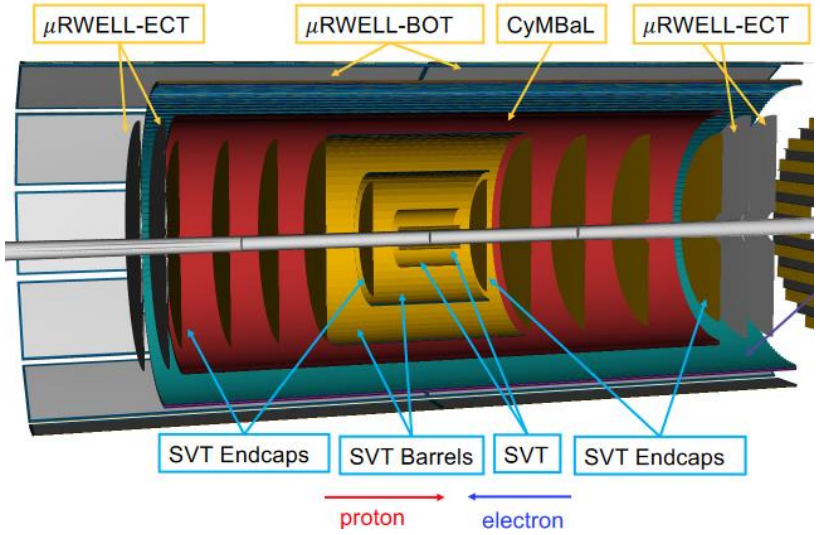


- µRWell End Cap Tracker : µRWell-ECT : ~30k channels
  - → 8 half-disks of 4 000 X-Y strips each



- ~160k-channel heterogeneous system
  - → Micromegas, µRWell, barrel, endcap, curved, planar, circular

- Common approach to acquire data from different types of ePIC MPGDs
  - → Use same frontend ASIC
    - Salsa – under development
  - → Share frontend design between groups
    - Adapt form factor if needed



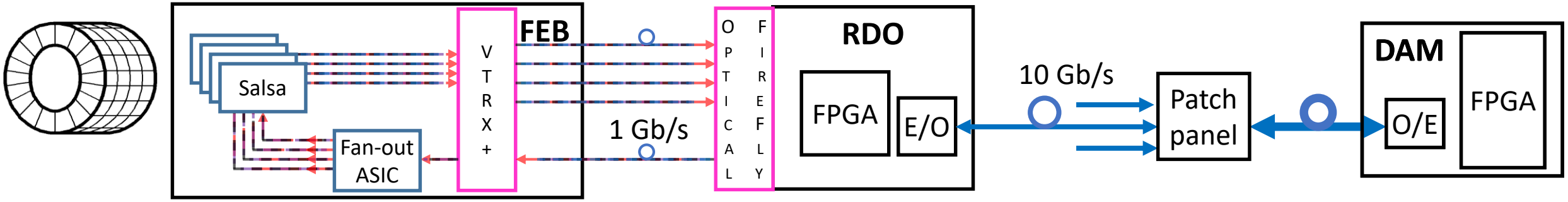
Options for MPGD architectures

On-detector

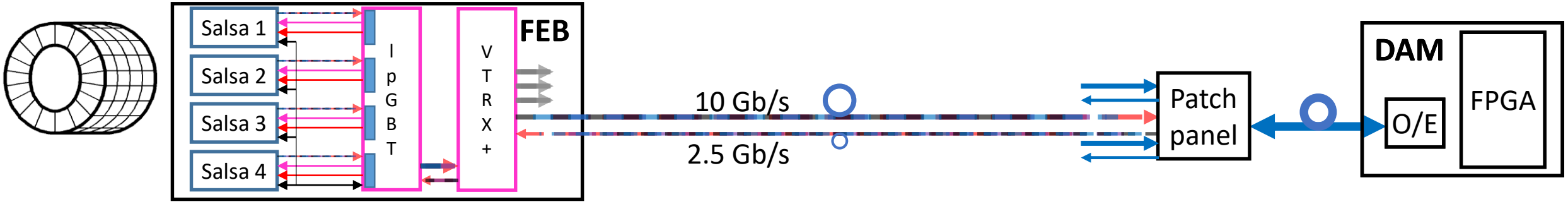
Low restriction area

Low restriction area

- Option 1 : FEB-RDO-DAM based on direct Salsa-VTRX+ interface

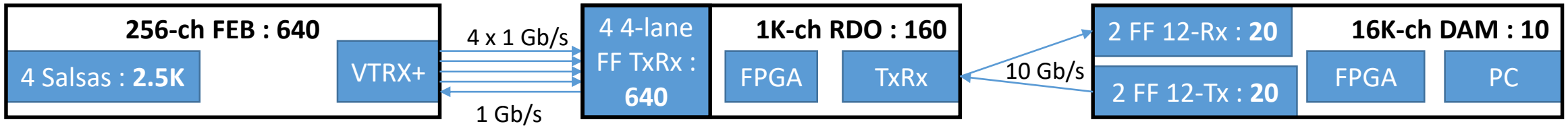


- Option 2 : FEB-DAM based on lpGBT-Vtrx+ interface



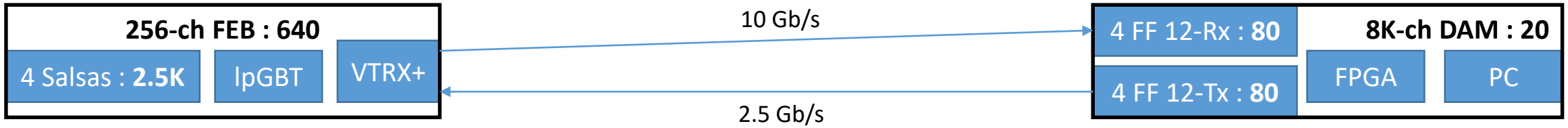
160K-ch MPGD readout configurations and component count

- Option 1 : FEB with direct Salsa-VTRX+ interface



Low density 1 Gb/s grade design

- Option 2 : FEB with direct DAM interface



Mix of low density low speed and high density 10 Gb/s grade design

No RDOs to design, produce, install, debug and maintain

4 times more 12-lane FF pairs
2 times more DAMs

Power

256-channel lpGBT-based FEB for CyMBaL : components

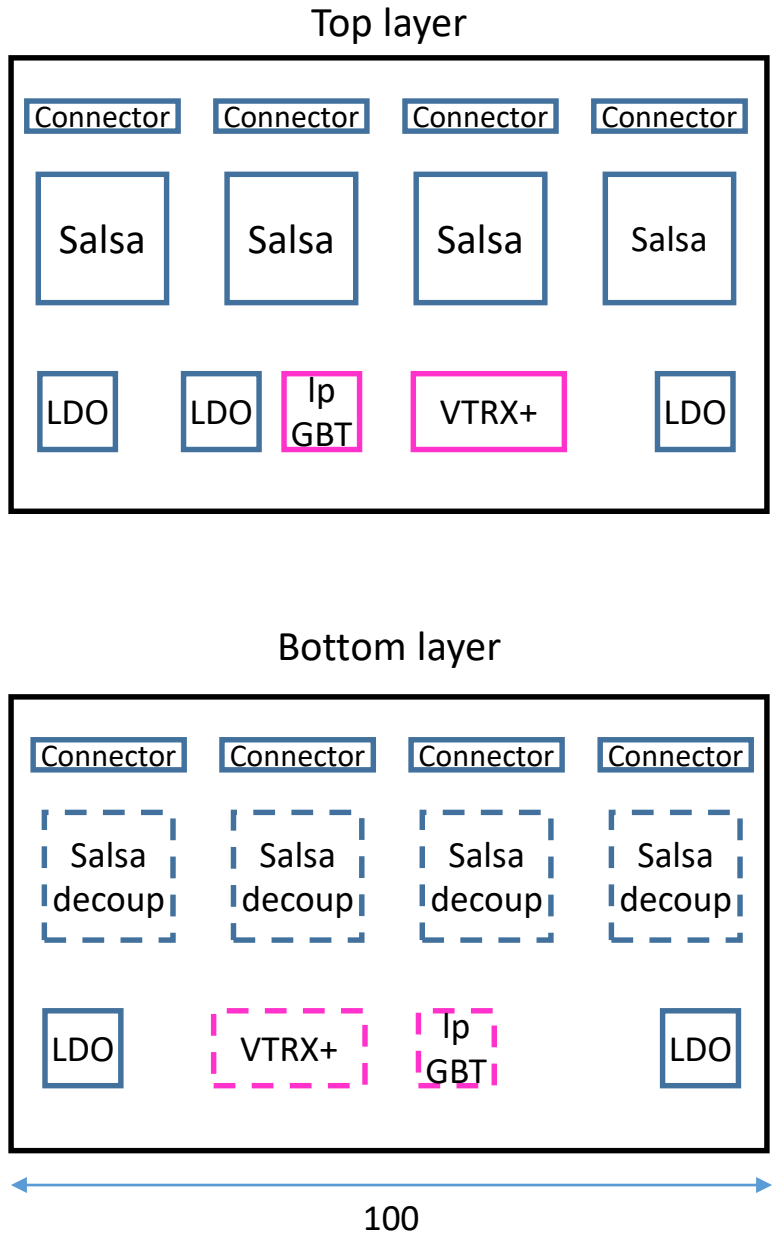
- Assuming 16 x 16 ball 1 mm pitch BGA package for Salsa
- Low profile 40-pin connectors for input signals over micro-coaxial cables
- Active components on both sides of the board

- Length and width give an idea

- Height of the board
  - → Need to accommodate cooling
  - → Need to include mechanical fixture for VTRX+ connector
    - The fragile optical pigtail to be secured within the board

- On-board linear low dropout regulators

- Radiation-hard magnetic field tolerant DC/DC converters
  - → On a companion board
  - → Count on common collaboration efforts
    - Type, surface including air core, height, shielding, cooling



256-channel lpGBT-based FEB : power

- Raw power budget with minimal margin : ~6.8 W
  - → 27 mW / ch
  - → 1.5V – 6.7 W
  - → 2.8V – 0.2W
- Assume 8.5 W for safety : 25% extra
  - → 33 mW / ch
  - → 1.5 V – 5.6 A
  - → 2.8 V – 90 mA
- Where to place DC/DC converters ?

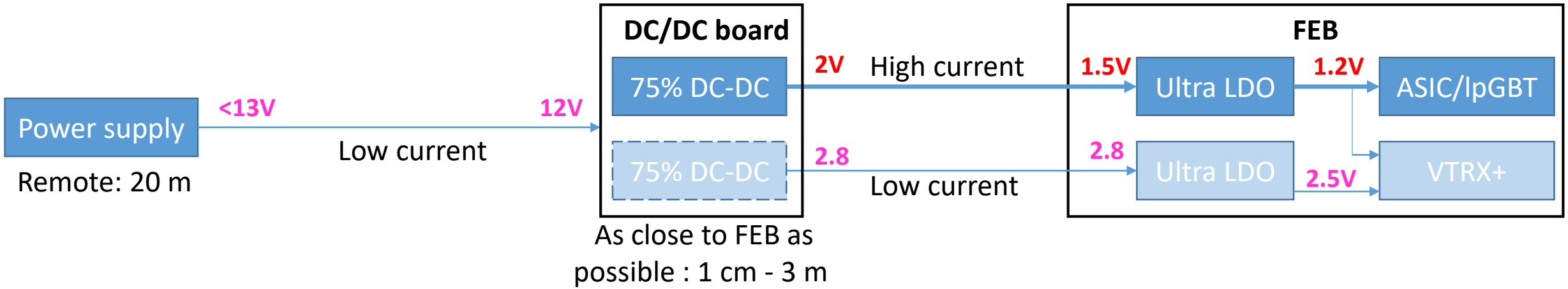
FEB components and their power consumption

Component	Vin V	Current mA	Power mW	Comment
Salsa 1	1.2	1 000	1 200	15 mW/ch
Salsa 2		1 000	1 200	
LDO Salsa 1-2	1.5	2 000	600	Can use 2 LDOs to avoid hotspot
Salsa 3	1.2	1 000	1 200	15 mW/ch
Salsa 4		1 000	1 200	
LDO Salsa 3-4	1.5	2 000	600	Can use 2 LDOs to avoid hotspot
lpGBT	1.2	420	500	Probably 25% overestimated
LDO lpGBT/VTRX+	1.5	440	130	
VTRX+	1.2	20	25	
	2.5	70	175	
LDO VTRX+	2.8	70	20	

FEB power distribution example

Reminder : https://indico.bnl.gov/event/22316/contributions/87363/attachments/52727/90159/240215_IM_MpgdPower.pdf

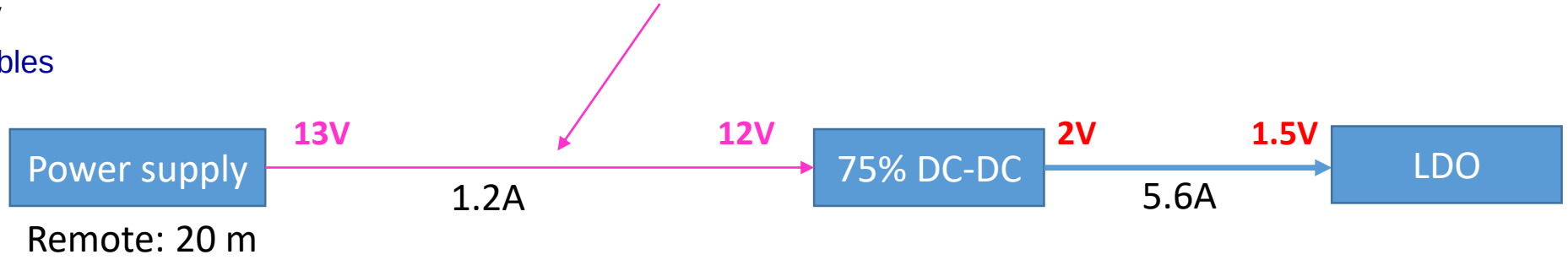
- DC/DC-based LV distribution: to be magnetic field tolerant
  - → Remote power supply distributes 12V with a low voltage drop over ~20 m cables
    - Say less than 1V
  - → Low cross-section power cables
    - The lower the drop the lower the power dissipation in cables but the large is their cross-section



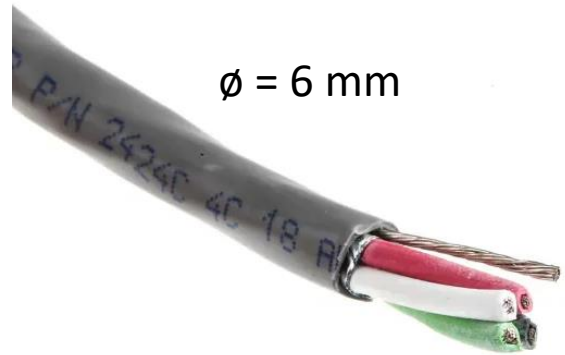
- DC/DC regulators
  - → Might be bulky and a source of EMI
    - Space + extra material for shielding
  - → Distribute high current for 1.2V power
    - Should be close to FEBs
      - Avoid significant power drop and power dissipation in cables
      - Avoid pickup noise and ground-loops

LV cables from power supply to DC/DC regulators

- Assumptions:
  - → Remote LV power supply 20 m away
  - → 1V voltage from between LVPS and DC/DC regulators
    - 13V LVPS output voltage for 12V DC/DC input
  - → 75% DC/DC efficiency
    - 1.2 A over LVPS cables

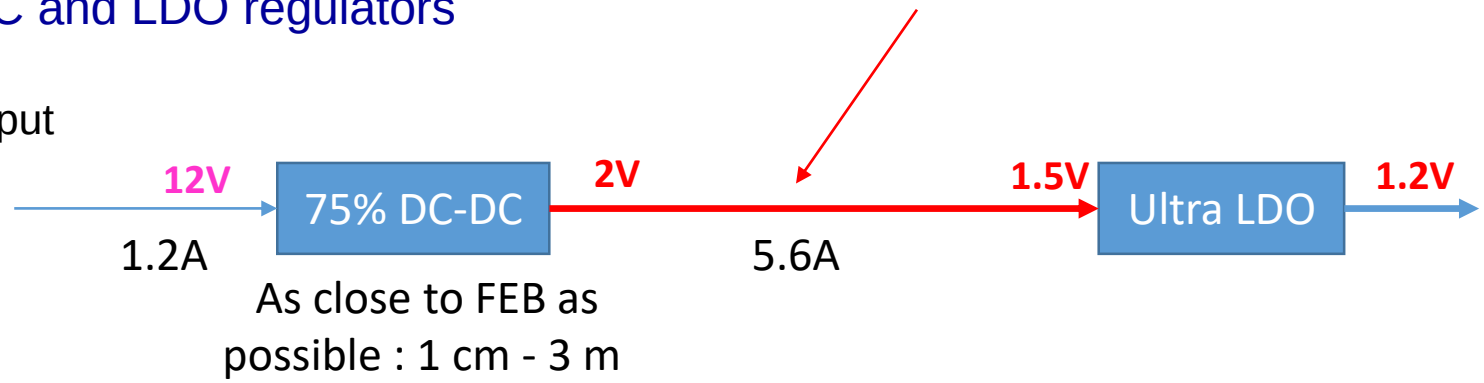


- LVPS power : 15 W / FEB
  - → 60 mW / channel
    - Remember : 15 mW / channel for Salsa !
  - → Power dissipation (loss) over LVPS cables : 1.2 W
- LVPS cables cross-section 0.8 mm^2 or 18 AWG
  - → Cable harness with two power cables and two sense wires
  - → Alpha Wire 2424C : commercial harness including shield and coating : ø = 6 mm
- Reminder : there are 160 CyMBaL FEBs



LV cables from DC/DC regulators to LDO regulators

- Assume 0.5V voltage from between DC/DC and LDO regulators
  - → Reminder : no remote sense regulation
  - → 2V DC/DC output voltage for 1.5V LDO input
  - → 2.8W power dissipation (loss)



Cable cross-section vs DC/DC-LDO distance

DC/DC-LDO Distance	Cross section		Harness + 2.5V cabs
cm	mm^2	AWG	Ø mm
30	0.1	26	4.6
50	0.2	24	5
100	0.4	20	5.4
200	0.8	18	6
300	1.2	16	

Alpha Wire
3464C

6328

2414C

2424C

- Reminder : there are 640 MPGD FEBs with tailored power cable assemblies
- If possible, having DC/DC board next to FEB is preferred

Power components

- Studies within the ePIC collaboration to have common approach / solution to power the frontends
  - → Magnetic field and mild radiation tolerant
  - → Lead by Tim Camarda and Gerard Visser

bPOL12V module prototype with custom coils and shield

© P. Aspell, CERN; S. Caregari, NSU Taiwan

- CERN power components
  - → DC/DC regulators
    - bPOL48
    - bPOL12
  - → Linear LDO regulator
    - from CMS : high power for 1.2V Salsa and lpGBT
    - Linear LDO regulator : low power LinPOL12 for 2.5V VTRX+
  - → ePIC-wide and personal contacts : confirmation of availability in needed quantities
    - MPGD needs
      - 1 500 DC/DC regulators and possibly LinPOL12
      - 3 000 CMS LDO

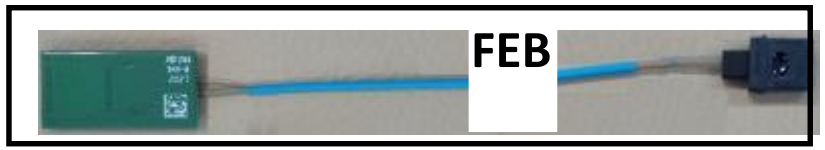
- But do we even need radiation tolerant components, can commercial components be used ?
  - → *e.g.* MIC69303 (RT) linear regulator from Microchip
  - → The PreTDR figures for radiation are extremely low : 0.4 krad after 10 years

- Magnetic field is a real issue
  - → Saclay counts on ePIC-wide developments, final design and validation, on guidance for adaptation to our needs

Frontend partitioning

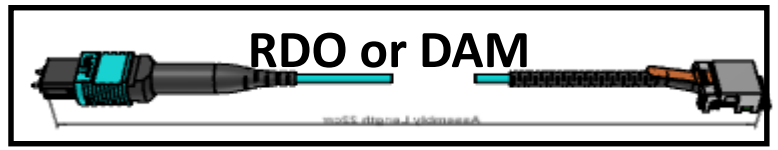
Height : ~10 mm

- Protect fragile VTRX+ and its pigtail by containing it within the FEB



Short pigtail / on board

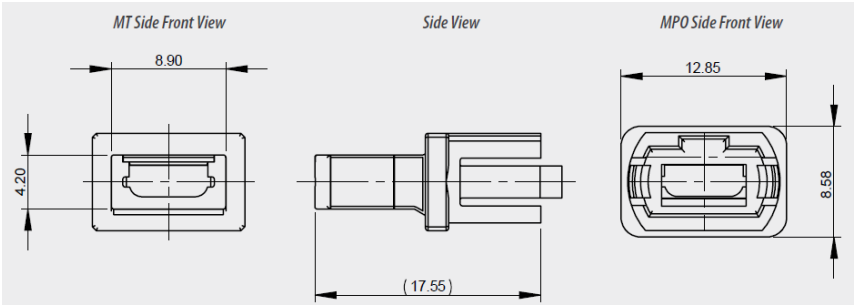
Fibers of adapted length between patch panels



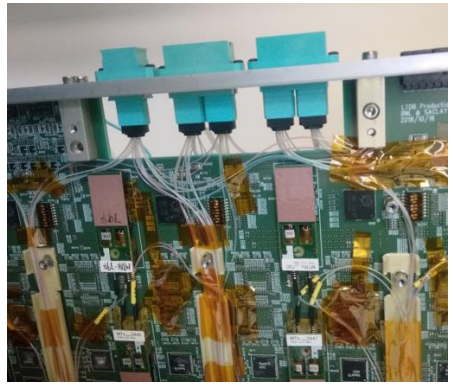
Short pigtail / on board

→ Common practice for commercial FireFly components in industry and VTRX predecessor in HEP community
→ Can limit pigtail length options to very few if not to 1 value : as small as farthest placement from front panel
  - Potential to have a common pool of VTRX+ components for all subsystems
→ Easier maintenance

- MT-MPO low-profile adapter from Senko : 7P5-SM-1
  → 8.6 mm height



VTRX example



FireFly example

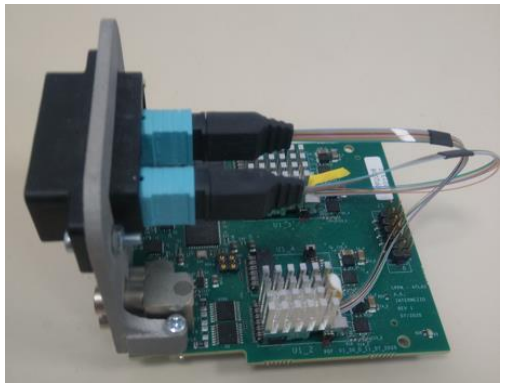
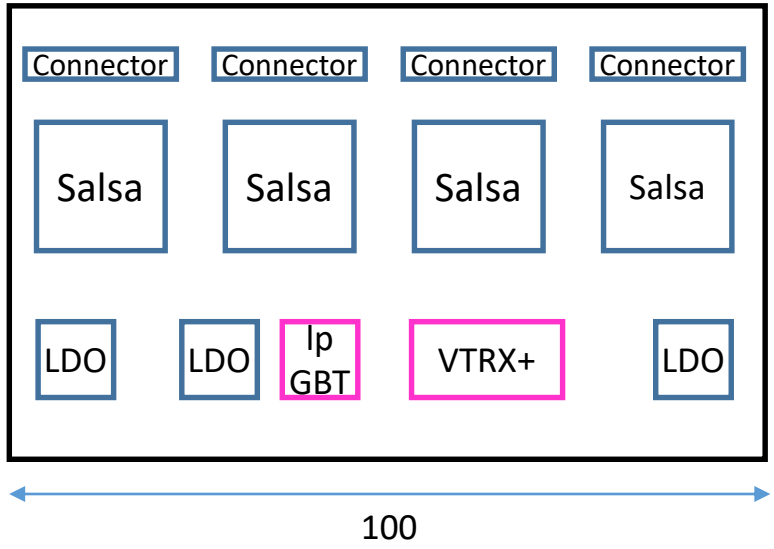


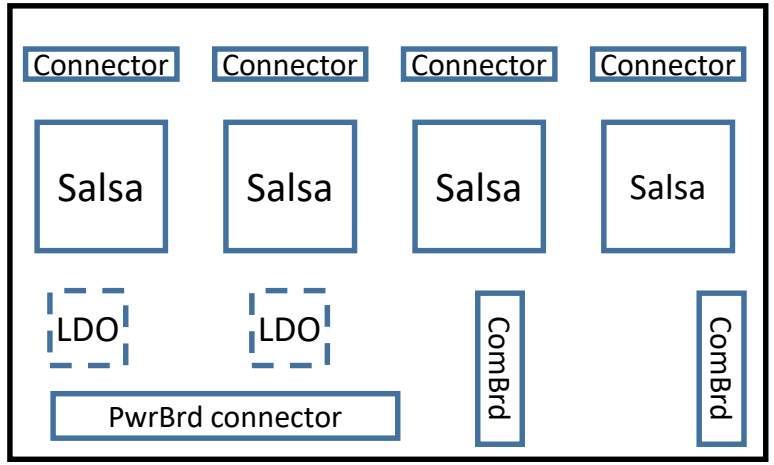
Illustration of CyMBaL lpGBT-based FEB organization options

- Single board

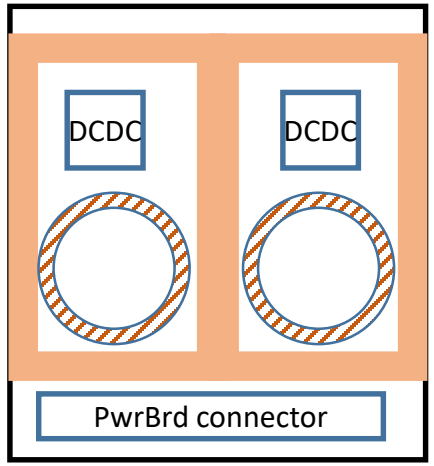


→ Complex high density high speed
→ MPGD-specific form factor

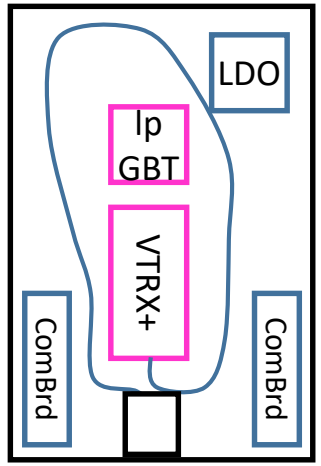
Mezzanine approach



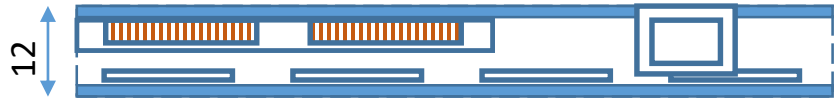
→ FEB mother-board
→ Low density low speed
→ MPGD-specific form factor



→ DC/DC mezzanine
→ 2 T tolerant low EMI
→ Common to all MPGDs ?



→ Communication mezzanine
→ high density high speed
→ Common to all MPGDs ?



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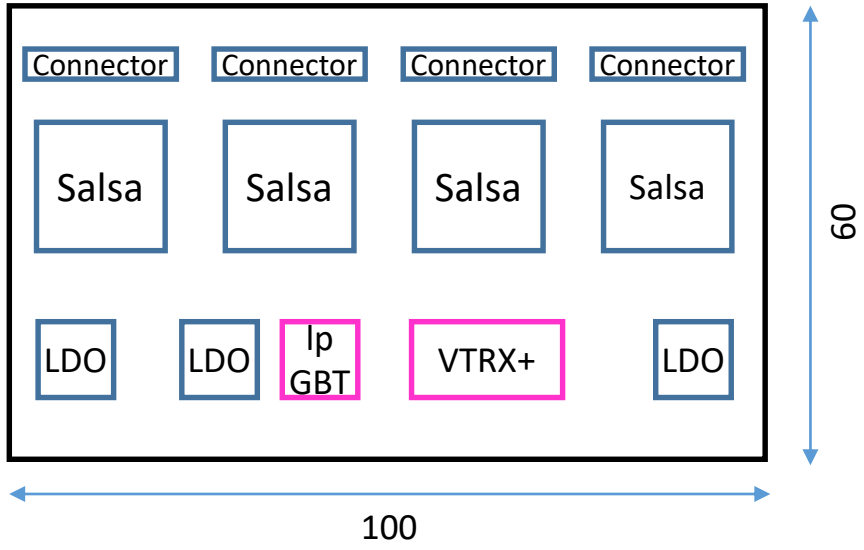
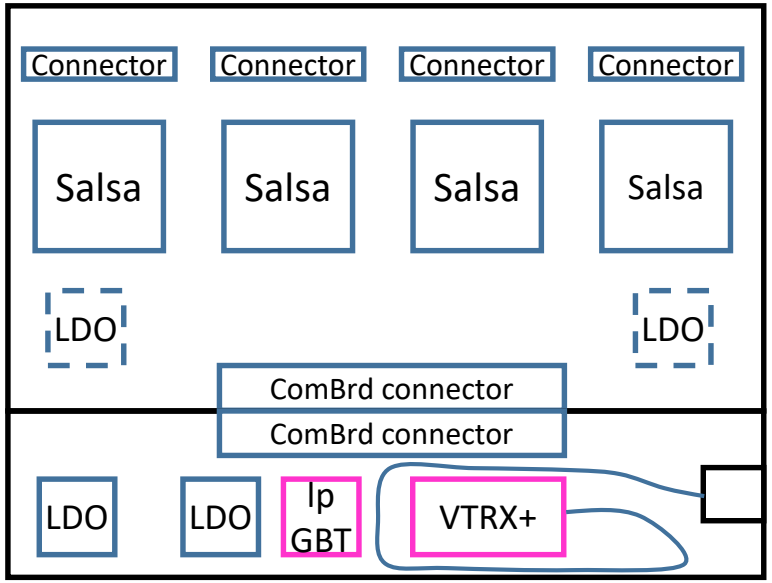


→ Complex high density high speed
→ MPGD-specific form factor

Companion board approach



→ FEB board
→ Low density low speed
→ MPGD-specific form factor

→ Communication board
→ high density high speed
→ Common to all MPGDs ?

→ board-to-board or board-to-cable (flex) connections

- DC/DC board whereabouts to be studied

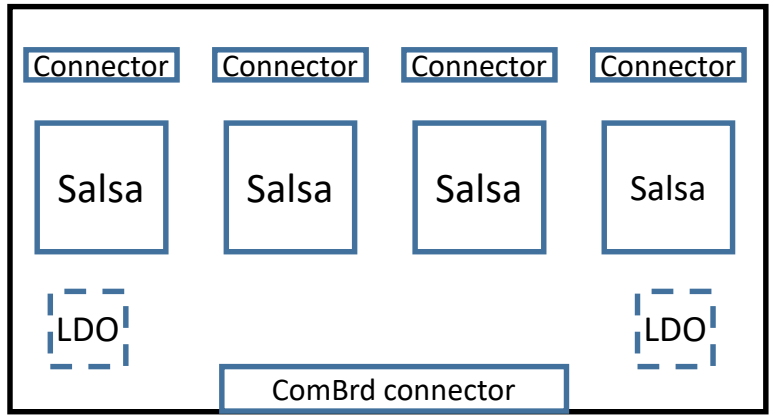
Instead of summary : what could be done as work sharing ?

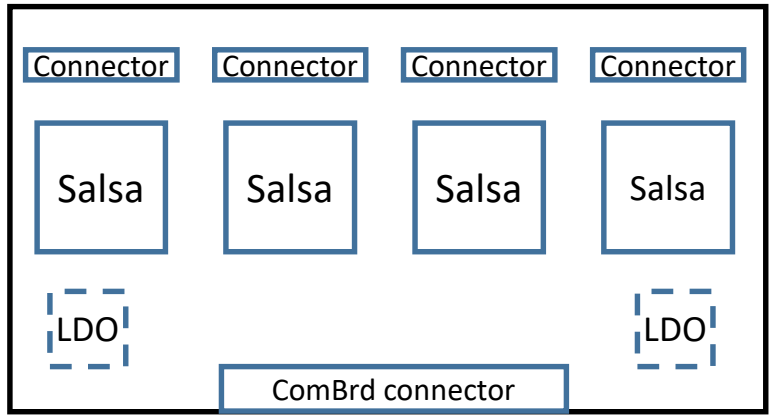
- Readout architecture
  - → Choice to be done : 2-stage lpGBT-based or 3-stage RDO-based
- FEB
  - → Frontend electronics partitioning based on space constraints
  - → FEB and communication board design
    - Saclay has an expertise
- Low voltage powering
  - → Common approach for low power distribution
  - → DC/DC board design
    - Saclay expects support from groups actively involved in powering studies
    - Adaptation for MPGD
- Colling
  - → No particular studies have been conducted at Saclay
- Only frontends have been discussed so far but there is much more
  - → Backend (hardware), firmware and software adaptation
  - → Run control, slow control and monitoring
- Consolidate readout specifications – mostly concerns Salsa
  - → Make sure they suit MPGD requirements
  - → Make sure envisaged calibration and monitoring means are adequate
  - → Timeline…
- Collaboration meeting at Frascati could be a good opportunity to discuss these questions ?

Backup

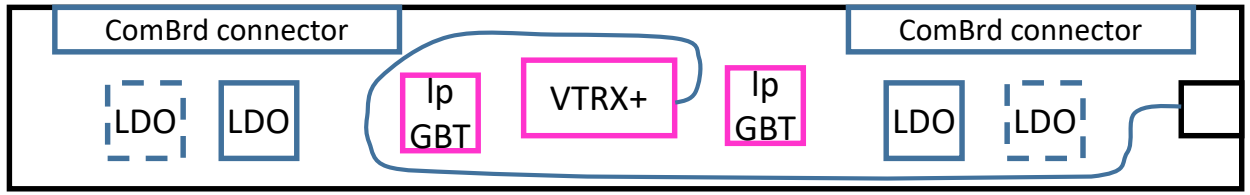
Illustration of CyMBaL lpGBT-based FEB organization options

- Shared communication board approach





→ FEB board
→ Low density low speed
→ MPGD-specific form factor



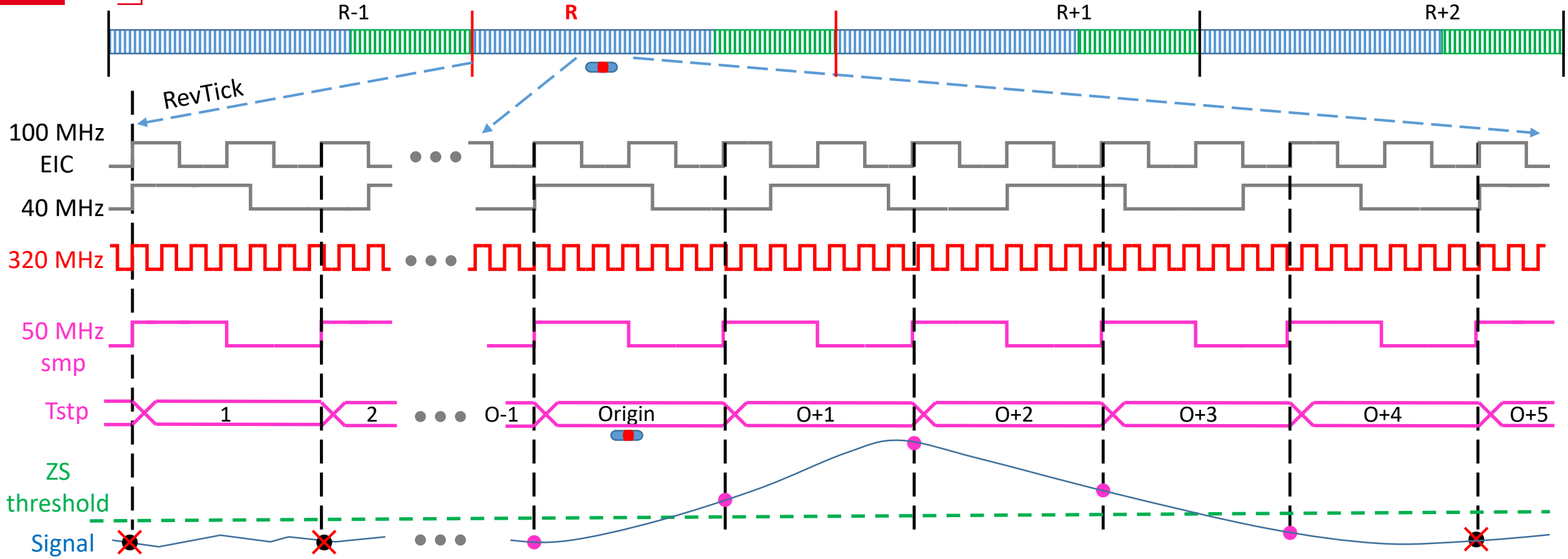
→ Communication board
→ high density high speed
→ Common to all MPGDs ?

→ Short board-to-cable (flex) connections

- Requires less VTRX+ components and fiber optic cables
  - → 2 VTRX+ optical outputs used
  - → Need to understand if detector curvature permits

- DC/DC board whereabouts to be studied

Signal timing with lpGBT



- Periodic “Sync” command generated when EIC and 40 MHz clocks are in phase
  - → RevTick in this example
  - → Allows phase alignment and monitoring of clocks within Salsa
- In this example Salsa is programmed to keep one sample before and after threshold crossing
  - → Salsa data for the signal : FrameCounter, Tstp(O-1) Smp(O-1) Smp(Origin) Smp(O+1) Smp(O+2) Smp(O+3)