eRD109 COTS Waveform Readout FEB – update Dec. 12, 2024

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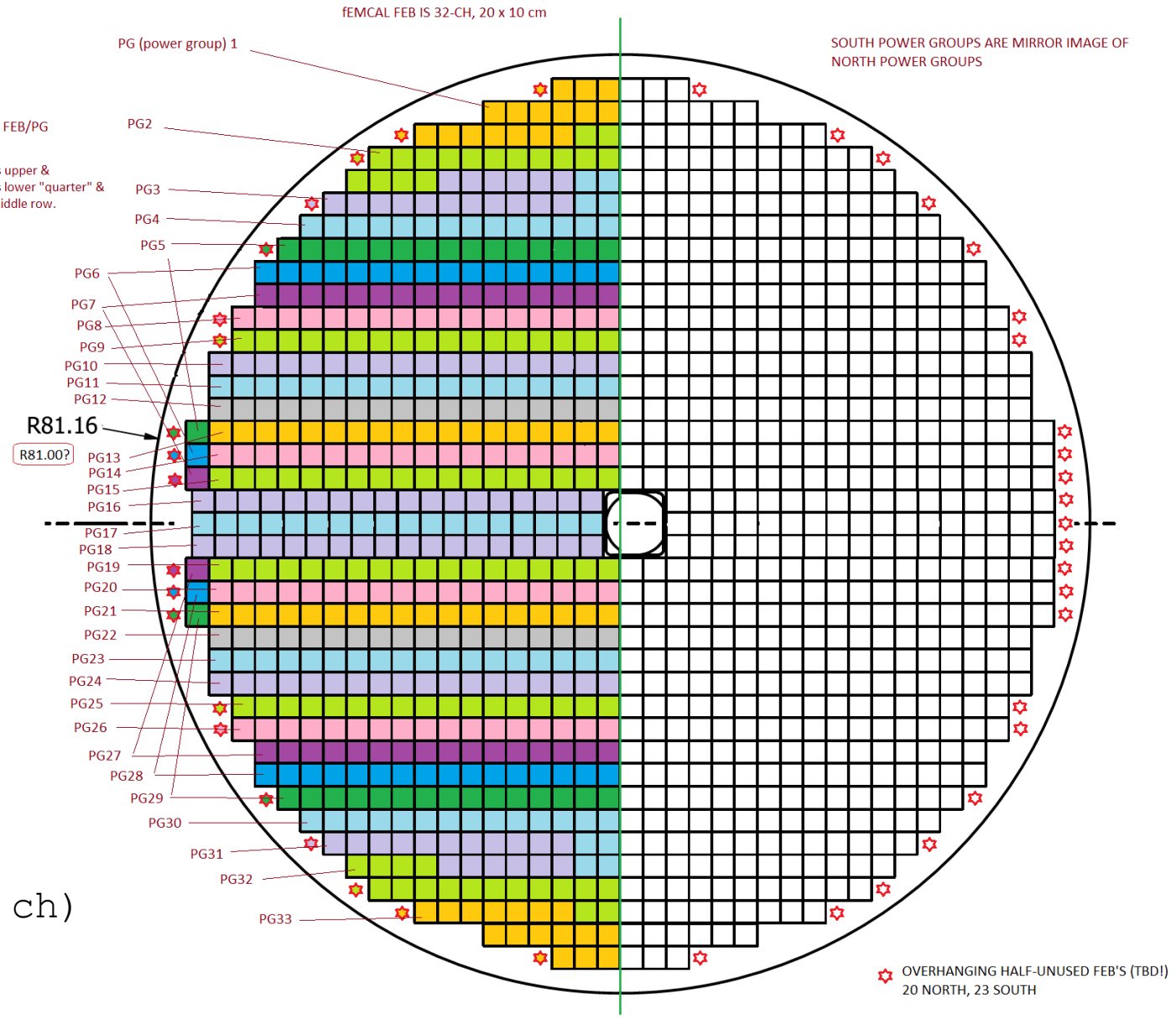


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fwd ECAL:
1145 blocks
594 FEB (18,320 ch
         or maybe 19,008 ch)
38? RDO
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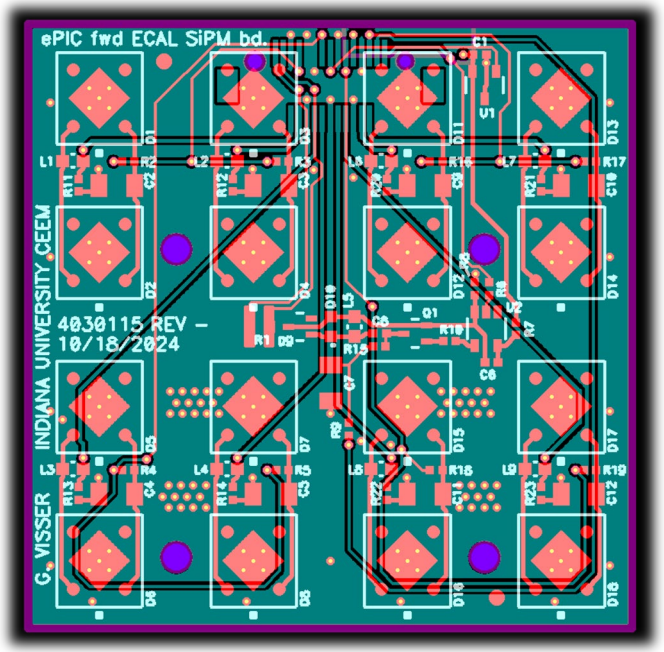
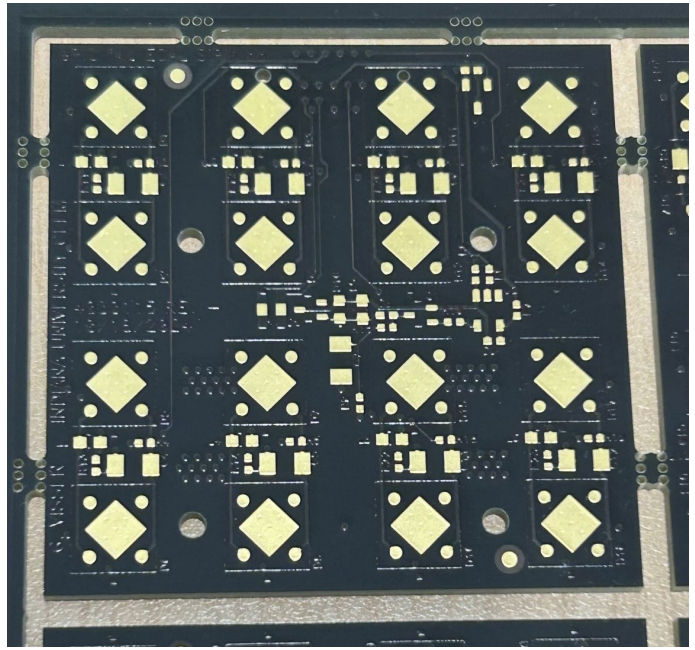
Progress since last report

- Fwd ECAL SiPM board received 11/27 (32 boards, $64.53 ea.)
  - 4-layer 370HR 1.9 mm thick, nonconductive filled/cap-plated vias (needed on FEB anyway, and better for SiPM thermal pads); thermal connectors (rear) for SiPM board to water line (use is to be evaluated)
  - Shipped to UCLA for assembly, should have first about mid-January
  - SiPM PCB production quote $13.85 @ 5,000
- Continued work on the schematic and PCB layout for fwd ECAL FEB (see next slide)
- Integration discussions with project mechanical engineers (11/15, 11/18, 12/5)
  - Absolutely vital discussions, and real help now with CAD models ☺
  - Complete correction of our thinking on light-tight cover, cable exit paths, and space available at perimeter of the detector…
  - …But confirmation from them that the blocks, lightguides, SiPM and FEB and cables as we have planned do fit within the integration envelope on detector ☺
  - Joshua Harvey (BNL) working on cooling tube details, will be some changes to FEB layout in finalizing this
  - Need for half-FEB's due to odd number of blocks in a half-row is still TBD (prefer to avoid of course)
- Bwd ECAL: Larry Isenhower has built a few prototypes (OSHpark) of the proposed preamp board. Same preamp as fwd ECAL FEB.
  - To be tested next week, then bwd ECAL group requests Jlab to order 26 assembled (as we were going to to do before), for the re-try of DESY beam test in February. (To use with CAEN V1725S, 14 bit, 250 MS/s.)



Fwd ECAL SiPM board (4 channels)



dark red silkscreen – not a bright idea

Continued work on the schematic and PCB layout for fwd ECAL FEB

- Small mechanical change (detector block spacing)
- Exploring changes in thermal contact area
- ADC's and close support components now fully routed, fits basically as planned/hoped
- Routing input signals and routing signals from analog channels to ADC's
    - Need to rip up and analog channel and space it a bit more to get that to fit; a few days
- Yet to do on FEB: bias, FPGA, power supplies

2 channel analog prototype (to use with the Polarfire evaluation board)

- Same layout (except for power planes); now clear that it can be exactly same. Will be copied out from FEB layout soon.
- Interfaces to one SiPM board. Will be tested with detector block and cosmics
- Also to serve a test article for radiation tests on opamps & ADC, with test I/O to isolate components for test
- Goal is to order that ~~before end of year~~ mid-January

Full FEB
- 10 layers (6 planes)
- nonconductive filled / cap-plated vias

2-channel prototype
- 6 layer (2-3 planes)
- OSHpark standard stackup
- open vias
- large "via" for QFN thermal pad
- hand-solderable prototype

Fwd ECAL FEB (8 channel portion, corresponding to 2-ch prototype PCB)