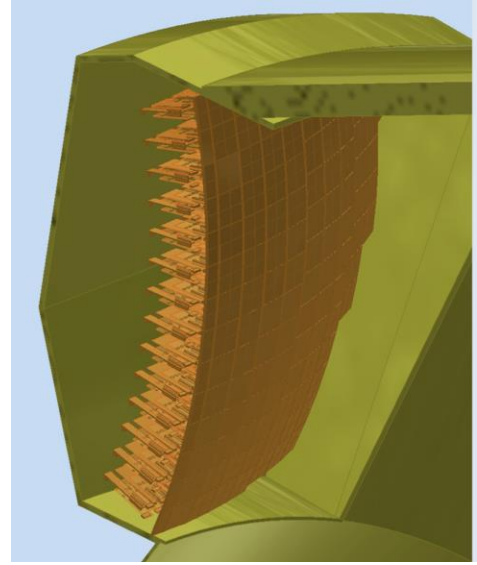

Status of dRICH RDO

INFN Bologna team
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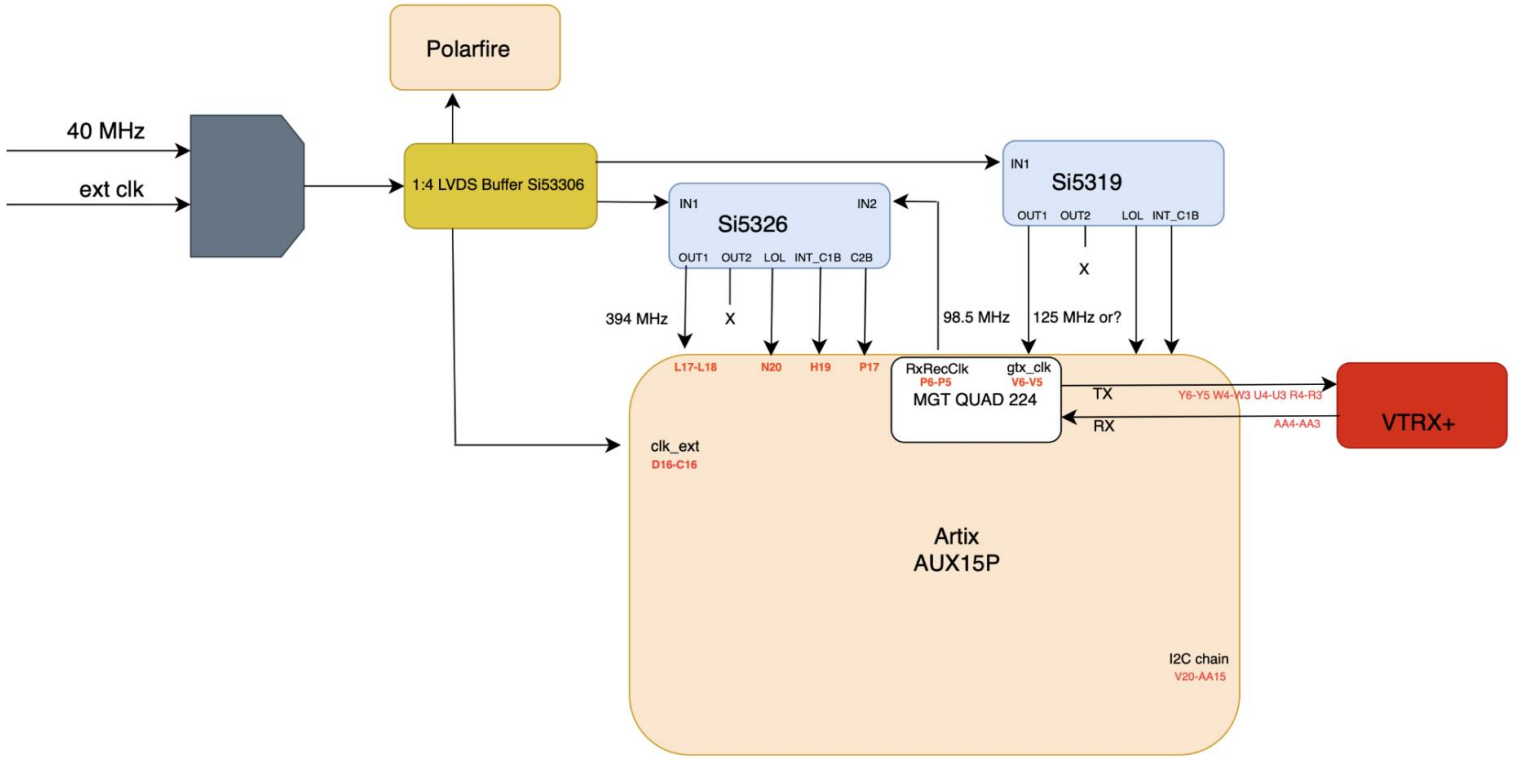
December 13rd, 2024

Since last update:

- work on SiLab SkyWorks (minor last minute change): we will use two SkyWorks ASIC
- discussed **at length** the VTRx pigtail **length → 1620 VTRx 20 cm** see presentation made at dRICH meeting 4 December
- development of firmware on AUX15P
  - implementation of IPBUS ("initial link connection") [migration from KC705]
  - implementation of ALCOR readout (on-going) [migration from KC705]
  - use of ALINX AUX15P for irradiation test (on AUX15P itself and to control SiLab chips).
- preparation of Trento **irradiation tests** (starting… today)

Clock scheme: including clock for VTRX+ serdes

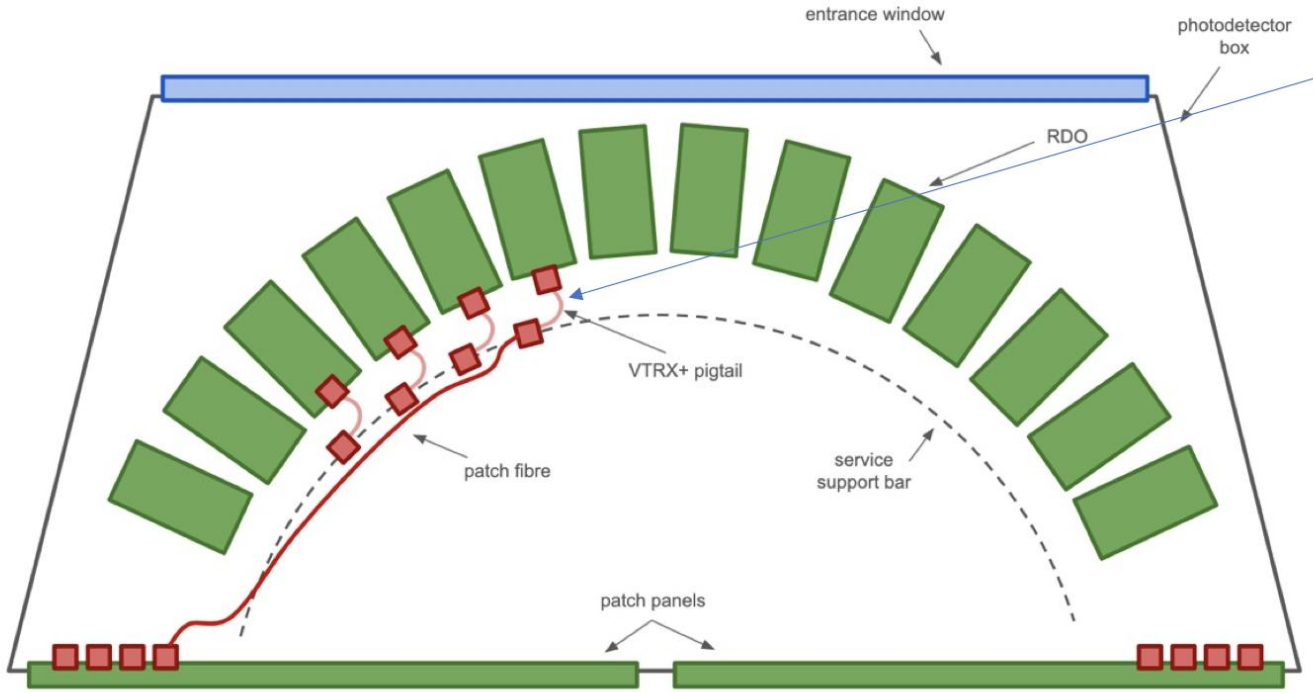


The additional Si5319 will allow us to keep flexible the frequency to be used by the VTRx+ serdes

RDO, VTRX+ and detector box: our baseline

For more details full presentation (Roberto) here

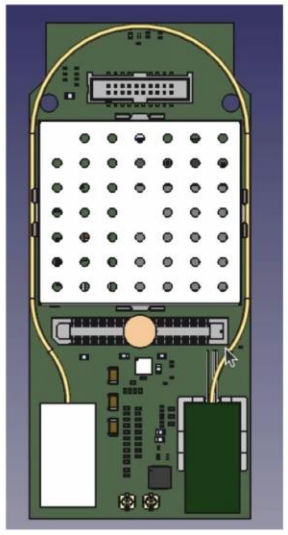
pigtail lengths



PROS: decision now "works"
CONS: leaves pigtail **"dangling"** →fragile?

- We use a support bar, additional patch cords have different lengths we will work out exact lengths later: the detector box can be opened
- Many details need to be still worked out: for many engineering design aspects we are not yet there in PDU/detector box design. We are in "hurry" here due to the need of defining now pigtail length (due to CERN schedule...)

Can we avoid dangling fiber/pigtail...?



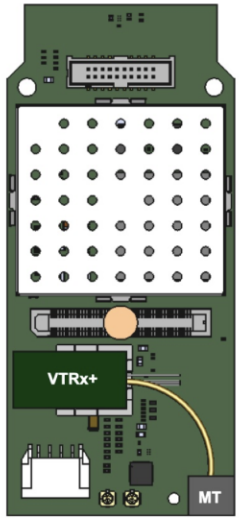
Option A:

it is 20 cm length
Requires modification of RDO pre-placement

- 20 cm is compatibile with our baseline option, so we seelct the baseline option now and we leave open this scenario

- the fiber all aorund the RDO is not very practical
- we might have **light emitted** everywhere
- fiber close to the hottest part of the RDO (during annealing) might not be good idea! → onnectiion could be inside emi-screen but **bending might be critical** (and length would be 15 cm or 25 cm depending on # of rollings)

Can we avoid dangling fiber/pigtail...?



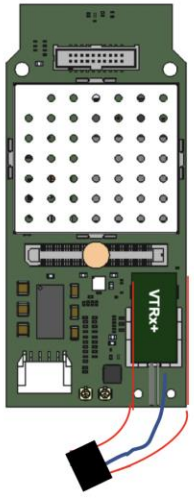
Option B:

it is 5.5 cm length
Requires modification of RDO pre-placement

- This is apparently robust but...

- we have seen **mechanical stretch on fiber is high**
- we need to add MT-MT (female) for mounting on PCB so we need one 1 cm more that we don't have.... (in the detector box) → **killer objection**

Can we avoid dangling fiber/pigtail...?



Option C:

it is 5.5 cm length Make some 3D–printed mini-box containing the fiber, the MT-MT female adapter, connected mechanically to the RDO

- This gives robustness and protection to the short pigtail
- It doesn't require modification of RDO pre-placement

- it is a "solution" we don't really have now
- we will need to produce different shapes depending on the RDO position in the detector box
- this "rigid" addendum must fit inside detector box and can make maintenance operations difficult
- **we might need strong bending in some** RDO

Summary

Going shorter and avoid dangling?
We considered several options but for each of them the number of cons largely exceeds the pros. And if too short we can't come back. We don't have any convincing option for such scheme.

How to proceed? We go baseline
We select a 20 cm dangling pigtail
Design needs to be carefully followed up to setup proper access, secure maintenance etc. (but this is valid for almost what we are doing ;-)

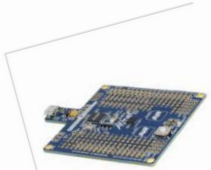
dRICH option: 1500 VTRX+ with total length 20 cm

We suggested to Fernando: 1620 VTRX+
(mitigation production risk: from 20% to 30%)

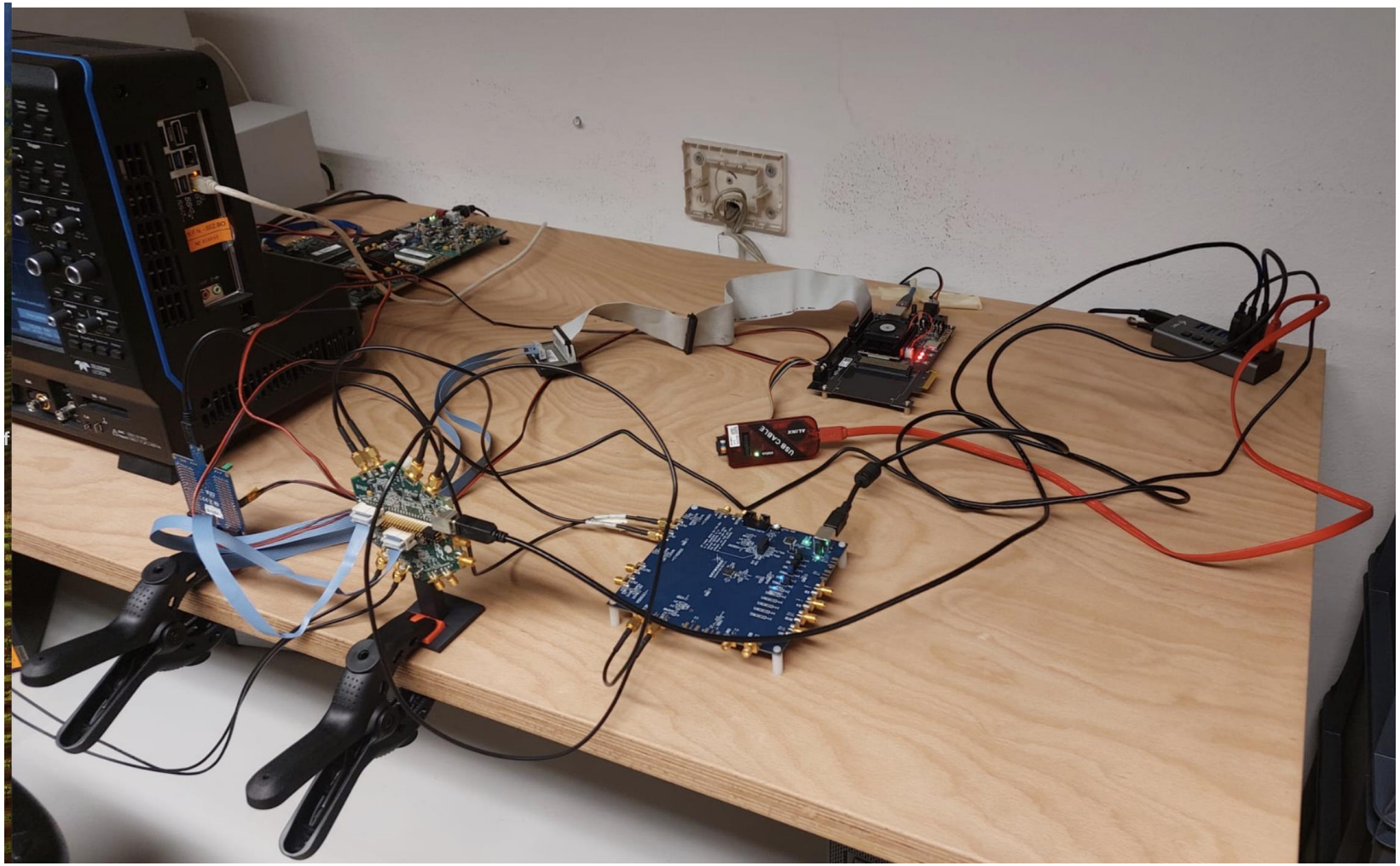
Shown in October
Test 13-14 December!

Irradiation tests

- realistically dRICH RDO will be available January 2025
- scheduled irradiation session at Trento next 12-14 December
- plan to test following components irradiating evaluation boards available on the market
  1. LDO: LTM4709
  2. ATtiny417: https://www.microchip.com/en-us/development-tool/attiny817-xmini
  3. Si5326: https://www.mouser.it/datasheet/2/472/Si5325-2507576.pdf
  4. Xilinx AXAU15 via evb from ALINX https://www.en.alinx.com/Product/FPGA-Development-Boards/Artix-UltraScale-plus/AXAU15.htm



DUT	Test/what we want to learn
LTM4709	SEL, output voltages stability under irradiation, TID test
ATtiny417	SEL, TID, check programming
Si5326	SEL, SEU (in programmed registers), clock stability under irradiation, TID test
AUX15	check existing literature on SEU (conf. bits + SEU in RAM + SEU in flip-flops)



Real updates
next time!

Setup in the lab as of yesterday, now going to Trento!
100 krad target for ATTiny and SiLab 5326
Si5326 fed with 40 MHz and 98.5 MHz clock, output 394 MHz will be monitored + (LOL and SEU)
ALINX: monitoring BRAM (3.5 Mbit) , CRAM (via SEM module) and FlipFlop

Milestones check

- Design and realisation of a specific ePIC RDO card prototype, housing a FPGA, LDO, optical transceiver and I/O and LV power connections to provide the read-out to four ALCOR v3 ASIC. A high degree of integration is foreseen between the RDO card and the 4 FEBs that will house each an ALCOR64 v3 chip.

Milestone scheduled for October 2024.

Order placed by November. Eagerly waiting for RDO (Jan 2025?)

We use ALINX AUX15P as main platform in the meantime. Gained experience on programming SkyWorks chip for example and progressing on firmware already (part of eRD109 for 2025)