



FCFD design status and specifications for AC-LGAD strip sensors for barrel TOF

Artur Apresyan, Tom Zimmerman EPIC Electronics & DAQ WG meeting : eRD109 Monthly Progress Reports Dec 12, 2024

- Work is progressing well
 - The front-end redesign is complete, implemented a dual-stage amp
- Performance evaluated with simulated LGAD signals
 - Use 1000 LGAD pulses generated with Wakefiled2 program and signals re-scaled to amplitude so that the MPV is ~20 fC
 - For simulation of one FCFDv1.1 channel, we used the AC-LGAD sensor RC-network model we presented last time
 - One of the 10 strips in the model is connected to the ASIC channel input.

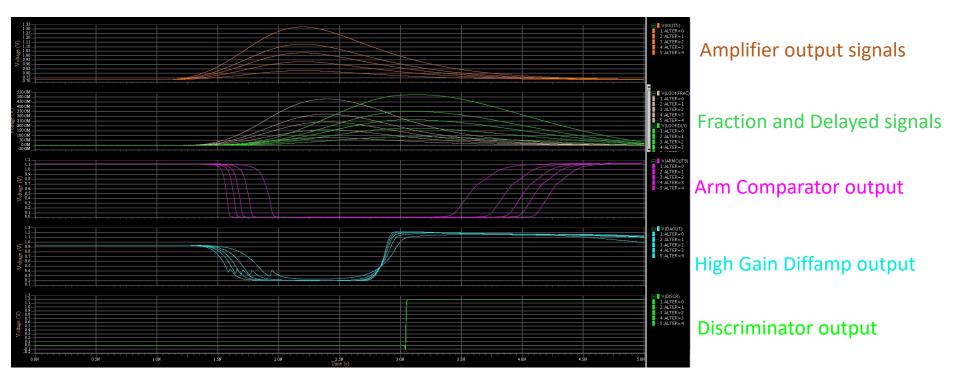


Simulatio results

- Two power settings tried:
 - In high power mode:
 - Using a "noiseless" simulation of 1000 runs with the 1000 LGAD pulses gives 28.6 ps jitter (expected, this is inherent signal jitter).
 - Using a "perfect" LGAD pulse of 20 fC and doing transient noise runs on the circuit gives a circuit jitter of 15.7 pS.
 - Doing transient noise runs with the 1000 LGAD pulses gives a final jitter of 31.9 pS, which is basically the LGAD inherent noise and the circuit noise summed in quadrature
 - In low power mode:
 - Transient noise runs with the 1000 LGAD pulses gives a final jitter of 34.6 pS



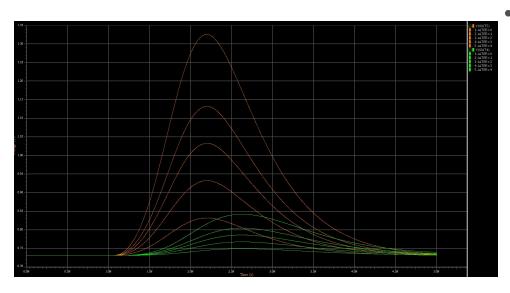
- The simulation is shown for a range of input charges of 15, 30, 45, 60, and 90 fC
 - Discriminator output shows that it moves only a few pS over this range of signals



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- Currently working on updates to the arming comparator and readout
 - Configurable threshold to trigger the comparator
 - If the signal is above ~7-10 fC \rightarrow trigger readout of that strip, and the neighbor on each side (the threshold is configurable)



- Stage-1 output along with the output of the neighbor channel.
 - Note that the neighbor channel signal is smeared (delayed) somewhat due to the RC components in the AC-LGAD
 - The neighbor amplitude is ~20% of the main channel.



Next steps

- Currently finalizing the design, expect to start the layout in the next few weeks, with submission in either Jan or Feb TSMC run
- Working on reserving the mini@sic run with TSMC
- No test beams in FNAL in FY25
 - We are working on several options to quickly perform characterization of the chip asap
 - Initial characterization with charge-injection and beta-source and laser will be performed once received from foundry
 - Reserved a slot in DESY test beam in July 2024, trying to book a slot in SLAC

