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Status report of the eRD109 project on SALSA chip development

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EPIC DAQ/electronics WG meeting

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SALSA CHIP TARGET SPECIFICATIONS

Versatile front-end characteristics

- Dedicated to MPGD detectors and beyond
- 64 channels
- Large input capacitance range, optimized for 50-200 pF, reasonable gain up to 1nF
- Large range of peaking times: 50-500 ns
- Large choice of gain ranges: 0-50, 0-250, 0-500 fC or 0-5 pC
- Large range of input rates, up to 100 kHz/ch with fast CSA reset (limit assumed for EPIC: 25 kHz/ch)
- Reversible polarity
- Front-end elements can be by-passed

Digital stage

- Fast sampling ADC for each channel on 12 bits (> 10 effective bits) at up to 50 MS/s
- Possibility under study to double rates by coupling pairs of channels
- Integrated DSP for internal data processing and size reduction, treatment processes to be selected according to user needs
- Continuous readout compatible with streaming DAQ foreseen at EIC, triggered mode also available
- Several 1 Gb/s output data links

General characteristics

- ~1 cm² die size, implemented on TSMC 65nm technology
- Low power consumption ~ 15 mW/channel at 1.2V
- Radiation hardened (SEU, TID)

LAST UPDATES ON SALSA PROTOTYPES

PRISME TID radiation tests (PLL test chip)

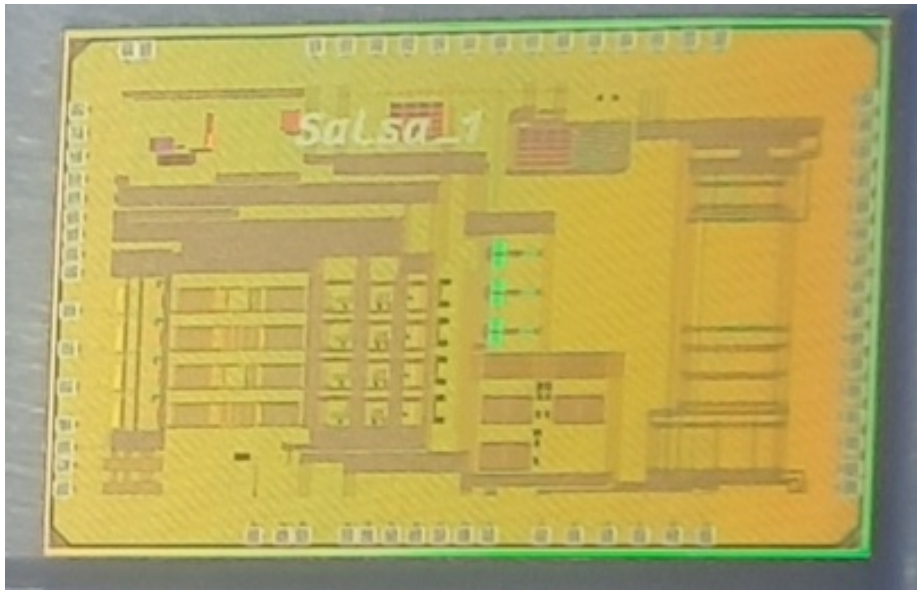
- Tests done mid-November on OBELIX high flux X-ray generator at CERN
- 2 cards tested, both reached 300Mrad irradiation
- Bandgap, analog voltage probes, temperature and radiation probes, high speed links, etc... tested ok up to 300Mrad
- Below 160Mrad PLL worked nominally at 3.2GHz internal frequency with a wide locking frequency range meeting 100MHz input clock specification
- Above 160Mrad locking range performance was degrading
- Cause of degradation understood and workaround elaborated
- Further studies considered, in particular with higher temperature
- NB: expected TID radiation level for EPIC MPGD readout below 100krad

Next steps on PRISME

- SEU radiation tests on I2C part foreseen at Sao Paulo in 2025
- Several updates done on PLL and chip design
  - improvement of deterministic jitter
  - compatibility with lpGBT input frequency
  - inclusion of CDR inside the IP for clock and data recovery from unified input serial port embedding clock, fast commands and slow-control input
  - improvements on radiation hardness
- Submission of PRISMEv1 prototype based on new design December 11th

LAST UPDATES ON SALSA PROTOTYPES

- **SALSA1 prototypes** (front-end + ADC chip)
  - Naked dies received beginning of October
  - Packaging done, encapsulated chips received at Saclay
  - PCB production of test-boards done
  - Cabling ongoing, boards should be delivered this week
  - Tests to be started as soon as boards are delivered, 1st results expected in January



LAST UPDATES ON SALSA PROTOTYPES

- **SALSA2** (fully featured prototype with up to 32 channels)
  - Main DSP modules and associated algorithms mostly defined, study still ongoing for peak finding and feature extraction algorithms
  - Design adaptation to lpGBT included in specifications
  - Work ongoing on HDL code of DSP modules, progresses done on pedestal equalization, common mode correction, baseline following algorithm, digital filtering, serial input and output links
  - New PLL version including CDR produced and integrated, will be checked with PRISMEv1
  - Refinements on architecture and interfaces between digital blocks ongoing
  - UVM environment under definition for high level verifications
  - Still considerable development work ahead

  - New staff engineer at Saclay on the project, + hiring of a new one ongoing
  - Also search for post-doc or temporary contracts
  - New students and post-doc at Sao Paulo

PROJECT MILESTONES AND NEXT STEPS

eRD109 FY23 project milestones

- Specifications of SALSA1 design → done
- Production of SALSA1 prototypes → done, packaged chips delivered to Saclay
- Test card production → almost done
- Performance evaluation → expected end of 2024 / beginning of 2025

Milestones of generic R&D program for EIC project (new 65nm PLL block)

- PRISME prototype submission → done July 19th 2023
- Packaging and test card production → done February 2024
- Radiation tests → done November 2024

eRD109 FY24 project milestones

- SALSA2 specifications → July 2024, details in progress
- SALSA2 submission → March 2025 originally, certainly later
- Beginning of SALSA2 tests → September 2025 originally, certainly later

Very next steps

- Beginning of SALSA1 tests → December 2024
- Radiation tests on PRISME prototypes → SEU tests on I2C in 2025
- Submission of new PRISMEv1 chip → December 2024
- SALSA2 HDL code → in progress