CALOROC status

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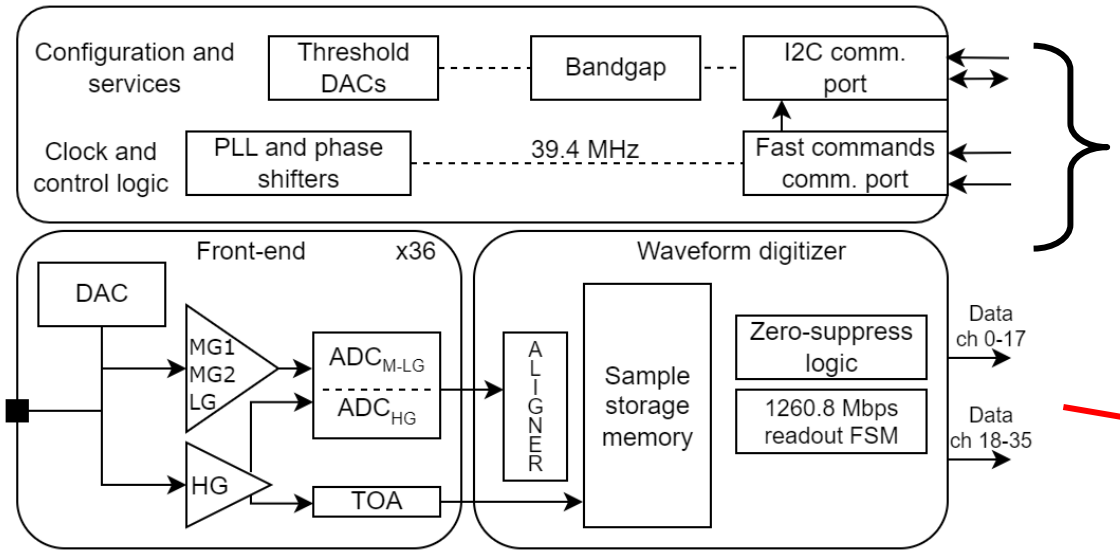
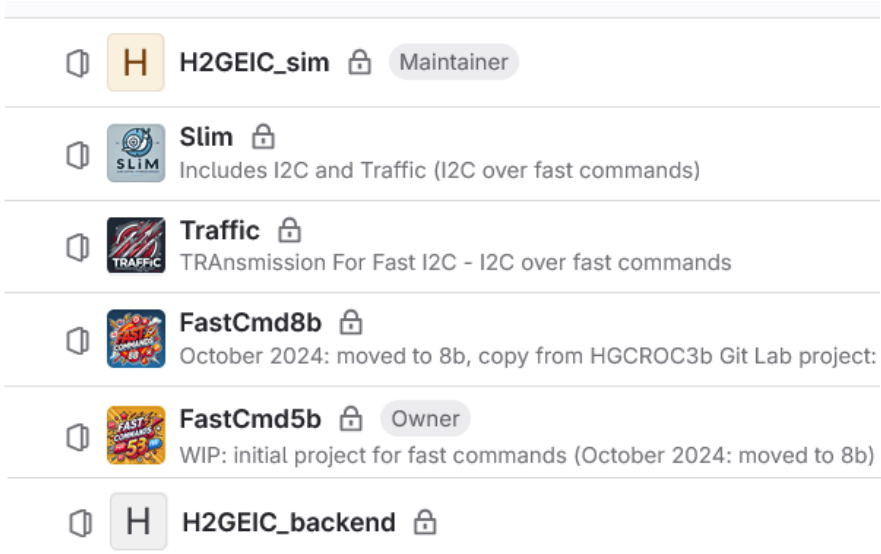
CALOROC development status - backend

- CALOROC project and submodules are available in GIT





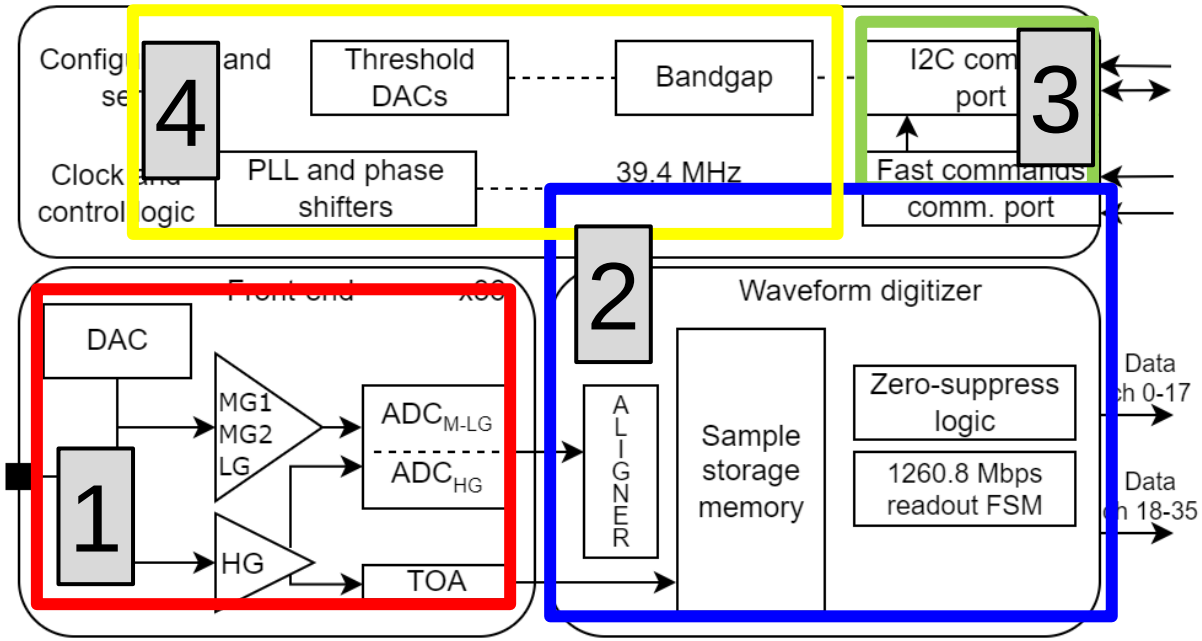
- Fast command (lpgbt compatible) added to project: Done
- Almost fully-assembled RTL verification: Done
- RTL (Verilog code) to schematic scripts finished : Done
- 3x “mini” design reviews: Done

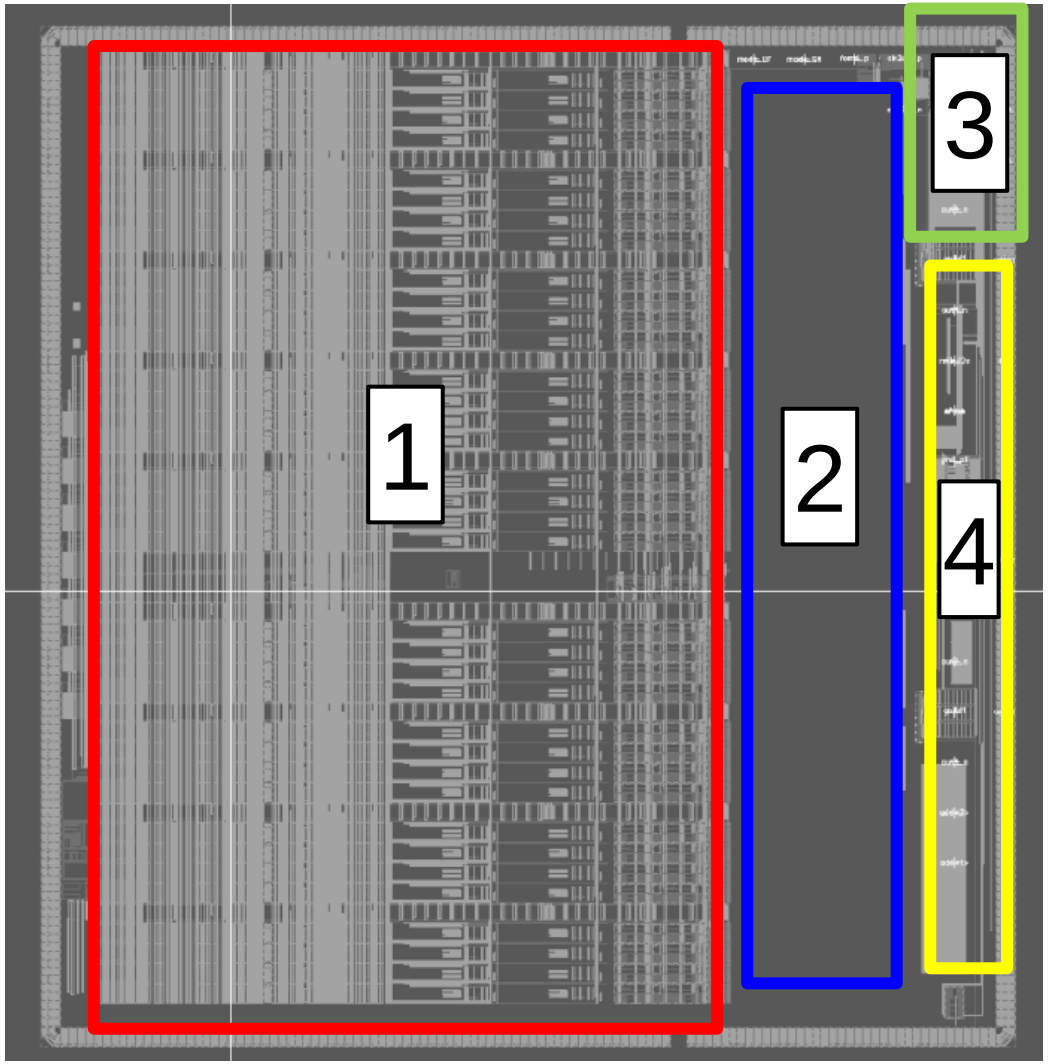
Analog layout finished
Digital layout in progress

- Waveform digitizer layout: WIP
- Analog + Digital assembly: Waiting digital part
- Radiation SEE injection: WIP (done for I2C and fast commands)

CALOROC development status – layout view

- Digital processing under layout (part 2) – only part missing
- SEE injection on part 4 (fast commands, I2C) in progress
- Others: finished waiting part 2 for final assembly





Fast commands for EIC

- Fast commands main characteristics:
  - 8 bits long (fast command “rate” of 39.4 MHz = internal clock of the ASIC)
  - Main and only clock needed from the outside: 315.2 MHz
  - Some new fast commands… to test I2C over fast commands (CALOROCB only)

Fast commands	Value	Description	Comment	Possible back to back
Idle	00110110	Default command inside	~99% of the time	Y
L1A	01001011	External trigger (all channels)	Calibration	Y
ChipSync	11010010	Reset FSM, buffers and counters		
BCR	00011101	Reset timestamp counter to a default value		
EBR	11010001	Empty readout buffers		
LinkResetROCD	10011010	Transmission of synchronization patterns	~ 400x same pattern	
ROC-Serializer-Reset	10011100	Reset serializer link module only		
CalPulseInt	00101101	800 ns internal calibration pulse		
CalPulseExt	01111000	100 ns external calibration pulse		
SC_0	01011010	Send bit 0 for SLIM	I2C over fast commands	Y
SC_1	01011100	Send bit 1 for SLIM	I2C over fast commands	Y
SC_Valid_Reset	10001011	Send validation to SLIM or a reset transaction (2 consecutives)	I2C over fast commands	Y

Summary

- Standardized fast commands CALOROC A/B
  - Will be also used for the future EICROC2)

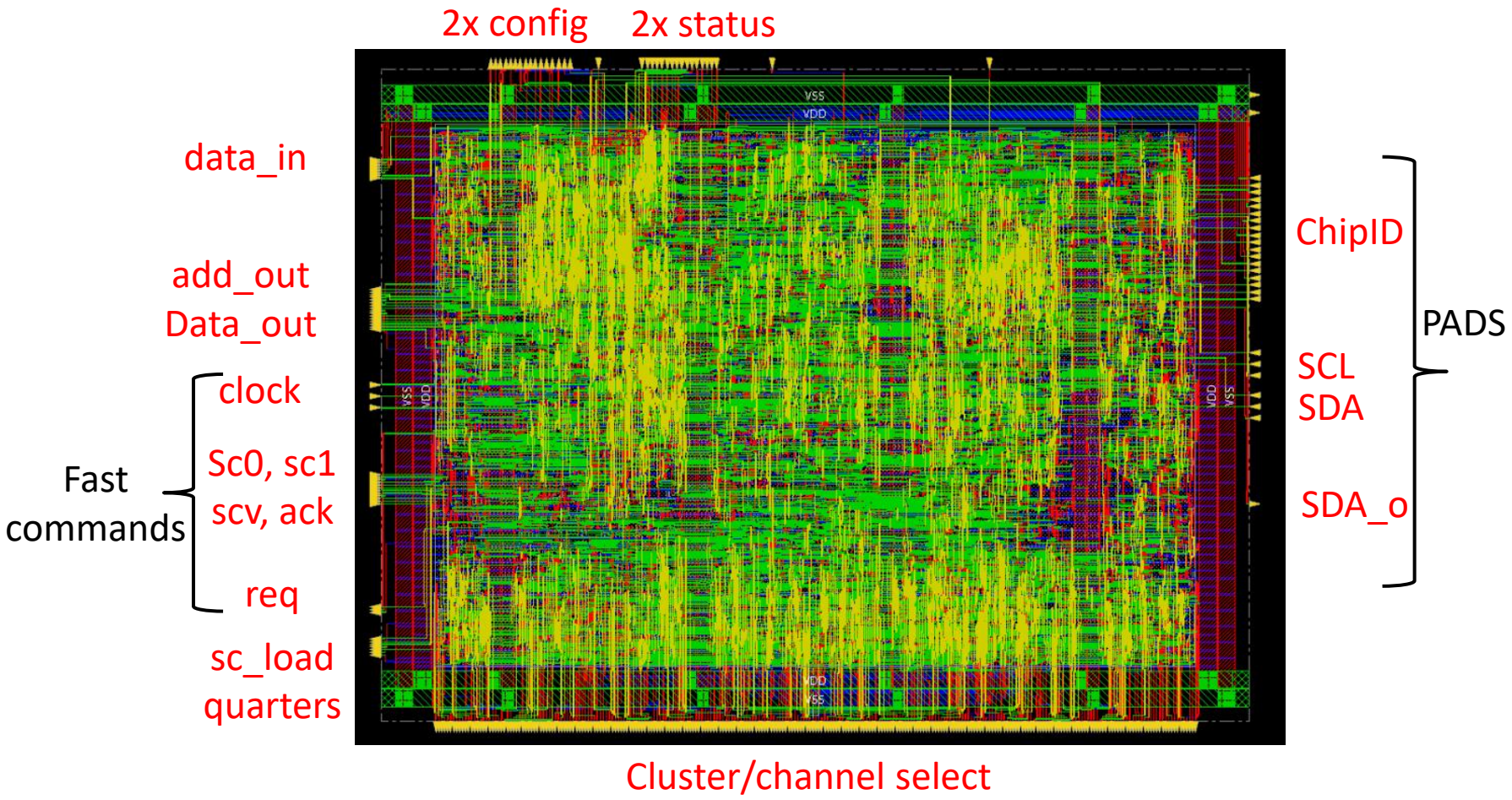
- Digital part layout is in progress
  - Tools assisted… but main problems need to be addressed manually
  - This work is driving the submission schedule (expected early 2025)

- Others: package, SEE simulations and GIT

Backup

Slim (I2C and I2C over fast commands)

- Size 400 x 300 um (part 3)



net	HK buffer	New buff	comments
Sc_load / wb_stb	D24	D16	Entire chip and 25ns pulse ➔ max Dx but no D20 and D24
Decoder 11b	D16	D6	From Pedro, large line RC (1,5k, 1,2 pF) ➔ D6-D16 small diff
Sc_data_out	D24	D6	Same
Sc_addr_out	D24	D6	Same