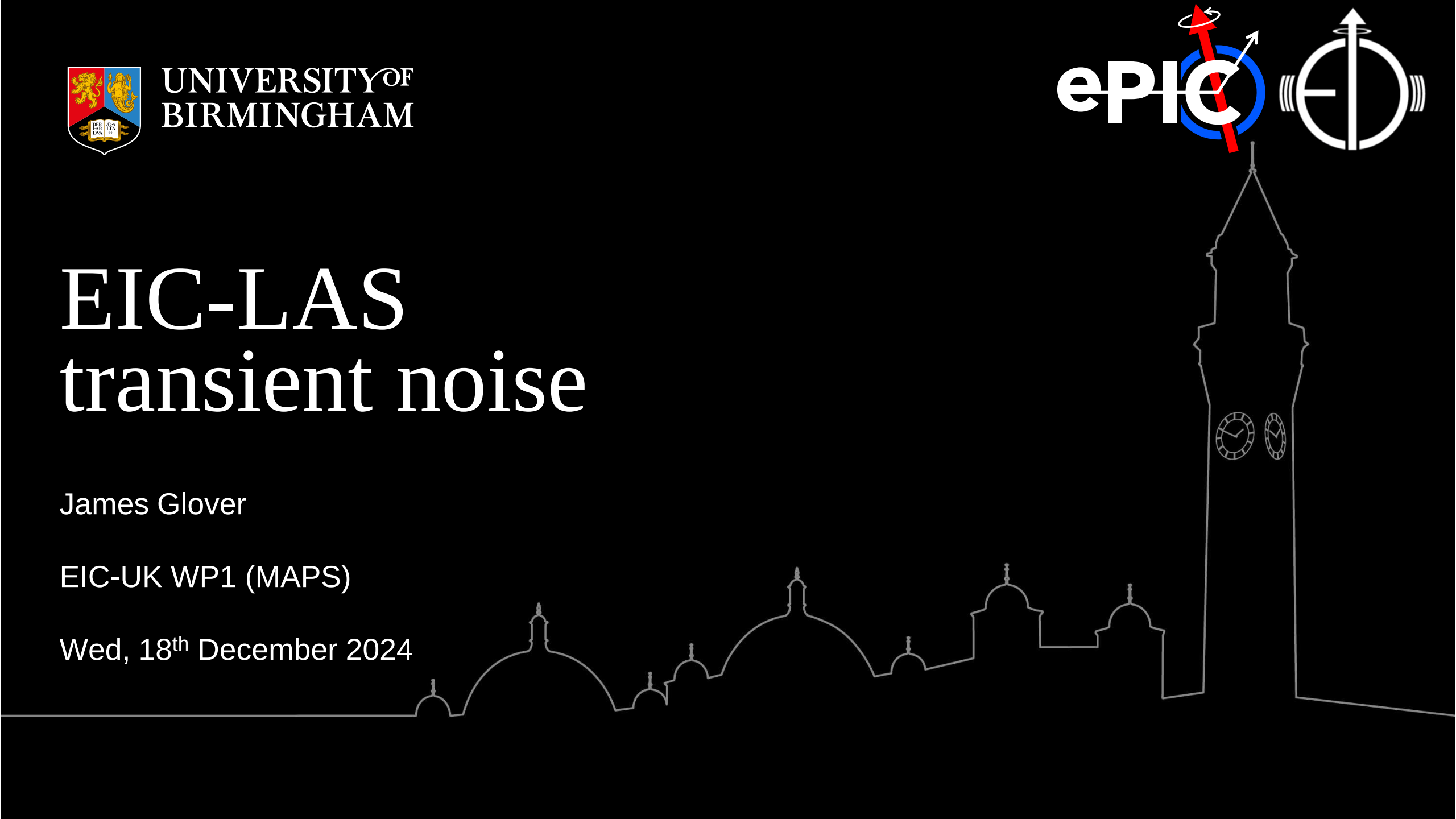


EIC-LAS transient noise

James Glover

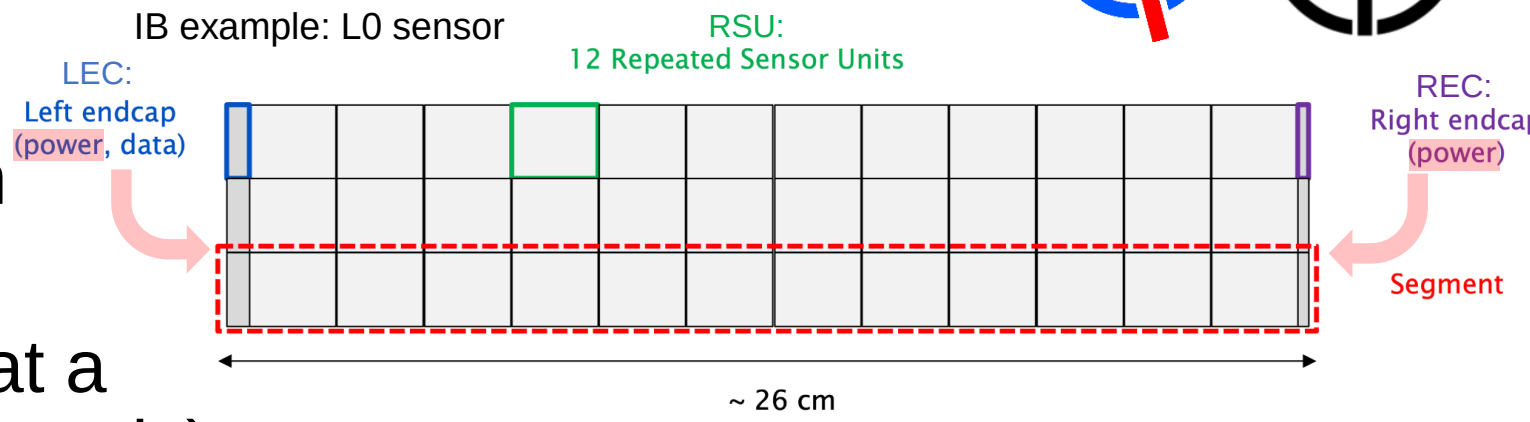
EIC-UK WP1 (MAPS)

Wed, 18th December 2024

Sensor Powering

MOSAIX (ITS3 & SVT IB):

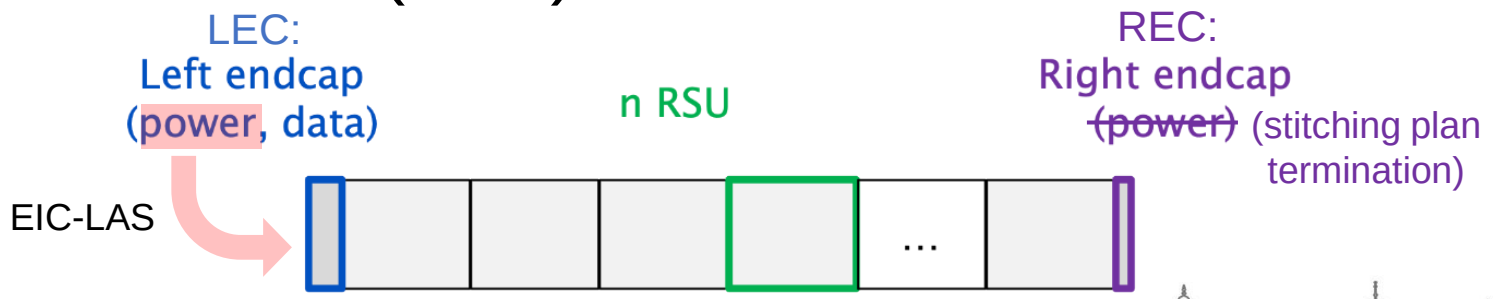
- Powering applied at both ends of the segment.
- Helps hold the voltages at a constant level (from both ends).



From: https://wiki.bnl.gov/EPIC/index.php?title=Si_Vertex_Tracker

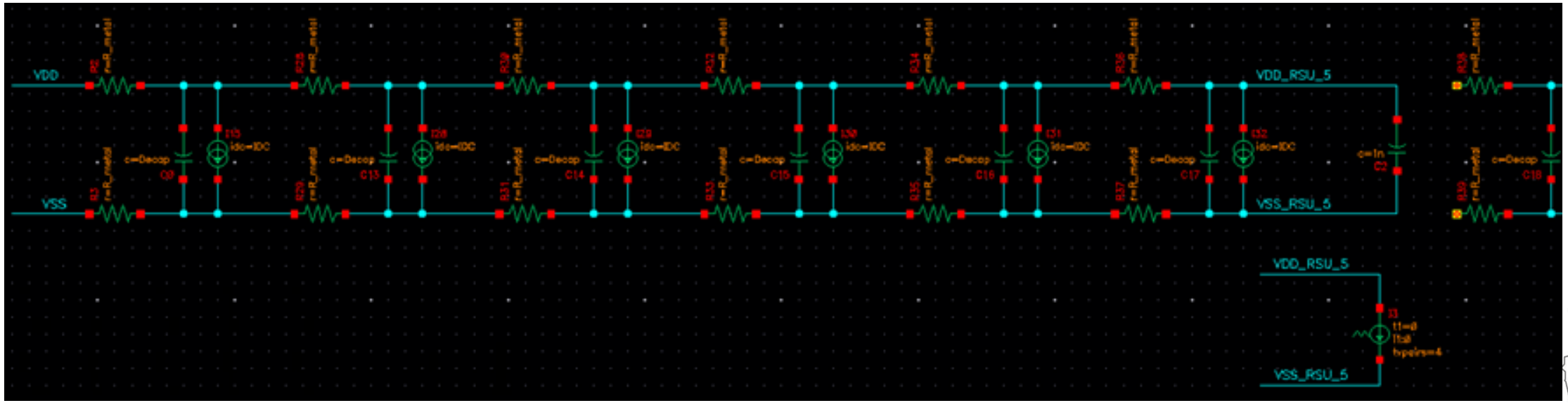
EIC-LAS (SVT OB & discs):

- Only powered from one side (LEC).
- REC is floating.



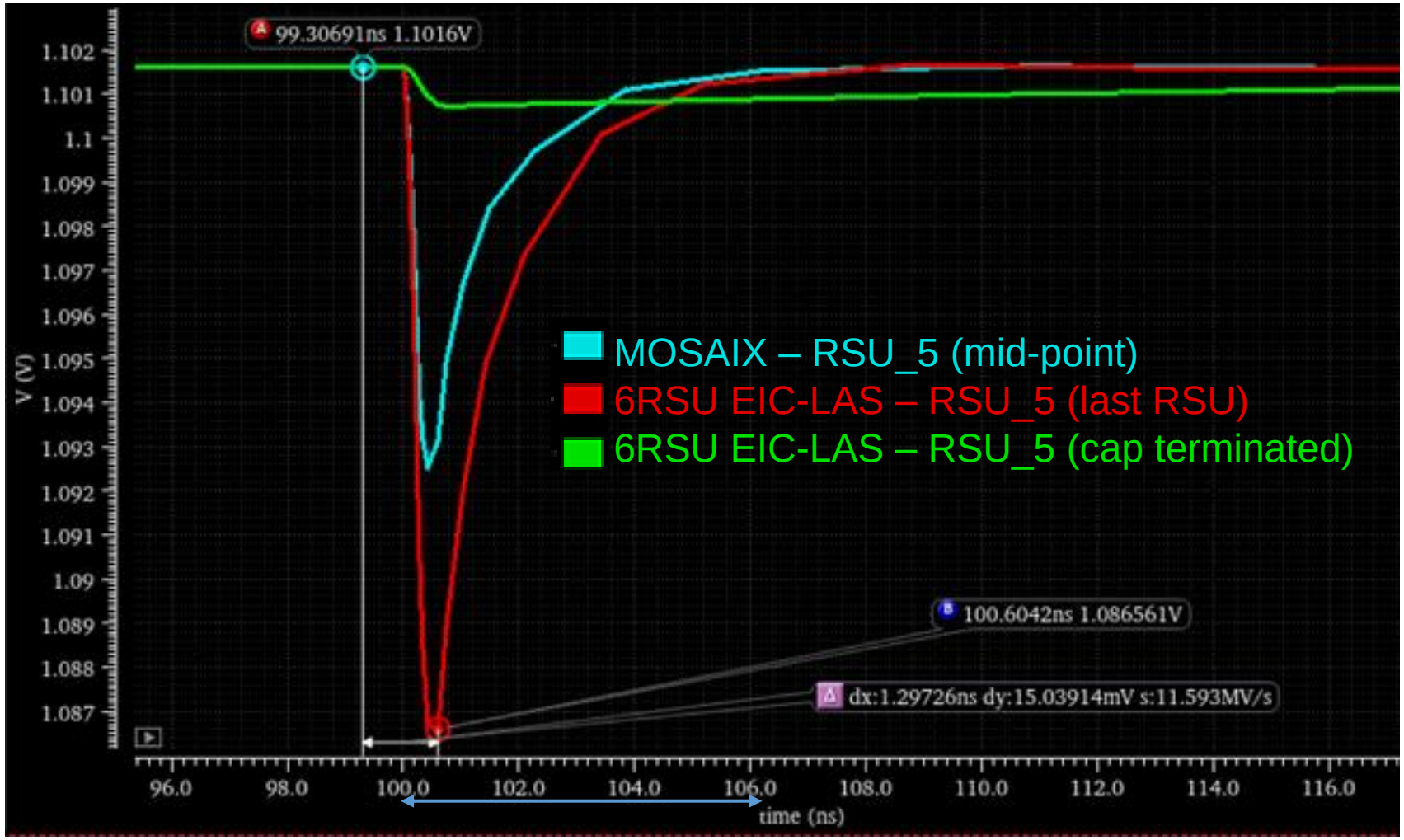
João's simulations

- João has been looking at how transient signals (such as the 160 MHz clock) could introduce noise into the power domains.



From João de Melo, part of an email thread (mostly) between the chip designers.

João's simulations



From João de Melo, part of an email thread (mostly) between the chip designers.

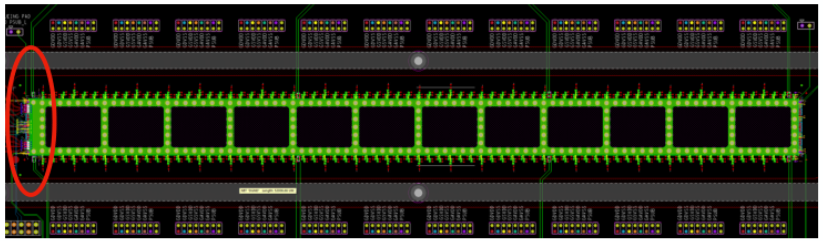
RSUs numbered from 0-11 (for the case of MOSAIX)

1 clock cycle (160 MHz) has a period of 6.25 ns.

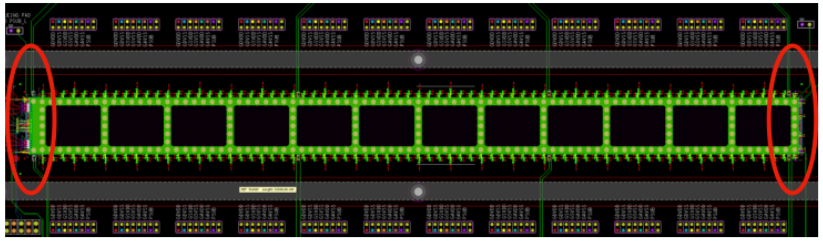
Testing plans

PROBE CARD OPTIONS

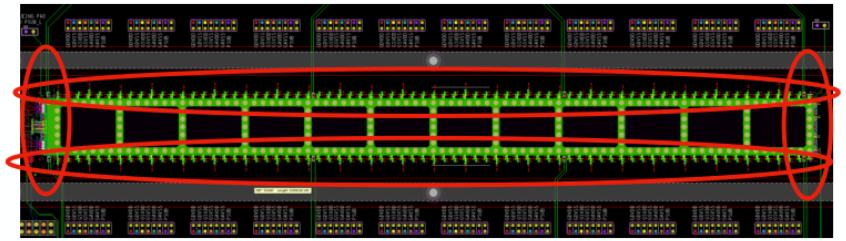
Probe card 1: Only needles for the Left Edge



Probe card 2: Needles for both Left and Right Edges



Probe card 3: Needles in all the four Left, Right, Top, and Bottom Edges



Probe card 4: Multipoint
Probe card 1 potentially can be used also for LAS

SVT WP2 are currently developing a vertical probe card.

- High speed testing of 10Gbps line for MOSAIX.
- All probe testing of EIC-LAS.

Probe card 1 is currently preferred.

- 1 design for all sensors.

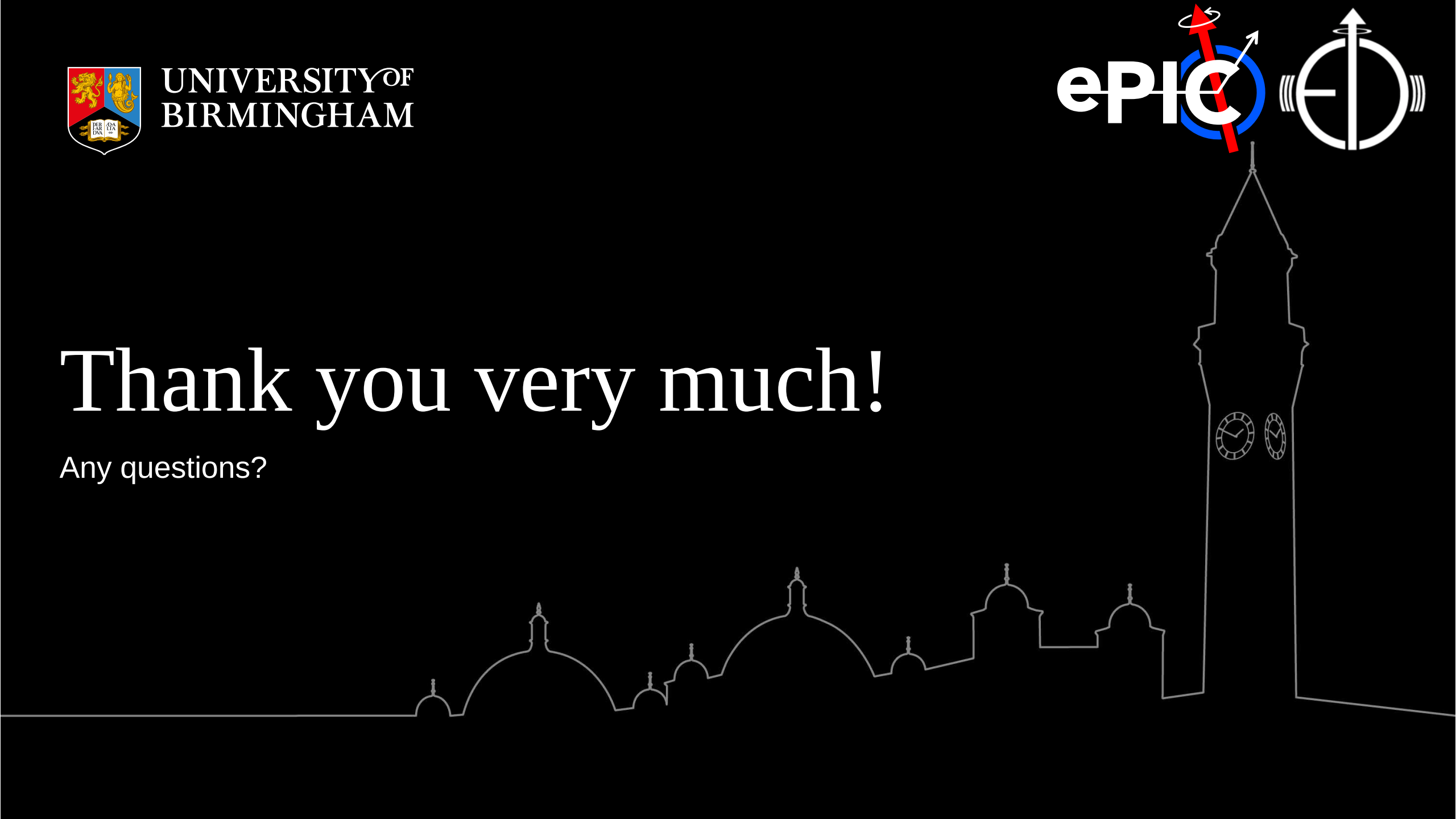
5

From “Update on testing strategy for MOSAIX”, WP2 meeting Thu 5th Dec ’24.

Testing complications

ITS3 chip designers have suggested a LEC only probe card should be fine, MOSAIX was designed with a floating REC in mind.

- All 12 RSUs can not be powered, but serialisers are all powered from the LEC.
  - For ITS3 a LEC only, vertical probe card is only used for HS tests.
  - Rest of chip functionality is tested with a full-segment, cantilever probe card.
- If the noise suggested by João is a problem and we need to add capacitors to the REC to attenuate this, a LEC only probe card is not representative of the way the chip will perform in the detector.
  - Only testing individual elements, not full chip.


UNIVERSITY OF BIRMINGHAM
ePIC
Thank you very much!
Any questions?

Additional (support) slides

Powering complications

ITS3 chip designers have suggested a LEC only probe card should be fine, MOSAIX was designed with a floating REC in mind.

- All 12 RSUs can not be powered, but serialisers are all powered from the LEC.
  - For ITS3 a LEC only, vertical probe card is only used for HS tests.
  - Rest of chip functionality is tested with a full-segment, cantilever probe card.
- If we adjust the powering for the serialisers (remove the on chip LDO), the serialisers will be affected by the same IR-drop as the other domains – Is this a problem?