# The Intermediate Silicon Strip Detector for sPHENIX⋆

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ARTICLE INFO

*Keywords*:
RHIC
sPHENIX
INTT
Silicon Detector
FPC
$\mu$-coax

ABSTRACT

A new strip type silicon detector has been developed to provide the sPHENIX experiment with precise charged particle tracking in central rapidity region. sPHENIX is a new detector at the Relativistic Heavy Ion Collider in the Brookhaven National Laboratory. The silicon strip detector is named intermediate tracker (INTT) composing the advanced tracking system of sPHENIX detector complex together with a MAPS-based silicon pixel vertex detector, a time projection chamber, and a micromegas based detector. The INTT detector is barrel shape and consists of 56 silicon ladders. Two different type of strip sensors of 78 $\mu m$ pitch and 320 $\mu m$ thick are mounted on an each half silicon ladder, each of which is segmented into 8×2 and 5×2 blocks whose strip length is 16 and 20 mm, respectively. Strips are read out with the FPHX chip which was developed for the FVTX detector installed in the PHENIX experiment at RHIC. The INTT detector construction was completed by the end of 2022 and installed to sPHENIX in Spring 2023. The sPHENIX detector including the INTT was commissioned with Au+Au beam collision at $\sqrt{s} = 200$ GeV in 2023.

## 1. Introduction

sPHENIX [1, 2] is a new detector and upgrade of the PHENIX detector [3] at the Relativistic Heavy Ion Collider (RHIC) in the Brookhaven National Laboratory. The PHENIX experiment was decommissioned in 2017. The sPHENIX experiment collects high statistics proton-proton, proton-nucleus and nucleus-nucleus data, enabling state-of-the-art studies of jet modification, upsilon suppression and open heavy flavor production to probe the microscopic nature of the strongly-coupled quark gluon plasma complementary to those measurements from the LHC experiments, and will allow a broad range of cold QCD studies [4].

The sPHENIX detector provides precision vertexing, tracking and electromagnetic and hadronic calorimetry in the central pseudorapidity region $|\eta| < 1.1$, with full azimuth coverage, at the full RHIC collision rate. A comprehensive assessment of these requirements has led to the development of the reference design shown in Figure 1. In its overall layout, sPHENIX folllows the typical geometry of modern collider detectors, with the tracking system consisting of a MAPS microvertex detector (MVTX), a silicon strip intermediate tracker (INTT) and a time projection chamber (TPC). A micromegas based detector (TPOT) partially covers the outside of the TPC acceptance for its calibration[5]. The calorimeter stack includes

⋆This work is supported by

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a tungsten/scintillating fiber electromagnetic calorimeter (EMCAL) and a steel/scintillator tile hadronic calorimeter (HCAL), divided into inner and outer parts. The inner HCAL sits inside a 1.5 T superconducting solenoid, which was refurbished from the decommissioned BaBar detector [6].

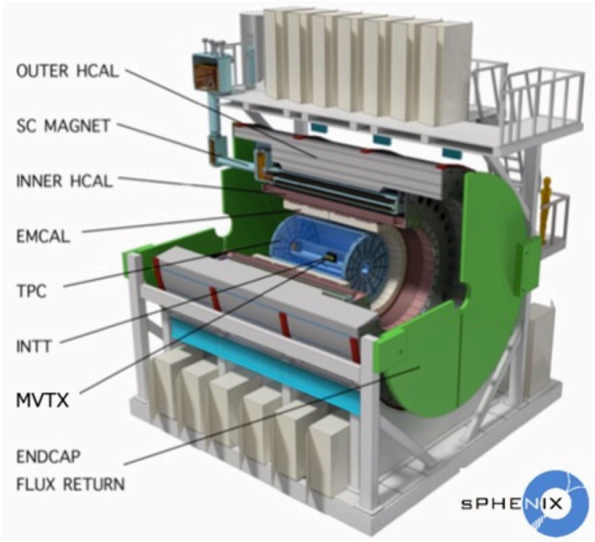


**Figure 1:** The mechanical drawing of the sPHENIX detector.

## 2. Detector Overview

The barrel type INTT detector consists of the inner and outer layers of INTT ladders. The adjacent ladders are staggered each other to prevent dead space between them in the azimuthal acceptance and forming inner and outer barrels by 24 and 32 ladders, respectively. Two silicon sensors and 26 FPHX readout chips [7] are mounted on a high density interconnect (HDI) flexible print cable forming an INTT silicon module. Two INTT modules are lined up longitudinally and glued to a carbon fiber composite support stave to form a INTT ladder as shown in Figure 2. Both glue and carbon fibers are high thermal conductive to diffuse heat generated by the FPHX chips. A water cooling system then removes the heat from the barrel through a carbon tube implemented inside the body of the stave.

The data of a given ladder are read out from both longitudinal ends for each silicon module, thus each HDI cable transmits data of half the ladder. The data are further transmitted to downstream from the HDI by a bus extender (BEX) cable [18] and a conversion cable (CC). The BEX is 1.11 meter long flexible print cable (FPC) employing liquid crystal polymer as a dielectric material to suppress losses in transmission lines. The conversion cable consisted of 3 components; 1) $\mu$-coaxial harness, 2) power and ground cables, 3) connector print boards in both ends. The downstream of the conversion cable is connected to the Read-out Card (ROC) which collects data from multiple half ladders and transmits reformatted data to further downstream electronics via an optical fiber connection.

**Table 1**
The dimensions of type-A and type-B silicon strip sensors [8].

| Type | # of blocks | active area dimension | strip pitch |
|---|---|---|---|
| A | 16 | 128 mm × 19.96 mm | 78 $\mu$m |
| B | 8 | 100 mm × 19.96 mm | 78 $\mu$m |

## 3. INTT Ladder

This section describes the electrical components and support systems used to read out and power the INTT. The silicon strip sensors and the FPHX readout chips are introduced in Sections 3.1 and 3.2, respectively. The HDI that provides power, bias voltage, and slow control signals to the sensor is discussed in Section 3.3. The stave support structure is discussed in Section 3.4.

### 3.1. Silicon Sensors

The silicon strip sensor [8] is single-sided and AC-coupled whose design was based on and modified from the FVTX silicon mini-strip sensors [7]. The sensors (model S14629-01) were fabricated by Hamamatsu Photonics KK as well as the ones of the FVTX. There are two types of sensors (type-A and type-B), which are distinguished by the length of strips and number of blocks. The type-A sensor has active area of 128 mm × 19.96 mm which is segmented into 8 in row and 2 in column blocks, each of which consisted of 128 strips in 78 $\mu$m pitch with 16 mm long, oriented towards the longitudinal direction. Similarly, the type-B sensor has active area of 100 mm × 19.96 mm which is segmented into 5 × 2 blocks, each of which consisted of 128 strips in 78 $\mu$m pitch with 20 mm long, also oriented towards the longitudinal direction. These dimensions of sensors are summarized in Table 1.

The small gap between adjacent blocks where the DC pads are laid out on the surface is completely active. The sensors were fabricated with p-implants on a 320 $\mu$m thick n-type substrate. The strips are AC-coupled and biased through individual 15 MΩ poly-silicon resistors to a typical operating voltage of 100 V. The aluminum metallization width on the strips is 20 $\mu$m which is wider than implant width of 10 $\mu$m to provide field plate protection against micro-discharges which is known to grow with radiation-induced increases in the leakage current. The strips are also protected by two p-implant guard rings and an n+ surround between the guard rings and the sensor edge. These designs are succeeded from the silicon strip sensors of the FVTX [7]. Figure 3 shows details of the sensor layout, including guard rings, bond pad locations, and mechanical fiducial marks.

In Figure 3, the strip runs horizontally (longitudinal direction). The readout lines of each strips are wired perpendicular to the strips orientation using the double metal technology. The other end of the readout lines are implemented with the readout pads which transmits to the FPHX chips with a wire bonding.

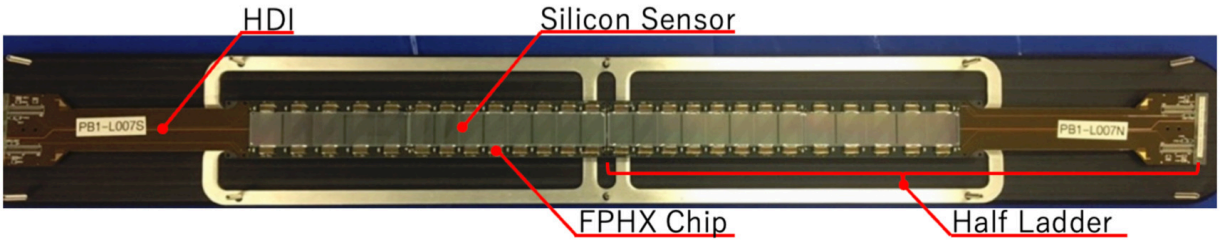


**Figure 2:** The photo of the INTT ladder with sensors facing up. Note the center line dividing the two halves of the sensor and rows of FPHX chips along the sensor edges.

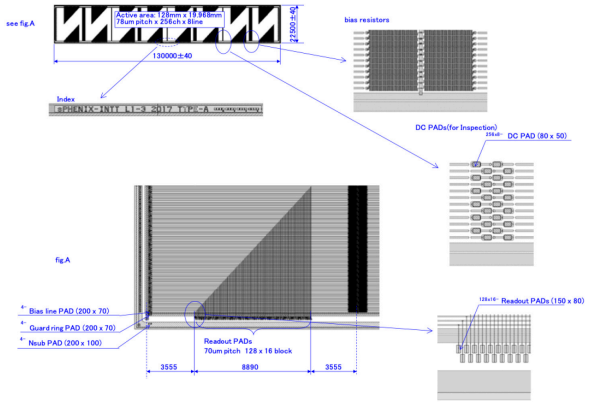


**Figure 3:** The schematics of the type-A silicon sensor [8].

**Table 2**
Specifications of the silicon strip sensors [8].

| Item | Specification |
|---|---|
| SSD type | AC-SSSD |
| Nominal operating voltage | 100 V |
| Bias Providing Type | Poly-Si bias |
| Poly-Si resistance | 15 MΩ |
| Silicon thickness | 320 $\mu$m |
| Strip implant width | 10 $\mu$m |
| Strip readout aluminum width | 20 $\mu$m |
| Number of strips per block | 128 |

## 3.2. FPHX chip

A custom 128-channel front-end ASIC, the FPHX, was developed at Fermilab for use in the FVTX Detector [7] of the PHENIX experiment at RHIC. The size of chip is 9 mm × 2 mm. The chip is operated at 2.5 V and consumes as low power as 64 mW per chip. The FPHX is a mixed-mode chip with two major and distinct sections, namely, the front-end analogue and the back-end digital parts. The analog section consists of an integrator/shaper stage followed by a 3-bit ADC. FPHX chip integrates and shapes signals from 128 channels of strips, digitizes and sparsifies the hit channels each beam crossing, and serially reads out the digitized data. The back-end is a novel trigger-less data push architecture that permits dead-timeless operation and high-speed readout

**Table 3**
Specifications of the FPHX readout chip [9].

| Item | Specification |
|---|---|
| Dimension | 9 mm × 2 mm |
| Operation voltage | 2.5 V |
| Power consumption | 64 mW |
| Number of Channels | 128 |
| ADC channels | 3 bits |
| Data Transmission | 200 MHz |

with very low latency. It has been designed to process up to four hits within four RHIC beam crossing. A fully processed hit pattern is zero-suppressed, contains a 7-bit time stamp in the unit of RHIC repetition frequency 9.4MHz (1/106 ns), 7-bit channel ID, and 3-bit ADC value. The data word is output over two LVDS serial lines in alternating order at up to 200 MHz clock rate. The summary of the FPHX specifications [9] is tabulated in Table 3.

In addition, the FPHX must be as "self-sufficient" as possible and provides its own internal bias voltages and currents with minimal external support circuitry. The user must be able to control internal parameters and biases, therefore a digital slow control interface is provided on each chip to enable programming. Adjustable parameters include gain, threshold, rise and fall time, input transistor bias current, channel mask, plus several additional fine tuning parameters [9].

## 3.3. High-density interconnects

The HDI is a flexible print circuit board to read out half the ladder which comprises two silicon sensors with 26 FPHX chips. The basic layer structure design of the HDI is succeeded from that of the FVTX [7]. The geometrical constraint for the silicon ladder is somewhat less tight for the INTT compared to that of the FVTX. The circuit design parameters such as line & space are thus relieved from the FVTX one, which resulted in improved yield rate at the fabricating process. The HDI was designed by Hayashi REPIC co. and fabricated by Yamashita Co. in Japan. The width of the HDI is 38 mm in the sensor area, while 43 mm in the connector end. The length is 398 mm which is the longest limit of the fabrication in the industry for the

multilayer FPC in the automated manner using dedicated fabrication machines.

The HDI is seven layered and is the stack up of 9 $\mu$m thick electrolytic copper foil, 50 $\mu$m thick polymide, and 15 to 25 $\mu$m thick resin glue. The total thickness is 418 $\mu$m in the sensor area. The total thickness governed by copper layers is 68 $\mu$m which is the major component of the material budget of the INTT ladder as to be discussed in Subsection 3.5. The top and bottom copper foil layers were plated with 15 $\mu$m thick copper[1]. Shown in Figure 4 is the cross section of the seven layer structure of the HDI.

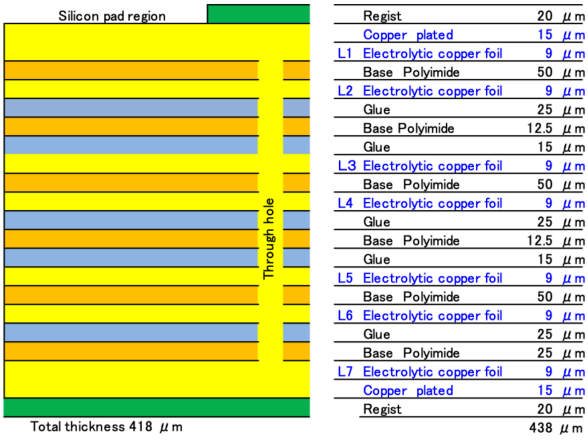


**Figure 4:** Seven layer structure of HDI.

The schematic of each layer is shown in Figure 5. From the top to the bottom layers, each layer has dedicated purpose to transmit bias for the type-B silicon sensor (L1), analogue ground (L2), signals (L3), DC powers for the analogue and digital parts of FPHX (L4), signal (L5), digital ground (L6), and bias for the type-A sensor and signals (L7). There are two thermistats implemented on the L7 to monitor the cooling status of the heats generated from the FPHX chips during the operation.

There are 122 signal lines total. They are 52 output data and 8 slow control & clock LVDS pairs, also two dedicated lines to inject calibration pulses to FPHX. Signal transmission lines are mainly placed in the layers 3 and 5 to be shielded from external electromagnetic (EM) fields by keeping these layers between solid copper layers which are assigned for either analogue or digital grounds or the DC power. The line & space is 60 & 60 $\mu$m, respectively. The characteristic impedance is designed to be 100 $\Omega$ differential for these LVDS pair lines to ensure matching with the rest of the readout cable chain.

Some signal lines running in sensor region in L7 is not succeeded design from the FVTX. This signal lines were bi-product of the philosophy to keep the HDI width as narrow as possible and thus couldn't fit within the signal layers. The narrow width allows us to build the barrel detector as round as possible by minimizing physical interference between adjacent ladders. Since the back plane of L7 is not shielded by neither the solid foil ground nor power layers, the signal lines are exposed to the external EM fields, the length of the lines were kept as short as possible (< a few cm). Figure 6 depicts the photo of the HDI cables with L1 and L7 face up. The major specifications of HDI cable are summarized in Table 4.

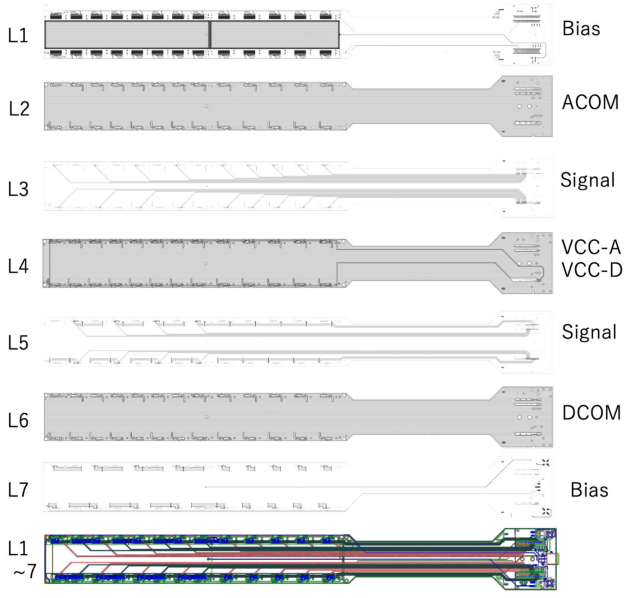


**Figure 5:** The schematic of each layer of the HDI. The ACOM and DCOM layers provide analogue and digital grounds to FPHX chips, respectively. The 2.5 V power solid lines for the analogue and digital parts of the FPHX chip shares the L4, but they are electrically isolated within the layer. The bottom schematic figure shows the overlay of all 7 layer's line patterns depicted in different colors.

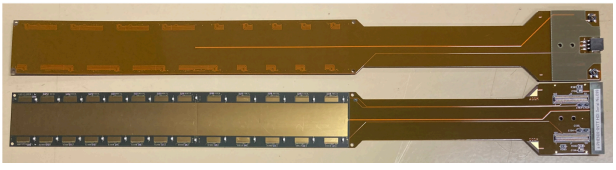

**Figure 6:** The photo of the HDI cables with L1 and L7 face up.

There are a pair of connectors for data, LV power for the FPHX, and grounds are implemented in the end of the HDI. The model of the data connector is Hirose co. DF18C-100DP-0.4V(51) plug, which consists of 100 channels with 400 $\mu$m pitch between conducting pins. There are also two bias connectors and 3-pin thermostat connectors implemented in the connector end area of the HDI.

[1]The copper plate was 15 $\mu$m thick for the 1st and 2nd batches of the HDI production. The thickness increased to 25 $\mu$m for the 3rd batch in HDI production. The total radiation length of the silicon ladder is increased by 3%.

**Table 4**
Specifications of the HDI cable. The characteristic impedance is for the LVDS pair.

| Item | Specification |
|---|---|
| Dimension | 398 mm × 38 mm |
| Width of connector ends | 43 mm |
| Total thickness (sensor pad region) | 418 $\mu$m |
| Conductive material | Copper |
| Dielectric material | Polymide |
| Number of layers | 7 |
| Number of signal lines | 122 |
| Line and space | 60 & 60 $\mu$m |
| Characteristic impedance | 100 Ω |

**Table 5**
The specifications of the CFRP prepreg.

| Item | Specification |
|---|---|
| CFRP prepreg | NT91500-520S [11] |
| Carbon fiber | XN-90 |
| Resin | 25R epoxy |
| Resin weight fraction | 20 % |
| density | 2.19 g/cm$^3$ |
| Thermal conductivity | 500 W/mK |
| Tensile module | 860 GPa |
| Tensilie strength | 3430 MPa |
| Thickness | 100 $\mu$m |

### 3.4. Stave

One mechanical support mainly made of carbon fiber composite (CFC) skins called stave. The stave itself plus an extension for mechanical attachment spans 497 mm long and 38 mm width matching with the HDI width around the sensor area and accommodates two silicon modules per stave forming the INTT silicon ladder. The heat load expected from each half ladder is: 64 mW × 26 FPHX chips ∼ 1.7 W. The total heat load over the entire INTT is about 186 W for 112 half ladders.

The stave is required not only the rigidity as the support structure, but also high thermal conductivity to dilute local heats generated by the FPHX chips. The main component of the stave is made of a carbon fiber reinforced plastic prepreg (CFRP) in order to fulfill the requirement. The GRANOC prepreg sheet model NT91500-520S of Nippon Graphite Fiber co. was employed. It consists of the 25R epoxy and XN-90 carbon fiber with a high thermal conductivity of 500 W/mK, with resin weight fractions of 20% [11]. The thickness of 0.10 mm with the density of 2.19 g/cm$^3$ prepreg provides satisfactory mechanical strength as tensile module and strength of 860 GPa and 3430 MPa. The specification of the CFRP prepreg is summarized in the Table 5.

The stuck up of the stave and the mechanical attachments of its edge are shown in Figure 7. The top and bottom shells of the stave are flat and formed CFC plates. The formed plate is U-shaped to accommodate the 3 mm diameter cooling tube between two CFC plates in the middle with the 3 mm thick ROHACELL 110 RIST form [12] that taper down near the edge forming a structural core. A cooling tube is made of Toreyca T700C carbon fiber prepreg [10] fabricated in Kimuraya co., Japan. The NT91500-520S sheet is unidirectional in the high thermal conductivity. Each CFC plates are baked up with three layers of the sheet orienting its unidirectional high thermal conductivity in longitudinal, transverse, and longitudinal, respectively to secure somewhat omnidirectional rigidity. The thickness of the CFC plate is 0.33 mm and the total thickness of the stave is 3.76 mm.

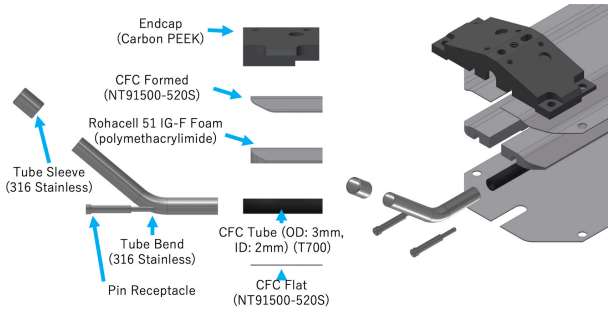


**Figure 7:** The mechanical design of the edge of the stave. The HDI is assembled on the bottom flat CFC plate.

The mechanical attachment of the both edge of stave consisted of the end caps, SUS316 cooling tube extensions, and pair of pin receptables manufactured by Mill-Max MFG co. for grounding. The endcap is made of Ketron CA30 PEEK [13] manufactured by Mitsubishi Chemical co. The stainless tubes and the cooling tubes were glued using the Henkel LOCTITE EA 9396 adhesive [14] to be leak tight. The rest of pieces of the stave are assembled using the graphite conductive EP75-1 epoxy adhesive (MasterBond co.) [15]. Shown in Figure 8 is the engineering drawing of the INTT stave. The material list of stave components and specifications are summarized in Table 6.

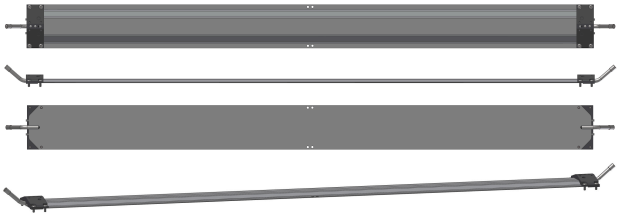

**Figure 8:** The INTT stave. The HDI is assembled on the bottom flat CFC plate.

The staves were fully fabricated in Asuka co., Japan including the baking process of the CFC plates. In order to secure the quality of the stave to meet the requirement, following four tests were examined to every cooling tubes (after the stainless extensions are glued) and staves and only ones which passed the examination were employed.

**Table 6**
The material list of stave components and specifications.

| Item | Model/Specification |
|---|---|
| Dimension | 497 mm × 38 mm |
| Total thickness (sensor region) | 3.76 mm |
| Adhesive for stave assembly | MasterBond EP75-1 [15] |
| Structure Core | ROHACELL 110 RIST [12] |
| End cap | Ketron CA3 PEEK [13] |
| CFC Cooling tube | Toreyca T700C [10] |
| Cooling tube extension | SUS316 |
| Cooling tube adhesive | Henkel LOCTITE 9396 [14] |

1. Burst test : Keep the tube at the high pressure of $60\pm2$ psi and won't burst for 1 hour.
2. Leak test : less than 0.2 ml-mbar/min.
3. Heat cycle test : $40 \leftrightarrow 0$°C (one cycle).
4. Flatness $< 100$ $\mu$m of the flat side of the stave and alignment positions are within specified tolerance.

The staves were assembled with only cooling tubes which qualified the item 1 and 2.

### 3.5. Material Budget

The material budget of the silicon ladder is summarized in the Table 7. The total thickness of the silicon pad area of the ladder is 4.57 mm and its effective radiation length $X/X_0$ is 1.19 %. Two largest contributions to the budget are the HDI and the stave and their radiation lengths are $X/X_0 = 0.37\%$ and $X/X_0 = 0.39\%$, respectively.

The material budget of the HDI is largely governed by the copper layers. As shown in the Figure 4, there are 7 layers of 9 $\mu$m thick copper layers which simply add up to 63 $\mu$m total. Furthermore both top and bottom surface layers are plated by 15 $\mu$m thickness copper. While the simple stack up of these copper thickness results in 93 $\mu$m, the effective amount of copper in the signal layers are much less unlike solid ground layers. The effective copper thickness was estimated based on the residual copper fraction after the etching process of the HDI fabrication and summarized in the Table 8. The effective total thickness so estimated is 37.6 $\mu$m, which is approximately 40% of simple adds up of 93 $\mu$m, and the radiation length $X/X_0$ is 0.26. The total thickness of polymide and glue layers is 325 $\mu$m and that of $X/X_0$ is 0.11. The total radiation length of the HDI in the silicon pad area is thus 0.37.

The silicon sensor and HDI were assembled using the electrically conductive silver epoxy, i.e. Henkel LOCTITE ABLESTIC 2902 adhesive. The radiatn length for 50 $\mu$m thick silver epoxy was estimated to be $X/X_0 = 0.14$ based on the mixing ratio of the silver powder and the mixing ratio of 0.21:0.79 [16].

In order to propagate heats generated by the FPHX chips, high thermally conductive glue was employed to assemble the HDI and the stave. The model of the glue is 3M$^{\text{TM}}$ thermally conductive epoxy adhesive TC-2810 [17]. The radiation length for the 50 $\mu$m thick glue makes very small contribution for the total material budget of the silicon ladder unlike the silver epoxy.

**Table 7**
The material budget of the silicon ladder. The TC-2810 is the thermally conductive glue.

| Item | Thickness mm | Radiation Length $X/X_0$ % |
|---|---|---|
| Silicon Sensor | 0.32 | 0.30 |
| Silver epoxy | 0.05? | 0.14 |
| HDI | 0.42 | 0.37 |
| TC-2810 | 0.05 | 0.02 |
| Stave | 3.76 | 0.33 |
| Total | 4.57 | 1.19 |

**Table 8**
The effective thickness of the HDI's copper layers.

| Layer | Function | Residual copper fraction % | Effective thickness $\mu$m |
|---|---|---|---|
| 1 | Bias + AGND | 71.3 | 10.7 |
| 2 | AGND | 93.5 | 8.42 |
| 3 | Signal | 6.5 | 0.59 |
| 4 | Power | 94.0 | 8.64 |
| 5 | Signal | 7.2 | 0.65 |
| 6 | DGND | 93.2 | 8.38 |
| 7 | Bias+Signal | 4.7 | 0.42 |
| | Total | | 37.6 |

## 4. INTT Readout Cables and Front End Circuit Board

Since the entire INTT barrel needs to be accommodated within the inner diameter of the TPC detector [1, 2], the signal from the barrel has to be transmitted all the way to the outside of the TPC volume because the downstream electronics for signal-processing, namely read out cards (ROC), which is reuse from the FVTX detector, can not fit within the inner diameter of the TPC. Massive raw data generated from the INTT have to be transmitted at high-speed to the ROC through curved cable path for longer than 1 m. Because no commercial cable satisfies the requirement, a novel cable, namely bus extender cable has been developed based on flexible printed circuits (FPC). This technology can satisfy the requirements of the high-density signal lines, the flexibility and the long cable length, simultaneously. On the other hand, the specification of the line & space of the bus extender prevented its connector end design to be compatible with the input connector ports of the existing ROC. Therefore another 15 to 25 cm adapter cable, that is called conversion cable, was developed to interconnect between the bus extender and the ROC. In order to guide the connection smoothly without introducing any stress at the input connector of the ROC, the flexibility in 3-dimension for the conversion cable was required to absorb the geometrical mismatch of the

downstream end of the bus extender and the corresponding input connector location of the ROC.

### 4.1. Bus Extender Cable

The details of the bus extender (BEX) cable is discussed in elsewhere [18]. Only key features of the BEX are described here. This FPC comprises four layers of three flexible-copper-clad laminate (FCCL) as shown in Figure 9. The top and third layers are for the digital and analogue grounds, respectively. The second layer is assigned for signal lines, while the bottom layer is designated to the power supply lines for the FPHX chips. The four layer structure is primarily driven by the fabrication constraint in contrast to the seven layer structure of the HDI. The yield rate is the one of the big concern of the BEX. Its main driver is the signal layer due to its required microfabrication accuracy over the extraordinary length of 1.11 meters. Reducing the number of signal layer was one of the solution to minimize the risk in the fabrication process. This is the reason the BEX employed different layer structure from the HDI and all signal lines were thus integrated into a single layer.

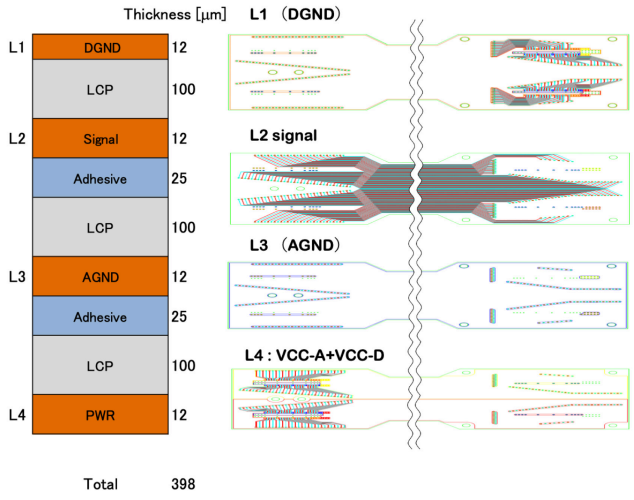


**Figure 9:** Four layer structure of the BEX (left), and schematics of each conductive layer (right) from L1 to L4.

The polymide is the most popular choice as a dielectric material for the FPCs in the market and its fabrication technology is well established in the industry. For the bus extender case, it was mandatory to challenge to employ the liquid crystal polymer (LCP) as the dielectric material for its lower transmission loss of the signal amplitude and the availability of thicker FCCLs in the industrial market compared to the polymide. These features are advantage for the bus extender of which design is strictly constrained by the precision and yield limit in the fabrication process due to its extraordinary long length as the FPC. The realistic limit of the line & space for the BEX was found to be 130 & 130 $\mu$m, respectively to achieve a reasonable yield rate in the fabrication factory, Print Electronics Laboratory. Given

**Table 9**
Specifications of the BEX cable.

| Item | Specification |
|---|---|
| Dimension | 1.11 m × 34 mm |
| Width (connector region) | 43 mm |
| Total thickness | 398 $\mu$m |
| Dielectric material | LCP |
| Dielectric model | Panasonic FELIOS [19] |
| Dielectric layer thickness | 100 $\mu$m |
| Bonding sheet model | A26R [20] |
| Bonding sheet make | Arisawa Manufacturing |
| Bonding sheet thickness | 25 $\mu$m |
| Number of layers | 4 |
| Number of signal lines | 122 |
| Line and space | 130 & 130 $\mu$m |

the line & space, the thickness of the dielectric material is required to be as thick as 100 $\mu$m to match the differential characteristic impedance of 100 Ω. While such a thick polymide is not available in the industrial market, the 100 $\mu$m thickness is available in the FERIOS model LCP from Panasonic co. [19]. The key specifications of the LCP to make the low transmission loss possible are the dielectric constant $\epsilon = 3.3$ and the dissipation factor, $\tan\delta = 0.002$, respectively.

For the choice of the bonding sheet, the model A26R of Arisawa Manufacturing co., ltd. [20] was employed with the thickness of 25 $\mu$m for its characteristics of the low dielectric constant. As a consequence of R&D, this was also a crucial choice to achieve the decent yield rate in the plating process of through holes [18] in Taiyo Manufacturing Co. ltd. since the fabrication technology for the LCP has not been as well established as the polymide. The specifications of the BEX cable are summarized in Table 9.

The pair of DF18C-100DS-0.4V(81) receptacle connectors manufactured by Hirose Electric co. ltd. are implemented at the both ends of the bus extender as shown in the Figure 10. The space between a pair of DF18 plug is 26 mm which is incompatible with the 10 mm spacing of the input connector pair of the ROC. This extra spacing between the connector pair of the BEX is caused by the difficulty to wire 122 signal lines of 130 & 130 $\mu$m line & space into the short connector spacing. Due to the incompatibility of the connector layout between the BEX and the ROC, another readout cable was introduced which converts the connector spacing from the BEX to the ROC one. The cable is named as the conversion cable.

The bus extender was thus successful to moderate the signal attenuation, however it is still not negligible level due to its extraordinary long cable as multilayered FPC. The performance of signal transmission was evaluated by following three measurements; 1) S-parameters, 2) eye-diagram, 3) time-domain reflectometry (TDR). From the S-parameter measurement, the insertion and reflection losses are -2.7 and -23 dB, respectively at 200 MHz. The measured eye-diagram is shown in Figure 11. The waveform is confirmed to exhibit

**Figure 10:** A photograph of the 1.11 meter long BEX cable.

**Table 10**
The performance of the BEX cable. The characteristic impedance is the differential of the LVDS pair.

| Item | Performance |
|---|---|
| Insertion Loss | -2.7 dB |
| Return Loss | -23 dB |
| Characteristic impedance | 90 Ω |

a sufficient margin to a defined mask[2] (solid hexagon) in the middle of figure by observing 1 million waveforms of the 200 MHz signal. The characteristic impedance was measured 90 Ω differential in the TDR measurement. This is 10 % smaller than the default 100 Ω, it is confirmed to be permissible by the return loss measurement of the daisy chain with conversion cable as discussed in the subsection 4.2. The performance of the BEX cable is summarized in the Table 10.

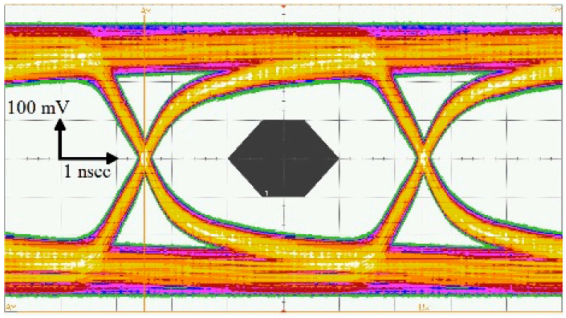


**Figure 11:** The measured eye-diagram of the BEX as a result of transmitting 200MHz signals for 1 million times [18].

## 4.2. Conversion Cable

As is discussed in previous sections, the FPC is known to be the first choice as the technology to satisfy the high performance requirements of signal transmission, high signal line density, and the flexibility. However, the FPC has a difficulty to satisfy an additional and unique requirement as the last stage of the readout cable series. It is the flexibility in three dimensions to connect the downstream end of the BEX and the input connector ports of the ROC board without introducing any stress at the connection. Due to the geometrical mismatch between the INTT barrel ladders and the input connector layout of the ROC, the flexibility in three dimension is crucial for the conversion cable. The flexibility of the FPC cable has a directivity and tends to induce a stress at the connector end to bend the cable to the transverse direction of the cable plane.

A $\mu$-coax technology is a suitable choice for such a case. The advantage is that there is no directional flexibility as the nature of the coaxial cable. Although the signal line density cannot be as high as the FPC, the three dimensional flexibility offers relevant trade-off as the INTT readout design. According to the engineering study, the FPC solution requires as many as 14 different design in curving and length design to interconnect mismatching connector geometries between the BEX and input connectors of the ROC due to its lack of flexibility. It is avoidable to have spare cables of all designs from the risk management point of view, which leads to a quite cost inefficient product. The $\mu$-coax solution reduces the number of designs to be only two in different length.

The CABLINE-UX II model manufactured by I-PEX Inc. [21] was employed as the last stage of the signal transmission cable chain for the INTT ladder. The model comprises an AWG#44 harness manufactured by Aosen co. The harness made of silver plated copper alloy as a center conductor insulated by 30$\mu$m thick perfluoroalkoxy alkane (PFA) dielectric material from tinned copper alloy wire wrapping in right hand ray as the outer spiral shield. The shield is covered by the outer most jacket made of the PFA as well forming four-layered coaxial cable of the total thickness of 0.24 $\pm$ 0.01 mm. The characteristic impedance of the harness is 45Ω (90 differential for a LVDS pair). A slim plug and small connectors are assembled both end of harnesses which bundle 50 harnesses in the wire spacing of 0.25 mm pitch. The harness bundle is wrapped by an acetate cloth adhesive tape for an utility purpose.

The conversion cable which interconnects between the BEX and the ROC consists of three $\mu$-coax bundles, two power and two ground cables, and the PC boards in both ends. The AWG#24 power and ground cables are assembled with HJ-3 male pin manufactured by MAC EIGHT co. ltd. in both ends. The male pin and the receptacle connection is secured by the HH-3-R lock. The wire gauge is optimized to be AWG#24 to drop the voltage for proper amount to provide the power at the FPHX chip power from the slightly higher regulator voltage output at the ROC, to be discussed in the Section 4.3. Three UX II receptacles and four HH-3-G sockets (manufactured by MAC EIGHT co. ltd.) are implemented on the top side of the PC board and two DF18C-100DS-0.4V(81) receptacle connectors are implemented on

[2]Private communication with the FPHX chip developers.

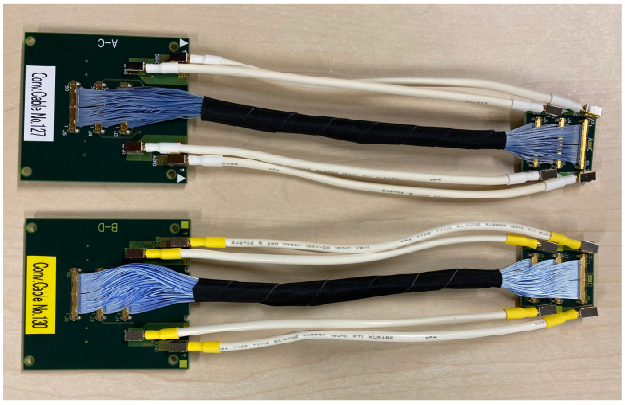


**Figure 12:** Conversion cable type-AC (top) type-BD (bottom). The bundles in the middle of the cable are 15 cm length $\mu$-coax harnesses while four white jacket cables are the power and the ground cables. The larger PC board is the connector for the BEX side and smaller one is the one for the ROC side.

**Table 11**
Specifications of the conversion cable. The characteristic impedance is given in differential of the LVDS pair.

| Item | Specification |
|---|---|
| $\mu$-coax model | CABLINE-UX II [21] |
| Harness model | Aosen co. SP-10005-027A |
| Harness AWG | 44 |
| Characteristic impedance | 90 Ω |
| Number of harness per bundle | 50 |
| Number of bundle | 3 |
| Power/ground cable AWG | 24 |
| Number of power cable | 2 |
| Number of ground cable | 2 |
| Length | 15 & 25 cm |

the bottom side of the board. The PC board is fabricated in Hayashi-REPIC co. ltd. and eight layered with dedicated layer for the digital and the analogue powers and grounds layer, respectively. The dimensions are 48 mm wide × 52 mm long for the BEX end to match the size of it's connector end, while the ROC side is rather compact; 25 mm wide × 25 mm long. There are two types of conversion cables namely "type-AC" and "type-BC" and the difference is the channel mapping to be compatible with the channel map differently designed for the column-A&C and column-B&D of the input ports on the ROC. There are two different kind of lengths which are 15 and 25 cm harnesses, the power and ground cables.

### 4.3. ROC

The ROC is the multilayered circuit board implemented at outside of the TPC volume. The ROCs were refurbished after the FVTX operation in the PHENIX experiment and reused for the INTT. Details of the ROC is described in else where [7]. In this article, any aspects of the different or customized usage of the ROC from the FVTX is discussed.

There are twelve pairs of DF18C-100DP-0.4V(51) plug connectors and four pairs of DF18C-60DP-0.4V(51) are implemented in the ROC as input ports for a half ladder. The DF18C-60DP-0.4V(51) plug connector has 60 pins and is not used for the INTT.

The ROC boards are originally implemented with 2.5 V regulators to provide analogue and digital powers for the FPHX chips, while operation voltage of the FPHX chip is 2.5 V for the both analogue and digital [9]. The voltage drop in the power transfer line was minor in the FVTX owing to its short readout cable chain and low power consumption of the FPHX chip. On the contrary, this is not the case for the INTT due to its extraordinary long readout cable chain as it has been discussed in previous sections. The FPHX has to be operated with higher LVDS current for its output data transmission than that of the FVTX's in order to secure the signal amplitude to be kept well above the receiver driver threshold. As a consequence, the FPHX is required to be operated with the higher power consumption mode in the INTT.

The maximum drawing current is measured to be 0.21 and 0.42 A per a half ladder (26 FPHX chips) for the analogue and the digital power of the FPHX chips, respectively. Although readout cables are designed to allocate reasonably large cross section or AWG for the power transmission lines as described in the readout cable sections, and in fact the resistances of these cables around a couple hundred mΩ. The resulting voltage drop of the daisy chain of the readout cables amounts as much as 0.2 to 0.4 V which is sizable enough for the FPHX chips to mulfunction due to insufficient voltage supply.

In order to compensate the voltage drop, the surface mounted regulators for the FPHX power are upgraded to supply larger output voltage. The upgraded regulators are same models from the original ones so that the pin layouts match with the pad pattern of the ROC. Newly implemented regulators are MCP1700-2802E/TT and MCP1726-3002E/MF (Microchip Technology Inc.), for analogue and digital powers, respectively and their outputs are 2.8 and 3.0 V, respectively. While the drawing currents are increased accordingly with the higher voltage outputs, the supplied voltages at the FPHX location are calculated to be 2.5 ∼ 2.6 V.

## 5. Radiation Hardness

In the INTT readout system discussed in Section 4, there are a few materials of which radiation hardness is not known or known to be not durable. In this section, the radiation hardness is discussed for these items in order to address the concern. The study of the potential radiation damage of the ROC boards in the PHENIX period is also discussed here.

### 5.1. Bus Extender

The FPC with standard polymide widely used under radiation environments and its radiation hardness is well established. On the other hand, the LCP is relatively new material as the dielectric layer of the FPC and its radiation

hardness of the FPC with LCP has not been established as well as that of the polymide. The radiation hardness of the LCP material itself is proven to be as durable as polymide [23] though, the radiation hardness of the bonding sheet [20] employed for the BEX is not known. Here the overall mechanical characters of the BEX after assembly was measured before and after a radiation exposure rather than investigating the radiation hardness of the bonding sheet individually. The primary concerns are the degradation in the flexibility of the BEX and the peel strength of the bonding sheet due to the radiation damage.

A few samples of the BEX cable were exposed to $^{60}$Co source for 7.2 kGy, 685 kGy, 1.45 MGy at National Institutes for Quantum Science and Technology, Japan. The expected radiation dose at the location where the BEX is installed in sPHENIX is approximately 5 kGy for five years operation[3]. The mechanical performances were evaluated by following two tests; 1) stress test to evaluate the flexibility, and 2) peel strength test between the copper and the LCP layers [18]. As the test item 1), the Young's modulus was measured of the samples before and after the radiation exposure. Shown in the Figure 13 is the Young's modulus of these samples based on the natural frequency measurements of each samples. No degradation of the flexibility was observed within the accuracy of the measurements (7%) in any samples. The error was estimated by the standard deviation of multiple samples within the same radiation dose group.

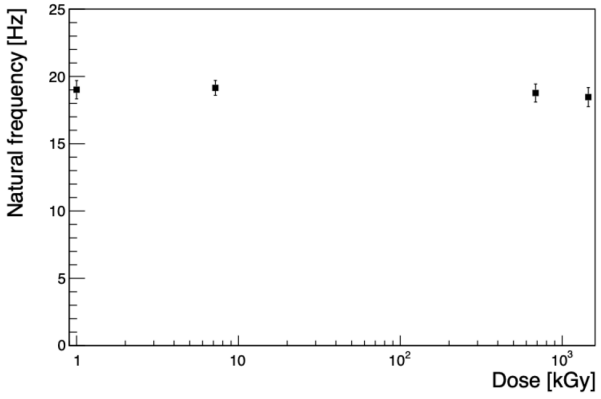


**Figure 13:** The Young's modulus measurement results of samples exposed to various radiation dose. The vertical axis is the natural frequency in the unit of Hz, while the horizontal axis is the radiation dose in the unit of kGy. The measurement of the sample with no radiation exposure is plotted at 1 kGy on purpose.

On the other hand, as shown in the Figure 14, approximately 50% and 70% degradations were observed in the peel strength for 685 kGy and 1.45 MGy samples, respectively. However the measured peel strength of 18 N/cm for 7.2 kGy sample which is similar level of typical polymide-based FPC and proven to be sufficiently strong. Although the safety margin to keep this peel strength for possible unexpected extra radiation dose may be marginal, it is unlikely that FCCL layers fallen a part by its own gravity even the peel strength got weaken by 50%. The conclusion was thus made the radiation hardness of the BEX suppose to be durable for three years of sPHENIX operation.

[3]including extra two years of operation beyond officially approved three years.

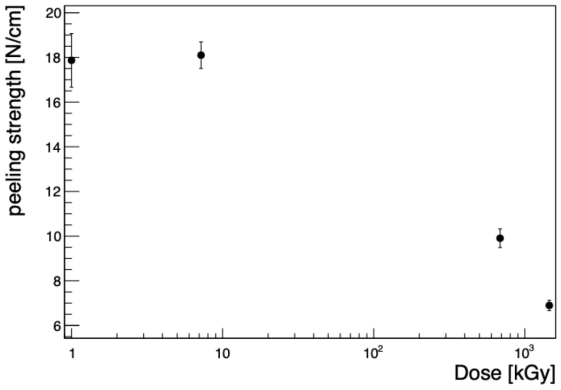


**Figure 14:** The peel strength measurement results of samples exposed to various radiation dose. The vertical axis is the peel strength in the unit of N/cm, while the horizontal axis is the radiation dose in the unit of kGy. The measurement of the sample with no radiation exposure is plotted at 1 kGy on purpose.

## 5.2. Conversion Cable

A material "fluorinated resin" used as a dielectric insulator for the $\mu$-coax cable [21] is reported to be weak against radiation [23] compared to popular dielectric insulator materials like the polyimide or the LCP. The estimated equivalent neurons at the location of conversion cables to be installed is $0.15 \times 10^{12}$ for the three years of sPHENIX operation.

In order to address the radiation hardness of the $\mu$-coax harness against three years of sPHENIX operation period, the effect of radiation was studied at RIKEN Accelerator-driven compact neutron systems facility (RANS), Japan. Three samples of harness bundle were exposed to the RANS neutron beam of energy up to 5 MeV. Each sample were exposed to 1.3, 2.6, and $4.0 \times 10^{12}$ equivalent neutrons, respectively. They are factor of 9, 17, and 27 more than estimated radiation dose for the INTT operation in sPHENIX. The signal transmission performances were compared before and after the irradiation to evaluate the radiation effect since it is not trivial for the conversion cable to measure the mechanical performance unlike the BEX case. The comparisons were made for the S-parameters, the eye diagrams, and the TDR. Any degradation was observed for all samples in any of these measurements regardless of the exposed radiation dose thus we concluded the radiation hardness of the conversion cable is durable for the INTT operation as well.

## 5.3. ROC

The radiation dose of the ROC boards throughout five years of operation of the FVTX detector in the PHENIX is

estimated to be approximately 300 Gy, while corresponding radiation dose for three years of the INTT operation in sPHENIX is estimated to be approximately 50 Gy. The dose for the INTT is moderate owing to relatively further distance of the ROC position from the collision point compared to that of FVTX's. Here the radiation hardness of the ROC board with respect to the total dose of 350 Gy is evaluated.

The ROC board is designed to be radiation hard and in fact it utilizes the FLASH-based ACTEL ProASIC3E FPGAs [7] which is known to be radiation hard. The optical data transmission system of the ROC board comprises the model TLK2711 (Texas Instruments) as the serializer/deserializer of data. There is a study of the radiation tolerance of the TLK2711 [24]. In this study, the increase of a leakage current and the bit error rate was monitored as a function of the radiation dose. It is reported the first bit error appeared $280 \sim 420$ Gy and the TLK2711 encountered functional failure as low as 700 Gy depending on the beam condition of the radiation exposure, f.i. high (low) intensity and short (long) duration. While the leakage current stays the same up to 400 Gy, rather rapid increase of the current was observed beyond that point.

According to the above study, the condition of the TLK2711 are already in the range that some bit error symptom may start after the FVTX use. It is rather preferable to replace them all before the reuse for the INTT though, the model was discontinued. Turned out only limited quantities were available in the market, which is insufficient to replace them all unfortunately. Hence the replacement candidates are prioritized and limited to the only ones which already have the symptom. The ROCs are installed only ones which passed the various function tests including no bit error symptoms.

## 6. Summary

A new silicon strip detector was developed for the sPHENIX experiment at RHIC. The silicon ladder consisted of silicon strip sensors, FPHX chips, HDIs, and the high thermally conductive carbon fiber stave. The ladder was designed to be as thin as $X/X_0 = 1.19$ %. The bus extender and the conversion cables were developed to transmit signals from the ladder to the ROC board. The 1.11 m long bus extender cable employs the novel low attenuation LCP as the dielectric material of the FPC. The conversion cable employs $\mu$-coaxial harnesses to secure flexibility in three dimensions in order to connect the bus extender end to the input/output ports of the ROC board without introducing any stress at the connection.

The result of the study indicated that the both bus extender and the conversion cables are sufficiently radiation hard against estimated radiation dose for three years of the INTT operation in the sPHENIX experiment. On the other hand, the exposed dose for TLK2711 chips of the ROC board throughout five years of the FVTX operation in the PHENIX experiment is in the level of some bit error starts to appear. These chips already show the symptom are replaced with new ones before reuse. Since the ROCs are installed relatively far away from the collision point for the INTT operation, the radiation dose for the ROC boards in the three years of INTT operation in the sPHENIX is estimated to be relatively moderate, i.e. 1/6 of that of the the FVTX.

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