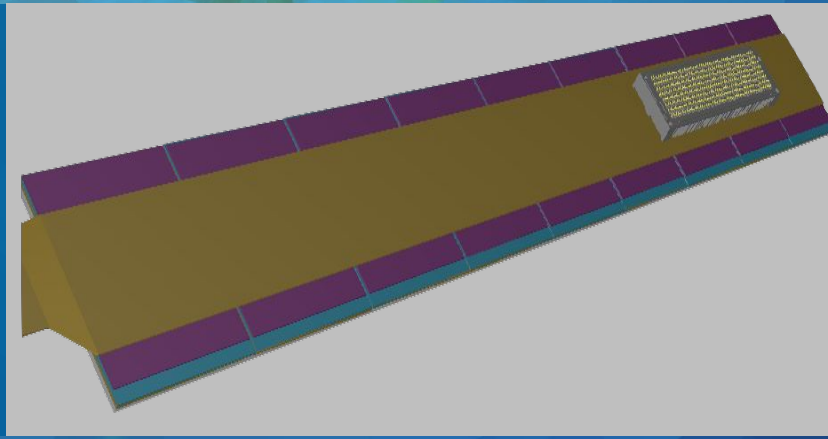
The ePIC Barrel Imaging Calorimeter

AstroPix Wafer QC, Modules and Staves



Manoj Jadhav
Argonne National Laboratory

BIC General Meeting
February 14, 2025

News

Wafer QC and Module/Stave meetings

- Kick-off meeting was held on February 3rd
- Alternatively on each Monday at 4 pm CT

AstroPix v5 Submission

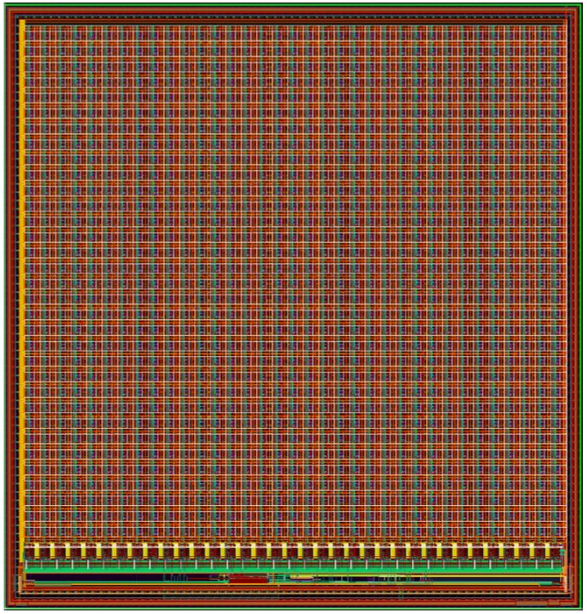
- v5 design is reviewed and ready fro fabrication
- Argonne procurement working on P.O.

Module and Stave test articles to be fabricated at Argonne

AstroPix v5

A low-power HV-CMOS monolithic active pixel sensor

- AMS ah18 180nm process
- 18610 um x 19485 um similar to AstroPix3
- Individual hitbuffers for 36 x 34 pixels
- NMOS comparator
- New guardring structure - smaller dead area, improved breakdown
- Total: ~2 mW/cm^2
- 2 Wafer resistivities: 200 – 400 and 600 – 2kOhm-cm Cz
- Integrated regulated charge pump (1.8 V – 2.6 V)
- Columns:
  - 32 Columns with Standard NMOS Comparator
  - 2 Columns with dynamic Feedback
  - 1 Column with NMOS Comparator and Resistor Load
  - 1 Column with NMOS Comparator and PMOS Load

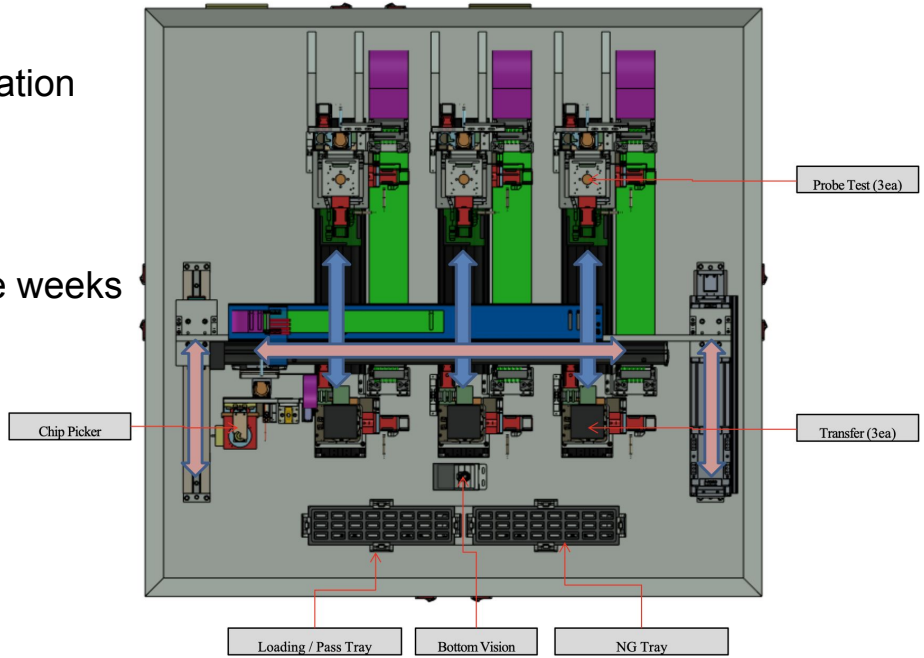


Chip expected ~July 2025

AstroPix wafer/chip QC

Chip QC preparation

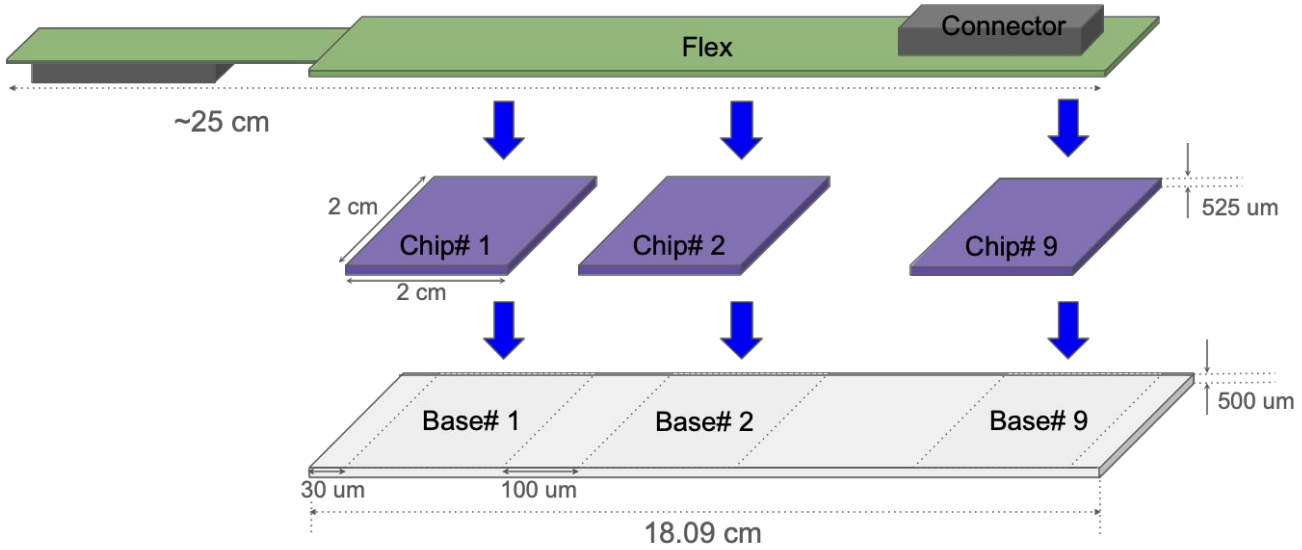
- Ongoing discussion with different companies for wafer probing (experience with ALICE ITS3)
- Design is ready for parallel chip probing
  - PNU is in discussion with vender for fabrication
- Help decide - Chip probing vs. wafer probing
- PNU has received one AstroPix v3 wafer
- Will receive 10 AstroPix v3 single chips in couple weeks
- Next step - decide on QC tasks list



AstroPix Module

Module design

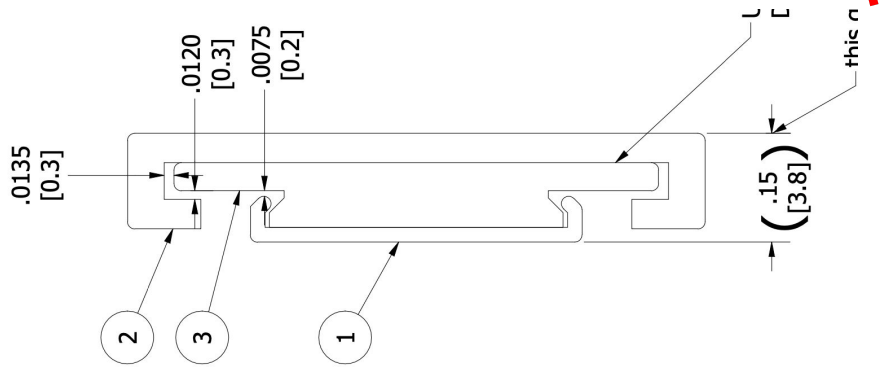
- AstroPix Module comprises of 3 layers/components
  - **Base Plate (Aluminum)**
  - **Nine AstroPix Chips**
  - **Flex PCB**
- **Failsafe design** - easy to rework on Stave

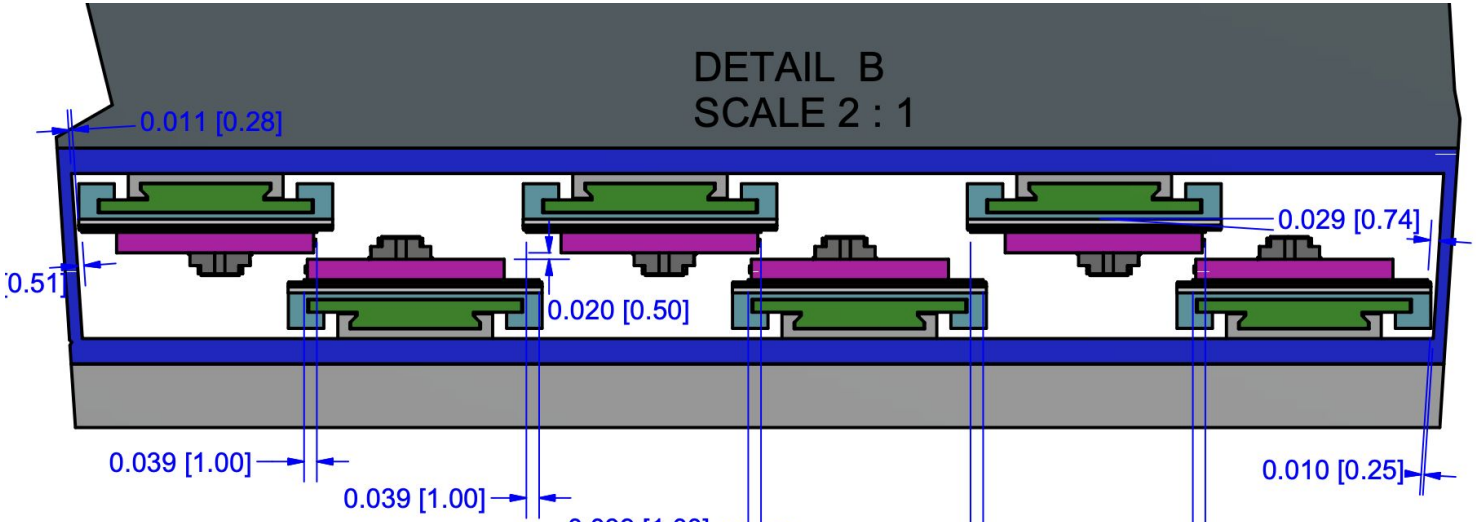


AstroPix Module/Stave

Mechanical Test Articles

- CAD drawings of Module/Stave test articles
- Timeline to receive test articles 8-10 weeks
- Help understand and improve loading procedure and design barriers
- Modules will be inserted alternatively upside down

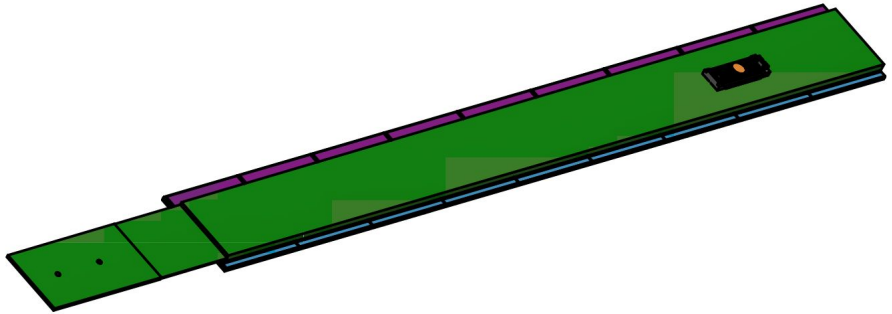




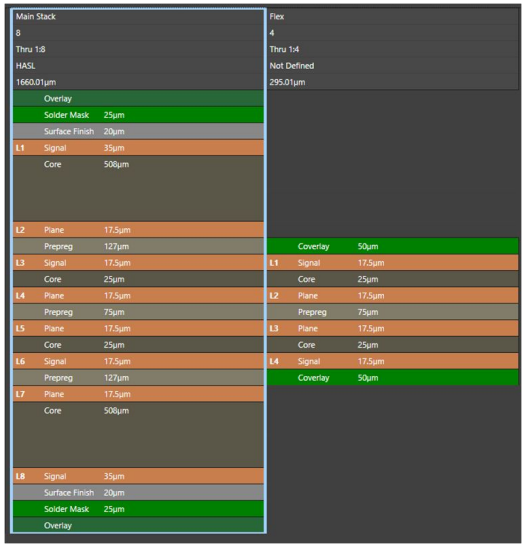
AstroPix Modules

AstroLinx

- OSU working on Flex-Rigid PCB
- PCB thickness ~1.66 mm
- Fits fine within the Imaging envelope in Sectors
- Tests with spare PCB to check if there is any wirebonding issues



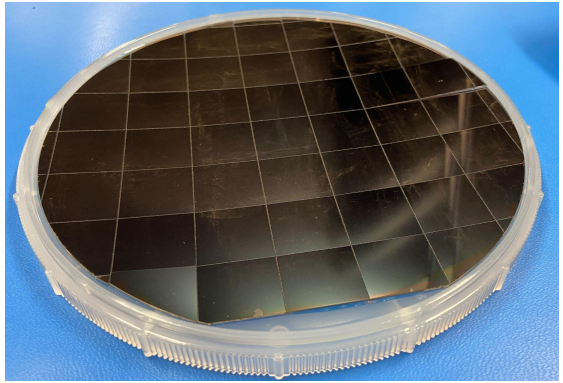
Current Stackup

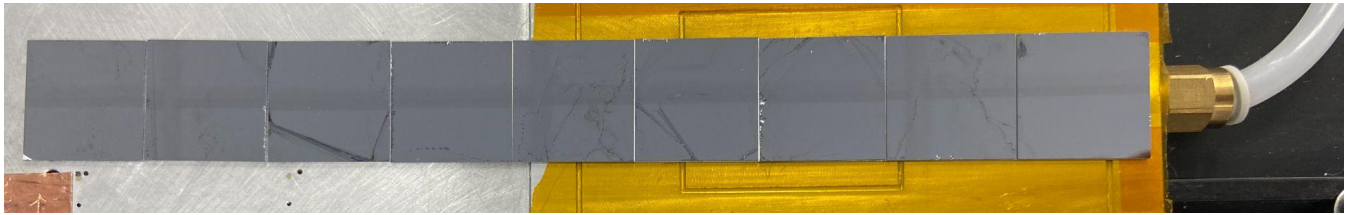


AstroPix Modules

Loading procedure

- Argonne and UCSC working on loading procedure with dummy chips and 0.5mm Al base plates
- UCSC received 2 Al base plates, 2 PCBs, 20 dummy chips and 20 AstroPix v3 chips
- Argonne showed initial mockup with dummy chips during last review
- UCSC working on prototype tool set including vacuum alignment tray/holder and a pickup tool
- UCSC will be procuring glass dummies for assembly trials

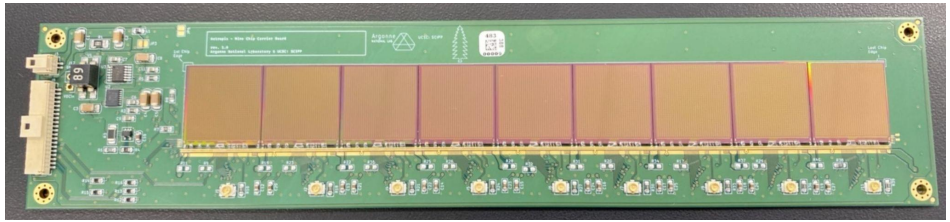


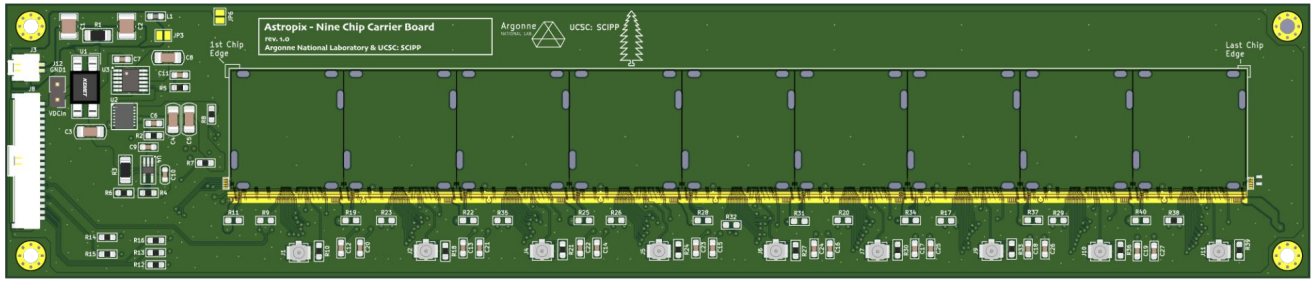


AstroPix Module Test Board

Test PCB board

- Will start testing PCB test board at Argonne
- Readout board **Daisy-chained 9 AstroPix chips**
  - Readout through SPI as well as Shift Registers (not on Module)
  - 2 LDOs (LT3041, LT3045 - radiation hard)
  - 20 Pin connector (Samtec T1M-20-F-SH-L) to plug into FPGA board (developed for Quadchip testing)
  - FW/SW available to test
  - One analog o/p available for each chip





Summary

- Biweekly follow up meetings for Astropix wafer QC and Module/Staves
- V5 design will be submitted soon for the fabrication
- Test articles for Module/Stave support will be submitted soon for fabrication
- Test PCB ready for electrical testing
- Ongoing work
    - Chip level QC test system - PNU
    - Module loading procedure - Argonne and UCSC
    - AstroLinx, a rigid+flex PCB - OSU

BACKUP

AstroPix Module

Mechanical design

- AstroPix Module comprises of 3 layers; **Base Plate, AstroPix Chips, and Flex PCB**
- AstroPix Chips will be glued to Aluminum plate using **thermally conductive adhesive** with good **electric insulation** (eg. DOW SE4445-CV, Stycast)
- **100 µm gap** between two AstroPix chips
- **Automatized chip placement and alignment** using pick-n-place machine (Gantry system)
- Flex PCB will be glued on top of chips (Araldite 2011)
- Electrical connection through wire bonds from AstroPix chip to Flex PCB - encapsulated using insulating epoxy/adhesive (eg. Dow Sylgard 186)