ALCOR interposer and FEB

Status of ALCOR-64 BGA package and FEB designs

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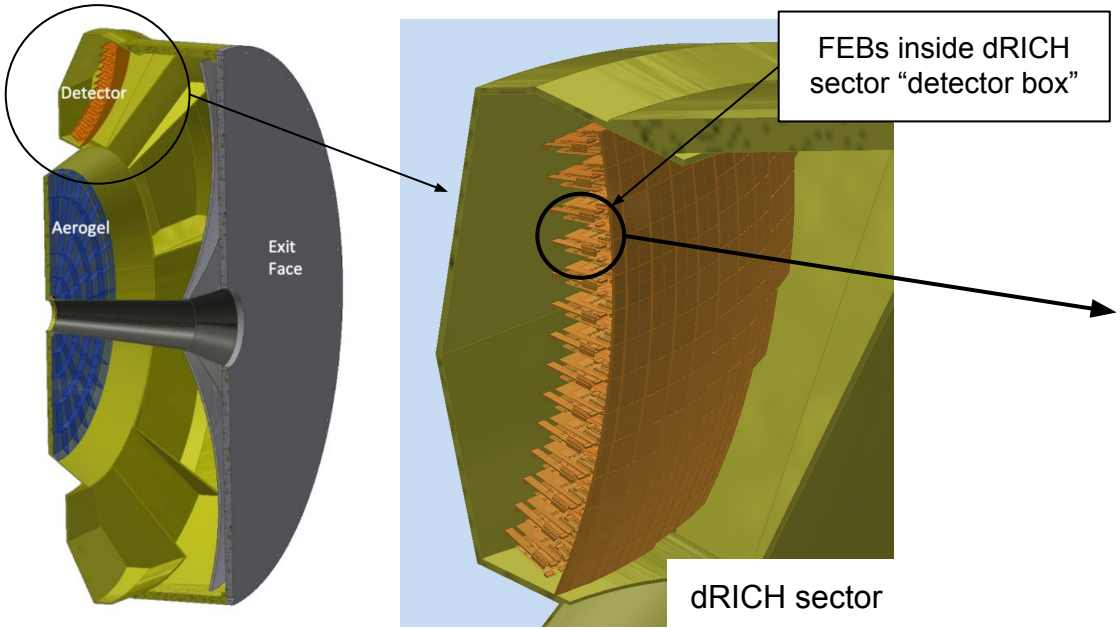
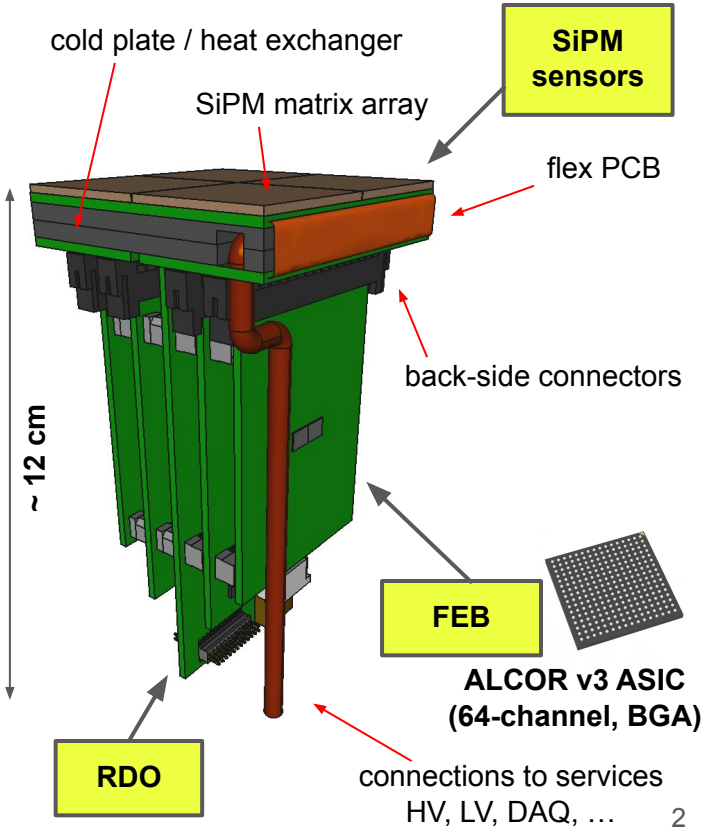
INFN Torino

dRICH Meeting - Sensors and Electronics
12.02.2025

ePIC dRICH electronics





- **1 PDU**: 4x64 SiPM array device (256 channels), **4 FEBs, 1 RDO**
- **1 ALCOR** (64 channels) per **FEB:** 8x8 SiPM matrix readout
- 1248 PDUs for full dRICH readout
- **4992 FEBs → 4992 ALCOR v3**
- **319488 readout channels**

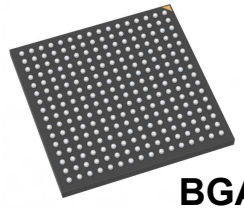
ALCOR BGA package

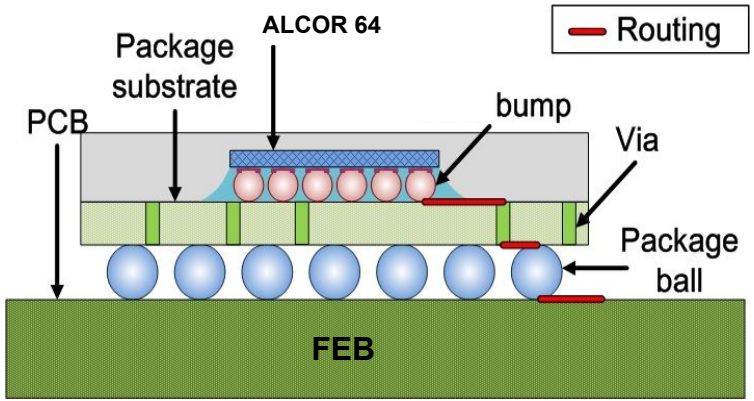
FC-BGA: flip-chip ball grid array

- Inside the package, the chip is flipped so that the active side of the device can be bump-bonded to the package substrate
- The whole bottom surface of the device can be used, not just the perimeter
- More interconnection pins wrt QFP or QFN
- Shorter interconnections reduce inductance, allow high-speed signals and carry heat better

256 balls BGA

- 1.0 mm ball pitch → 17x17 mm^2 package

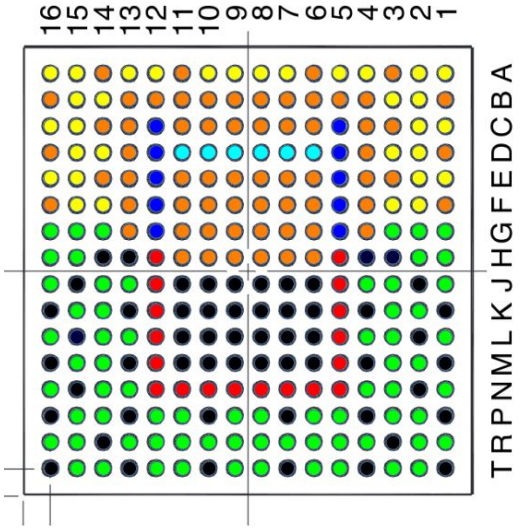


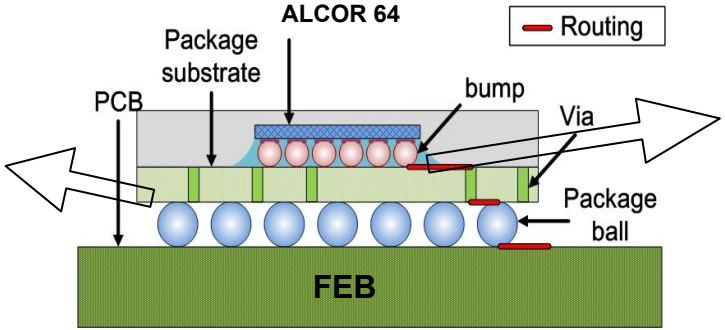


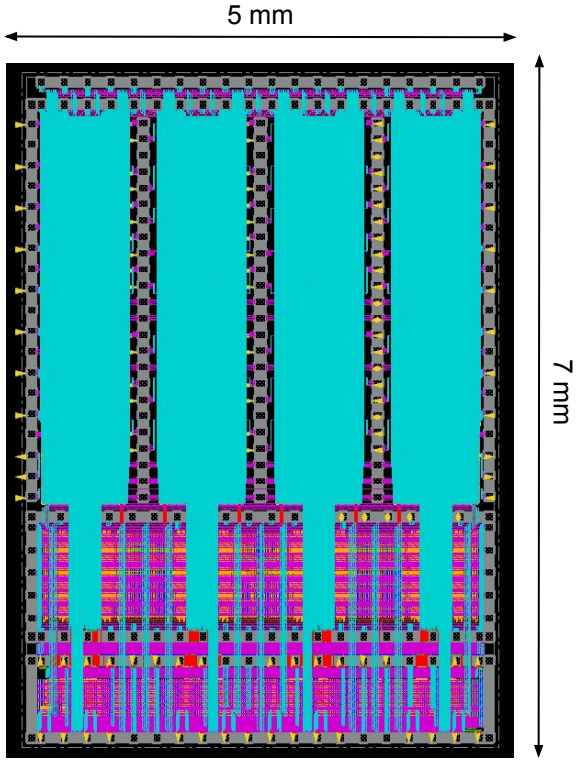
ALCOR BGA package

FC-BGA: flip-chip ball grid array

- BGA substrate designed by INFN Torino (M. Mignone)
- Substrate production, flip-chip assembly and packaging done by I-Tronics (https://www.itronics-sg.com/)



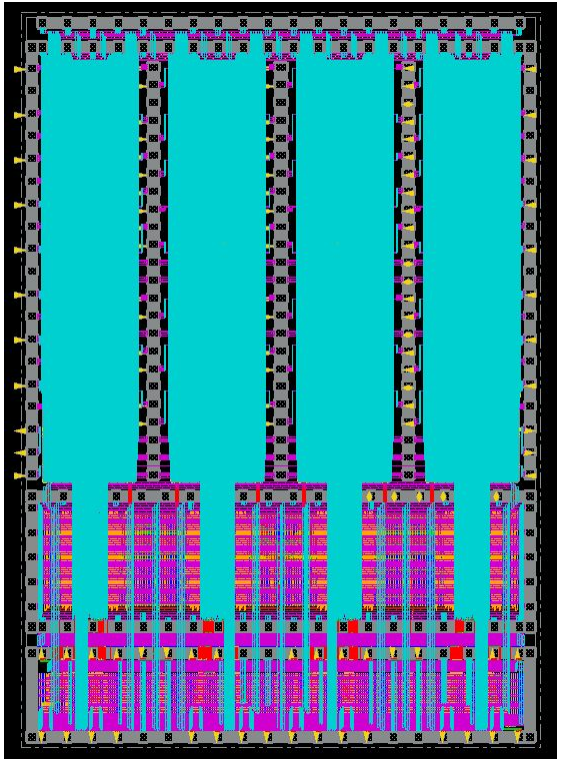




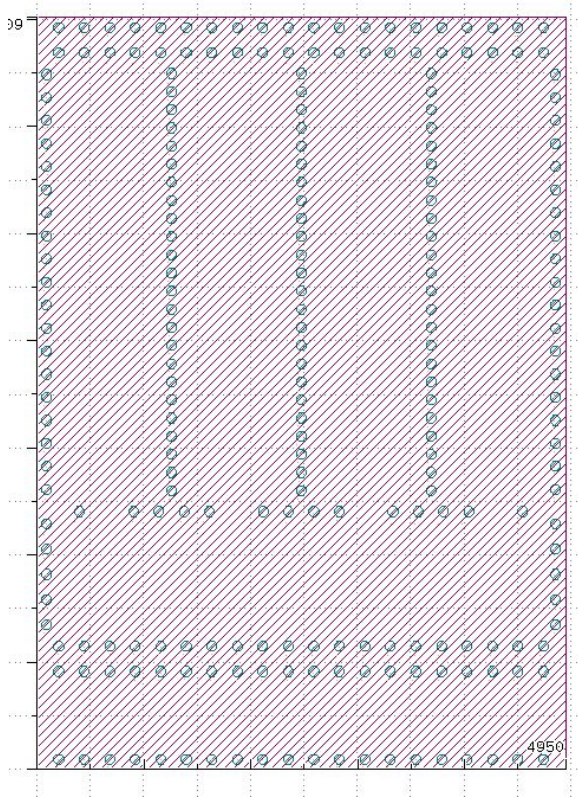
ALCOR v3

- ALCOR-64:
  - 7.02mm x 4.95mm
  - 234 PADs
- No redistribution layer (**RDL***) available in UMC 110nm technology
  - ASIC bump pads geometry not uniform
  - fan-out to BGA balls done on the interposer/substrate
- Bump pads pitch:
  - ~170 µm (analog inputs)
  - ~215 µm

ALCOR-64 top layout



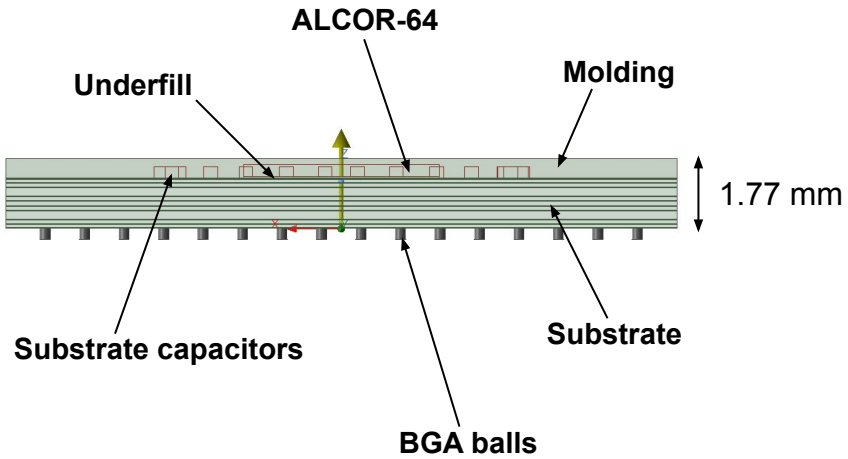
ALCOR-64 bump pads

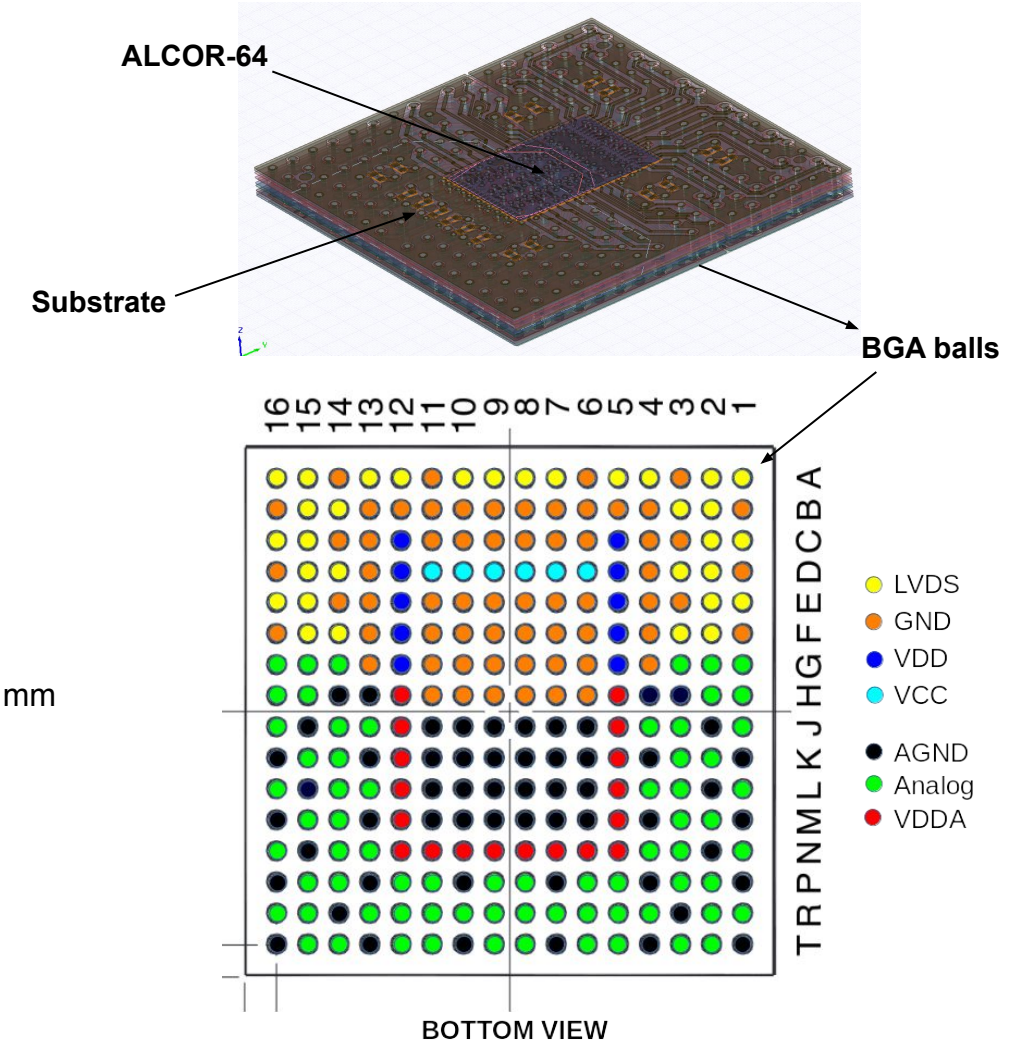


***RDL** (redistribution layer): special metal layer used to connect ASIC internal circuitry to its bump pads, which are then usually placed in a uniform grid pattern

ALCOR BGA package

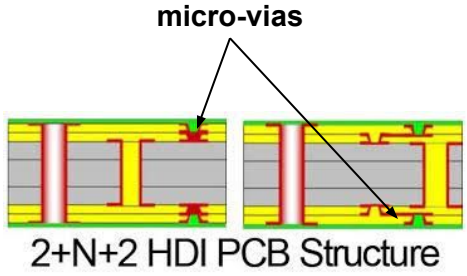
- BGA 256 (16 x 16)
- Size: 17 mm x 17 mm
- Ball pitch: 1 mm

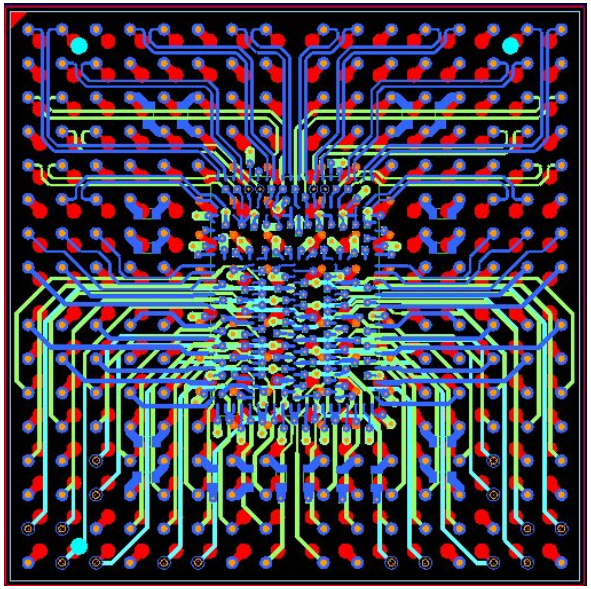


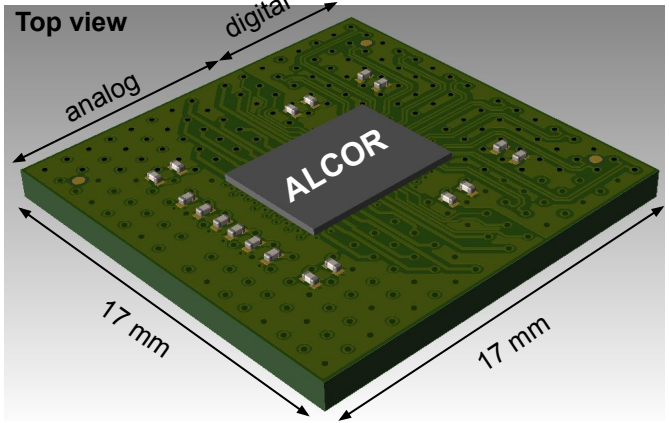


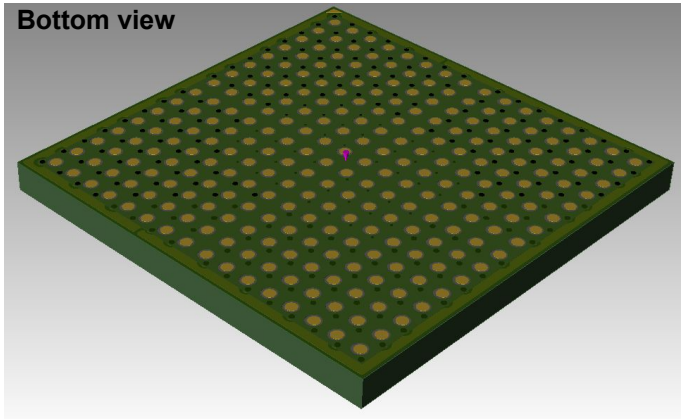
ALCOR-64 substrate

- BGA 256 Ball 17x17mm 1mm-pitch
- BT-Epoxy
- 10 Layers (2+N+2)
- Thickness: 1.27 mm
- Decoupling capacitors (0201)
- Design completed
- Verification ongoing: *signal* and *power integrity* simulations

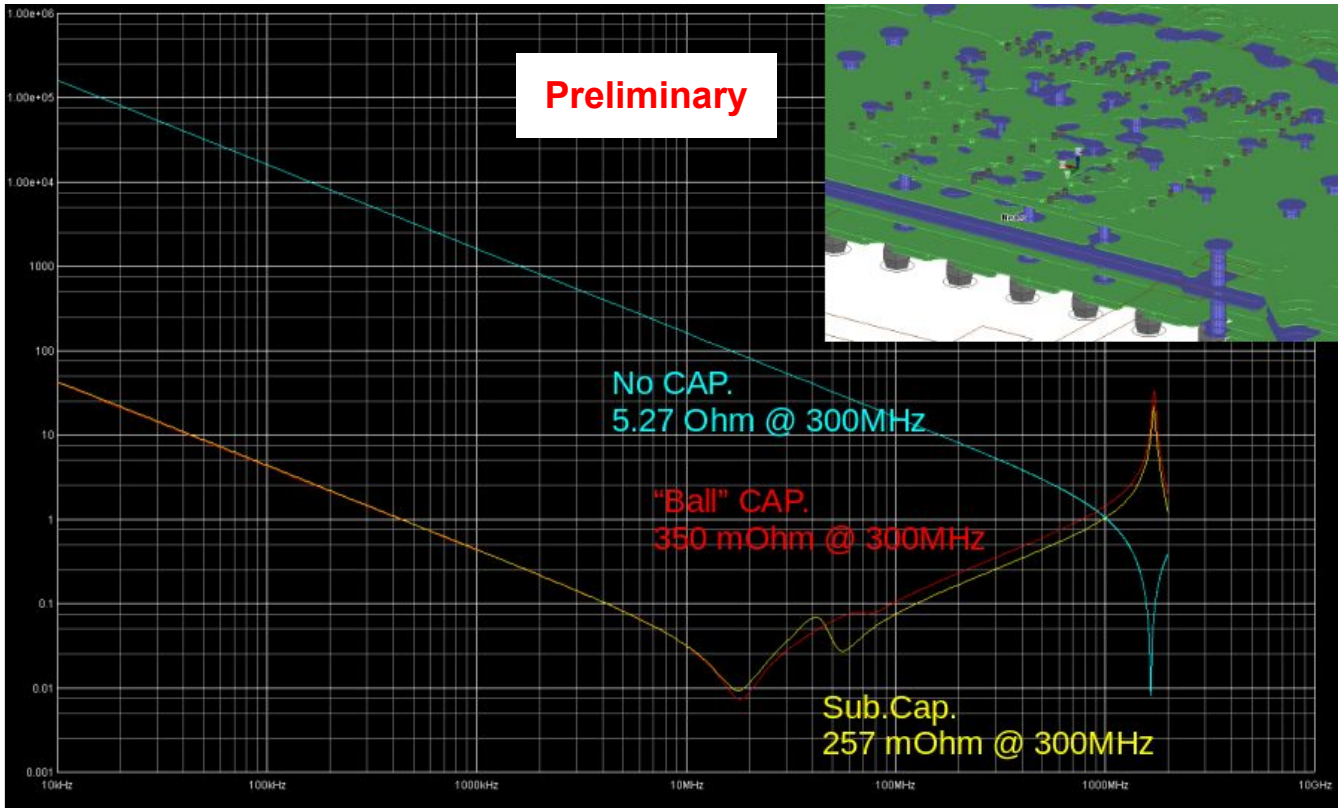








ALCOR-64 substrate - simulations (Ball+PCB+Bump)

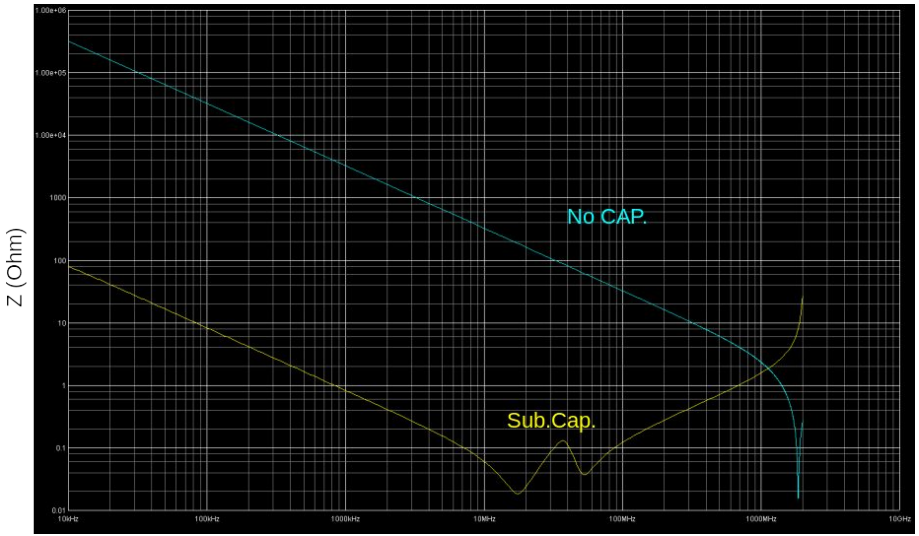


VDD-PDN (analog core supply power distribution network)

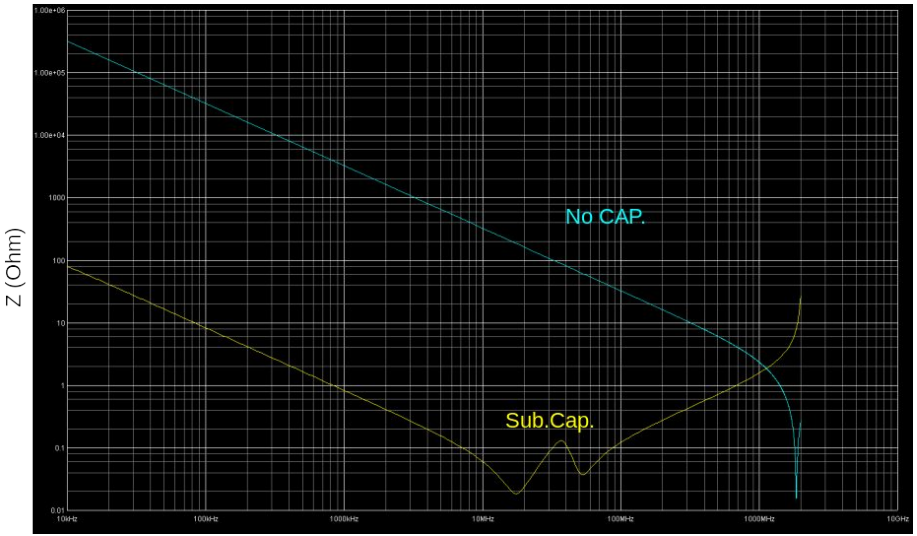
- **Sub.CAP**: substrate capacitors provides lower impedance
- **Ball CAP**: ideal case (not feasible)

Back-annotate this model into ALCOR simulations

ALCOR-64 substrate - simulations (Ball+PCB+Bump)



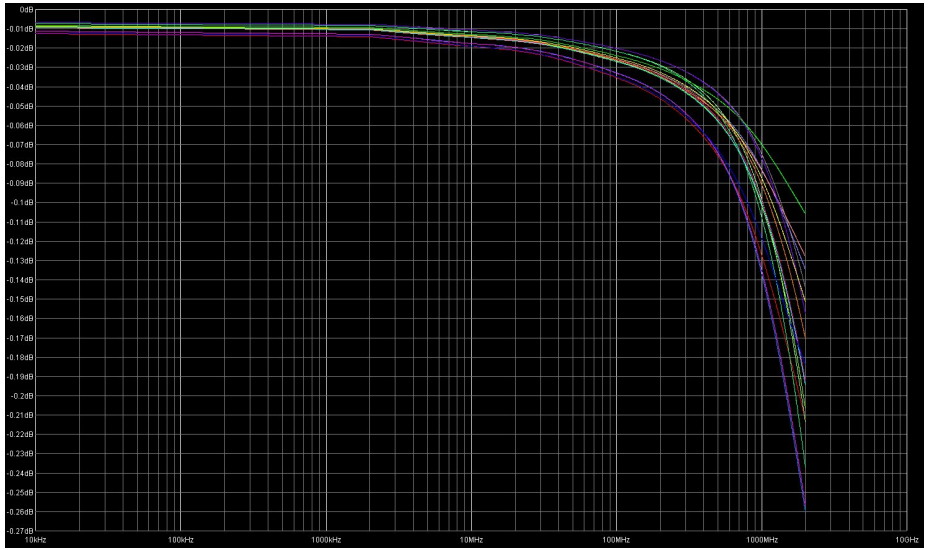
VDD-PDN (Digital core power supply)

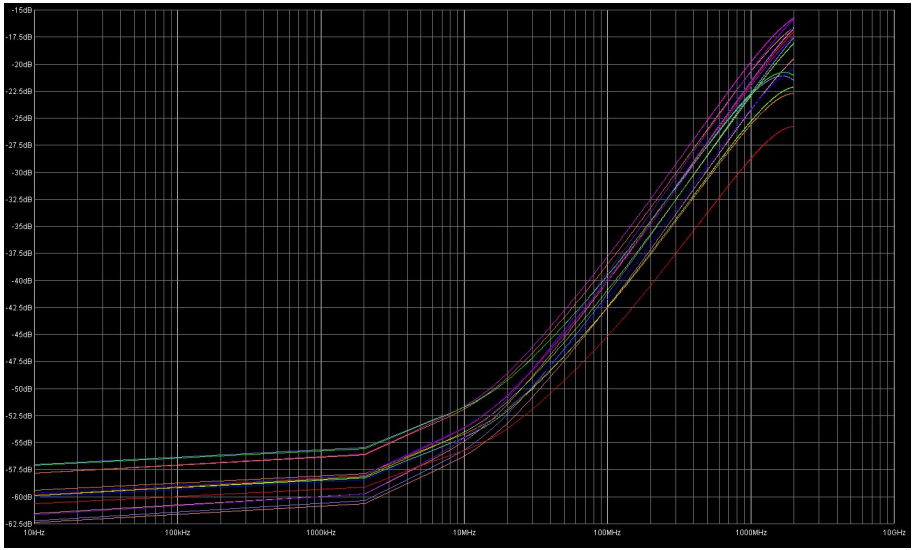


VCC-PDN (Digital IO power supply)

ALCOR-64 substrate - simulations (Ball+PCB+Bump)

Digital IO - LVDS transmission lines



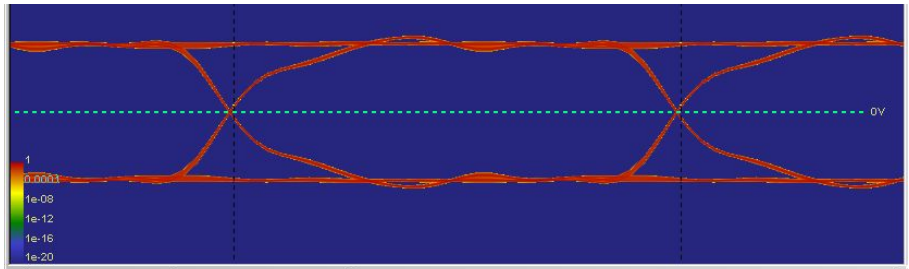


Insertion loss: amount of energy that a signal loses as it travels along the PCB trace

Return loss: loss of signal power due to signal reflection (impedance mismatch)

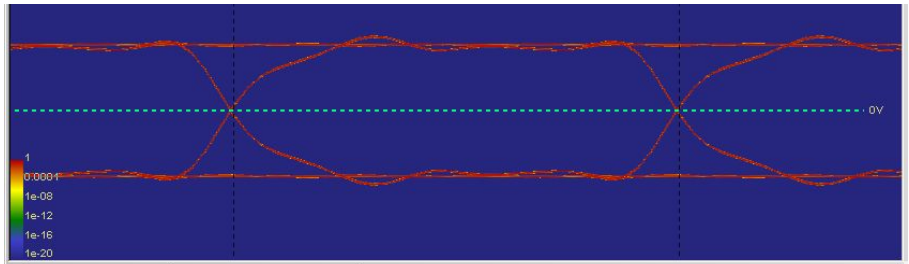
ALCOR-64 substrate - simulations (Ball+PCB+Bump)

Digital IO - LVDS transmission lines



Simulation date	Probe name	Simulation results					
		Highest BER	Pass/fail eye mask	Eye mask margin		Eye opening	
				Time, UI	Voltage, V	Time, UI	Voltage, V
Mon Sep 16 15:04:07 2024	U8.494P (at die)/U8.494N (at die)	0	Passed	0.187982	0.125092	0.987982	0.601042

ALCOR substrate=Ball+Via+Line+Bump
Q0-PRBS 19bit 800Mbps



Simulation date	Probe name	Simulation results					
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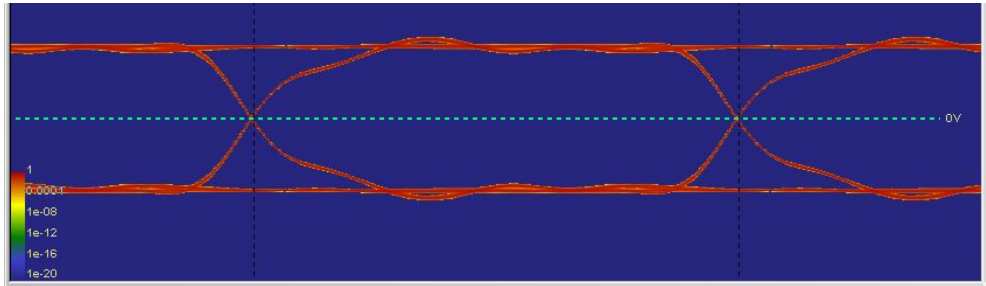
				Time, UI	Voltage, V	Time, UI	Voltage, V
Mon Sep 16 15:09:00 2024	U34.494P (at die)/U34.494N (at die)	0	Passed	0.187982	0.133418	0.987982	0.581125

“Ideal” TLINE
Q0-PRBS 19bit 800Mbps

Tx and Rx model used is
LVDS_2V5 Driver (Artix UltraScale+)

Q3-PRBS 19bit 800Mbps



Simulation date	Probe name	Simulation results					
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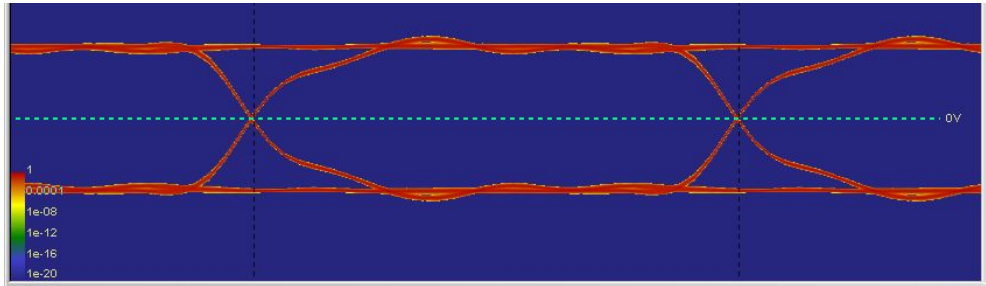
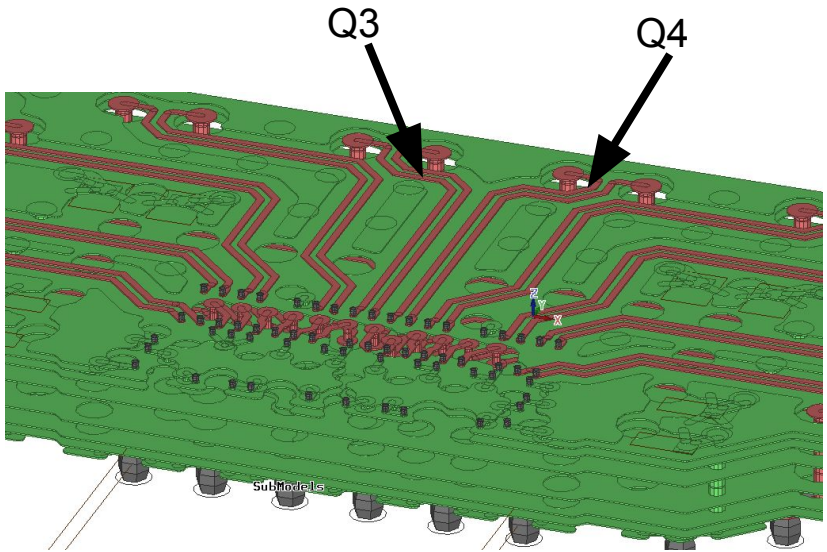
				Time, UI	Voltage, V	Time, UI	Voltage, V
Wed Sep 18 10:00:58 2024	U14.494P (at die)/U14.494N (at die)	0	Passed	0.187982	0.131482	0.987982	0.567655

Q3-PRBS 19bit 800Mbps
(+**Q4 “Aggressor” Crosstalk** PRBS 19bit 800 Mbps)



Simulation date	Probe name	Simulation results					
		Highest BER	Pass/fail eye mask	Eye mask margin		Eye opening	
				Time, UI	Voltage, V	Time, UI	Voltage, V
Wed Sep 18 10:06:52 2024	U14.494P (at die)/U14.494N (at die)	0	Passed	0.187982	0.129136	0.987982	0.562963

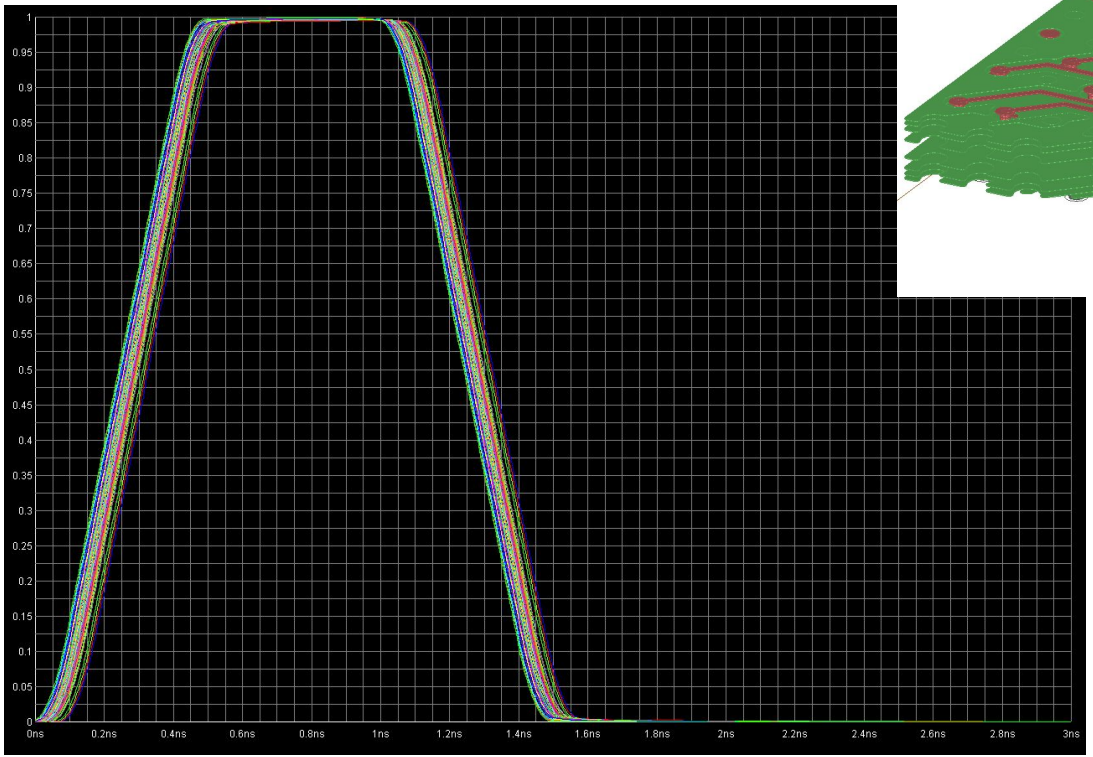
Crosstalk

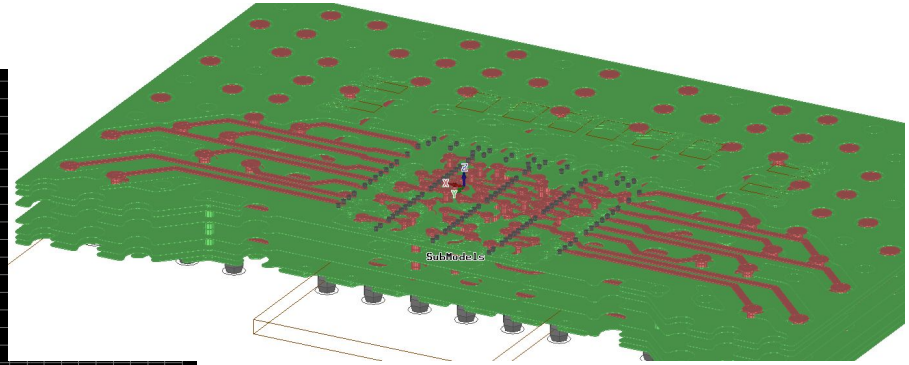


Tx and Rx model used is
LVDS_2V5 Driver (Artix UltraScale+)

ALCOR-64 substrate - simulations (Ball+PCB+Bump)

Analog inputs - 64 channels





Input waveform:

T_p = 1 ns

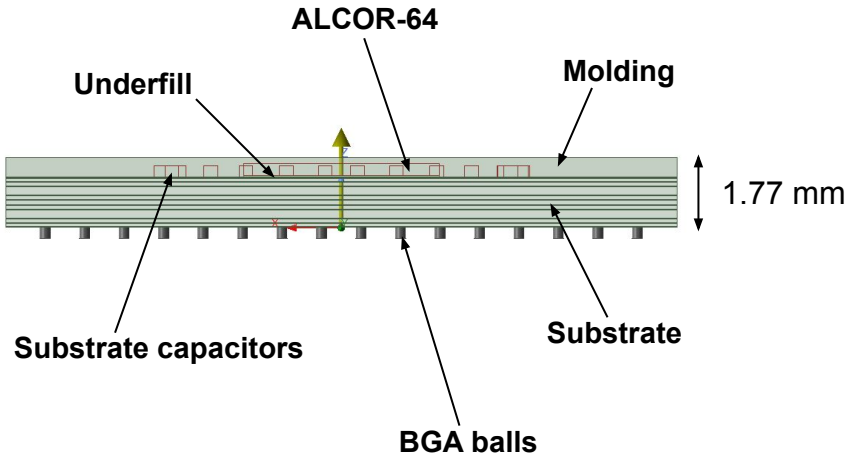
T_r = 400 ps

T_f = 400 ps

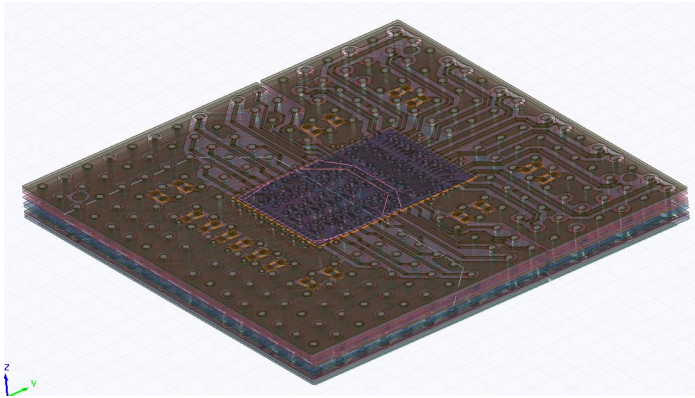
Z_O = 50 Ω

Z_L = 50 Ω

Package Thermal Resistance



- Molding 0.5 mm (0.16 mm above ASIC)
- ALCOR-64
- Underfill
- Substrate

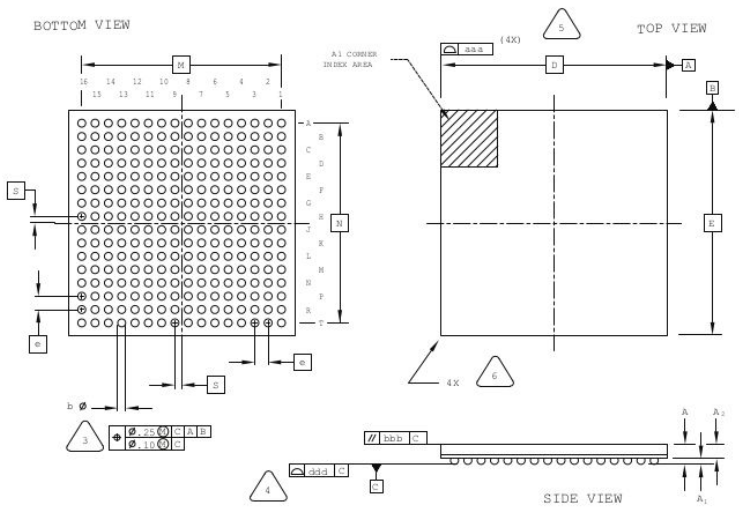


Underfill Thermal Conductivity	θ_{JC} (ASIC-case)	θ_{JB} (ASIC-board)
0.2 W/mK	3.45 °C/W	14.86 °C/W
0.8 W/mK	3.13 °C/W	11.01 °C/W

Commercial 256-ball BGA package datasheet

256-Ball ftBGA Package C

Dimensions in Millimeters



NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C
4. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

SYMBOL	MIN.	NOM.	MAX.
A	1.30	1.70	2.10
A1	0.30	0.50	0.70
A2		1.40 REF	
D/E		17.0 BSC	
M/N		15.0 BSC	
S		0.50 BSC	
b	0.50	0.60	0.70
e		1.0 BSC	
aaa	-	-	0.20
bbb	-	-	0.25
ddd	-	-	0.20

Geometry very similar to ALCOR BGA

Table 2. Device/Package Thermal Resistance[1]

Family	Device	Package	Dimensions	Pin Count	θ_{JA} (0lfm) °C/W	θ_{JA} (200lfm) °C/W	θ_{JA} (500lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LatticeECP2M™	LFE2M20E	FPBGA	17 x 17 mm	256	24.2	20.2	17.8	12.6	3.2
	LFE2M20E	FPBGA	23 x 23 mm	484	18.1	15.6	13.8	9.5	5.1
	LFE2M35E	FPBGA	17 x 17 mm	256	22.4	18.5	16.2	11.0	2.5
	LFE2M35E	FPBGA	23 x 23 mm	484	16.8	14.3	12.5	8.1	4.0
	LFE2M35E	FPBGA	27 x 27 mm	672	15.5	13.0	11.1	5.9	3.1
	LFE2M50E	FPBGA	23 x 23 mm	484	15.6	13.1	11.3	6.9	3.1
	LFE2M50E	FPBGA	27 x 27 mm	672	14.2	11.9	10.2	5.9	2.6
	LFE2M50E	FPBGA	31 x 31 mm	900	12.5	10.4	9.1	6.1	1.9
	LFE2M70E	FPBGA	31 x 31 mm	900	11.7	9.5	8.1	5.3	1.5
	LFE2M70E	FPBGA	35 x 35 mm	1152	13.7	12.0	11.0	6.5	2.0
	LFE2M100E	FPBGA	31 x 31 mm	900	10.8	8.6	7.1	4.5	1.2
	LFE2M100E	FPBGA	35 x 35 mm	1152	13.2	11.2	9.8	5.7	1.5
LatticeECP3™	LFE3-17	FTBGA	17 x 17 mm	256	24.5	20.6	18.2	12.9	3.3
	LFE3-17	CSBGA	10 x 10 mm	328	30.8	27.8	25.5	12.5	6.1
	LFE3-17	FPBGA	23 x 23 mm	484	18.4	15.8	14.1	9.8	5.4
	LFE3-35	FTBGA	17 x 17 mm	256	24.5	20.6	18.2	12.9	3.3
	LFE3-35	FPBGA	23 x 23 mm	484	18.4	15.8	14.1	9.8	5.4
	LFE3-35	FPBGA	27 x 27 mm	672	17.1	14.7	12.7	9.5	4.5
	LFE3-70	FPBGA	23 x 23 mm	484	15.7	13.2	11.4	7	3.2
	LFE3-70	FPBGA	27 x 27 mm	672	14.3	12	10.3	6	2.7
	LFE3-70	FPBGA	35 x 35 mm	1156	12.9	11.5	10.6	7.3	2.3

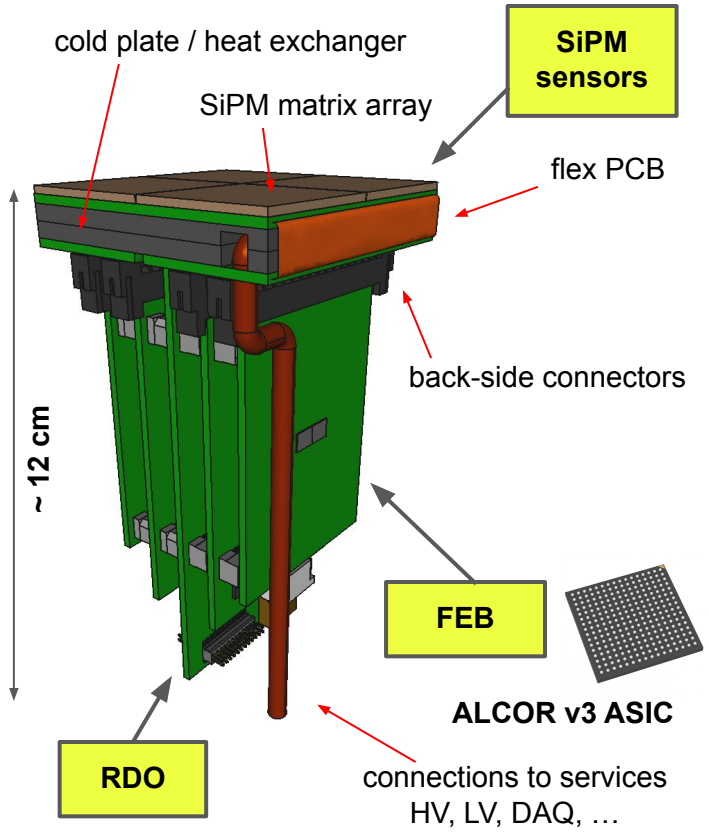
Package Thermal Resistance

- θ_{JB} = 12.9 °C/W (Junction-to-Board)
- θ_{JC} = 3.3 °C/W (Junction-to-Case)

Results from our simulations match quite well specs from commercial BGA

dRICH ALCOR FEB

- 4 FEBs in each PDU (256 readout channels)
- Functionalities defined, components selected, schematic design done
- 2 slightly different FEB versions, they share the ALCOR BUS connector (interface with RDO):
  - *Master*: internal FEB
  - *Slave*: external FEB
- Layout ongoing: many constraints already finalized to match RDO and ALCOR designs, PCB traces routing ongoing



PDU

Designed by **INFN Torino** (M. Mignone), close cooperation with **Bologna-Ferrara** colleagues for RDO design, SiPMs requirements and space constraints

dRICH ALCOR FEB

- **ALCOR v3**: 64-channel, BGA package
- **ALCOR BUS connector**: interface between RDO and 4 FEB
- **SiPM connector**: interface between ALCOR inputs and SiPM
- **Service connector**: provides LV (for ALCOR) and HV (for SiPM)
- Dedicated PCB section for SiPMs **HV routing**: 2 V_{bias} channels, to be used also for **SiPM annealing** (forward-bias, T=150°C on SiPM matrix board, up to 3.2 A on each V_{bias} channel, 0.1 A for each SiPM)
- ALCOR **AC-coupling** circuitry + **annealing diodes**
- **Voltage regulators** with **current monitors** (managed by RDO via I2C expander)
- **NTC temperature sensor**