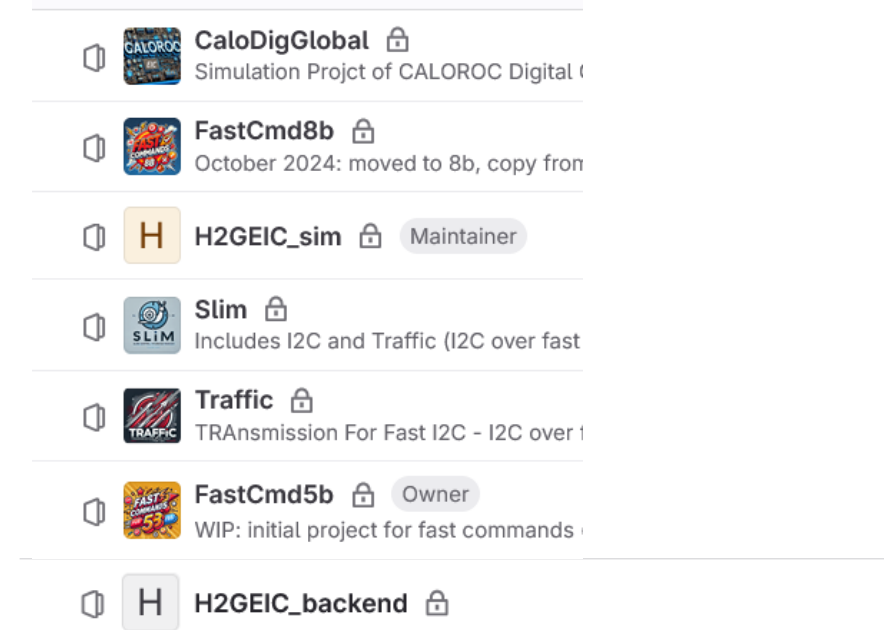
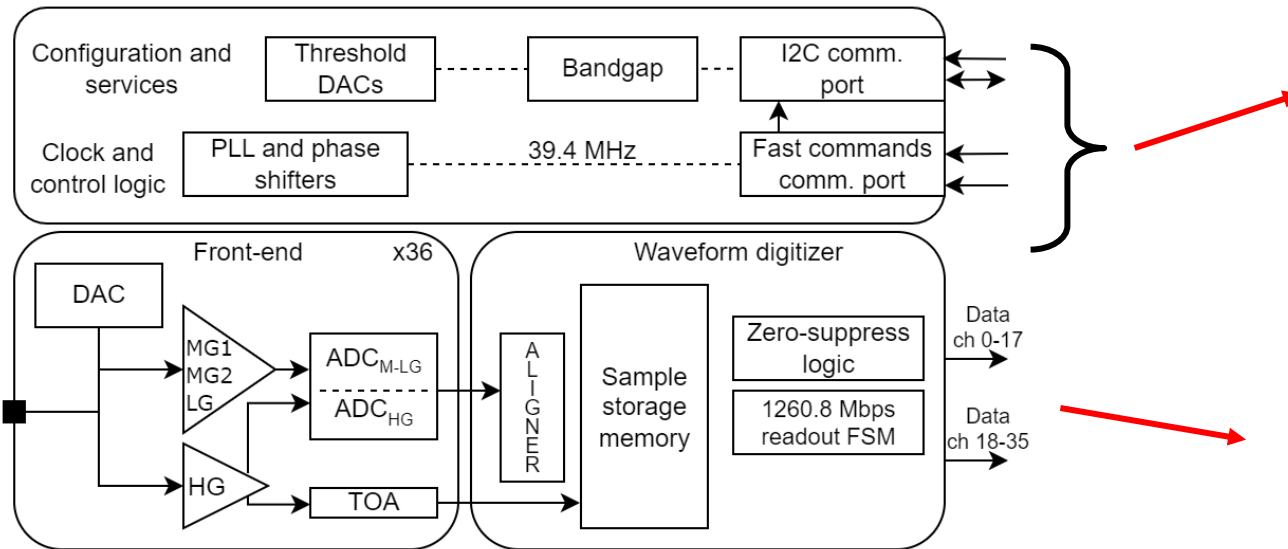


## CALOROC status

Feb 2025

Frederic DULUCQ – [fdulucq@in2p3.fr](mailto:fdulucq@in2p3.fr)  
Ecole Polytechnique – CNRS

- ❑ CALOROC project and submodules are available in GIT



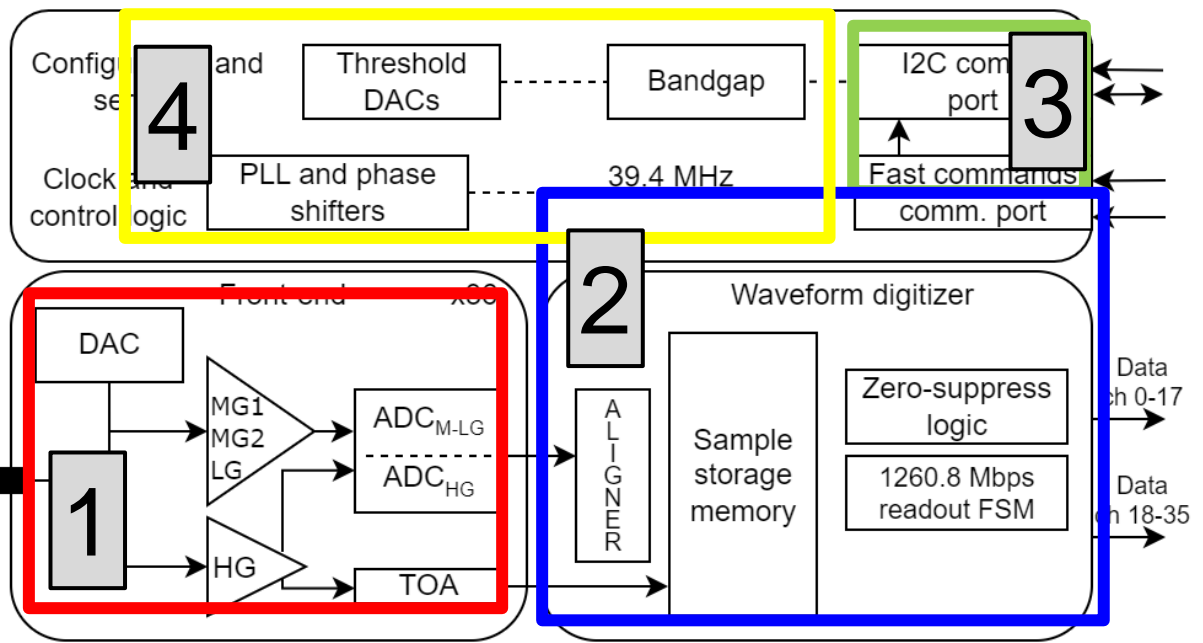
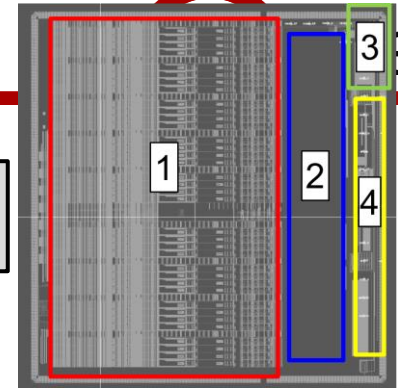
- ❑ Fast command (lpgbt compatible) added to project: Done
- ❑ Almost fully-assembled RTL verification: Done
- ❑ RTL (Verilog code) to schematic scripts finished : Done
- ❑ 3x “mini” design reviews: Done
  
- ❑ Waveform digitizer layout: Done (status changed)
- ❑ Analog + Digital assembly: WIP (status changed)
- ❑ Radiation SEE injection: Done (status changed)

# CALOROC development status – layout view

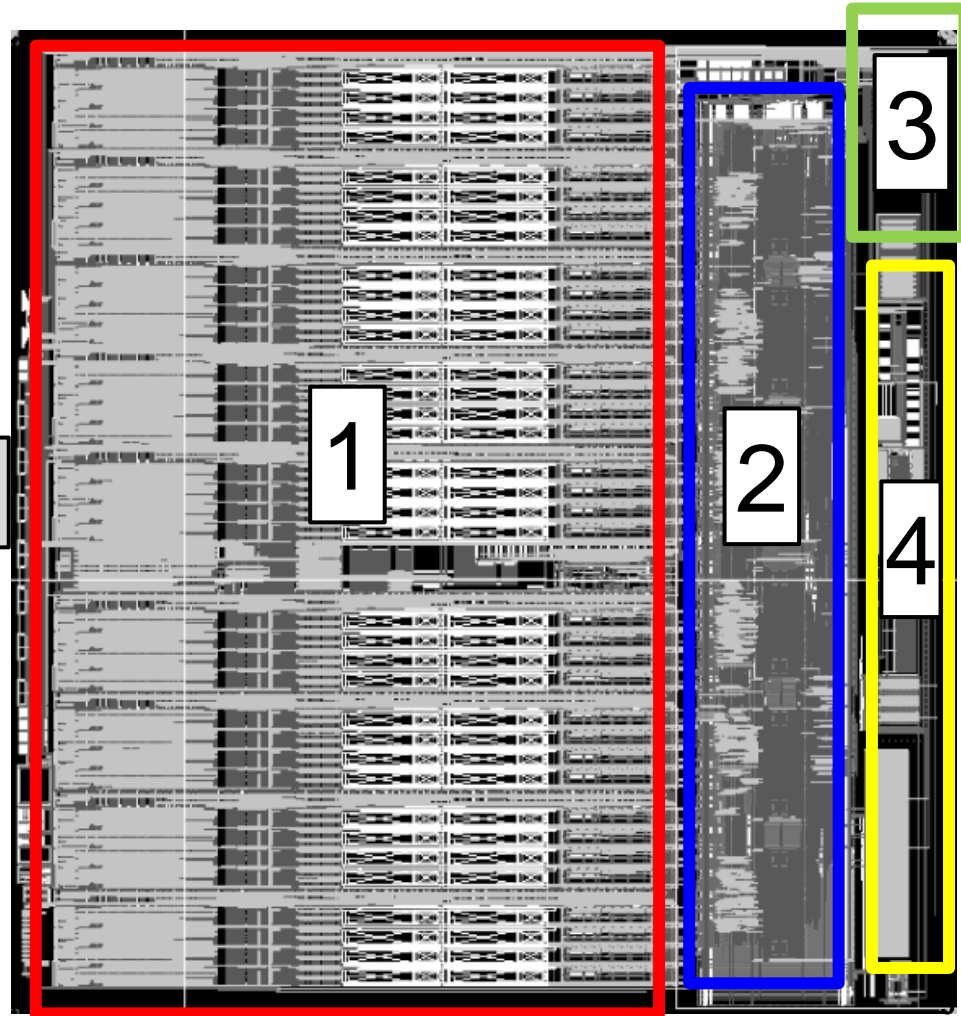
mega

- ❑ All the submodules are in place – no part missing
- ❑ All interconnections done
- ❑ Top level connection and verifications in progress

December 2024

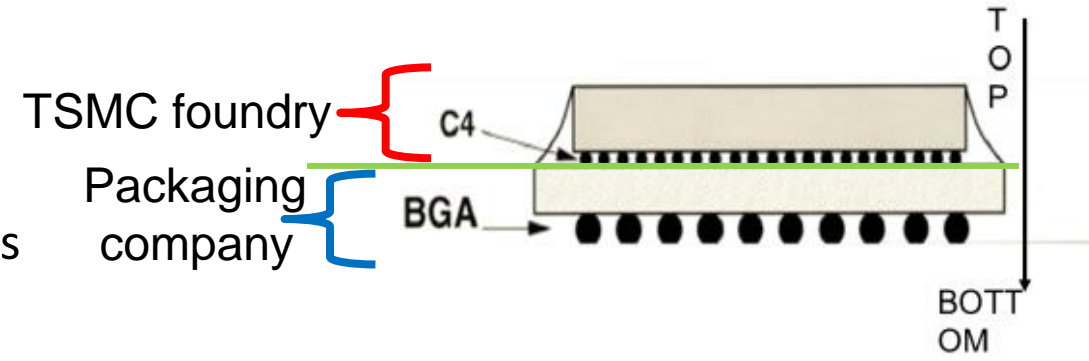


January 2025



Design of the CALOROC substrate started (for the packaging):

- Interposer between die and BGA



Design based on existing substrate with latest HGCROC changes

- BGA 17x17 mm 0,8 mm pitch (400 balls)
- Fabrication (12w) should match ASIC fabrication

Will be sent to fabrication company next week for feasibility (plus quote)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A		gnd_dac	gnd_pa	in<1>	in<0>	gnd_pa	gnd_sk	gnd_buf	vcm_adc	gnd_adc	gndd	gnd_tdc	gndd	vss	mode_UF	mode_SN	fcmd_p	clk320_p	soft_resetb		A
B	vss	vdd_dac	gnd_pa	in<3>	in<2>								vddd	vddd2	flag_AF	VH110	fcmd_n	clk320_n	hard_resetb	SDA	B
C	vdd_pad	gnd_dac	gnd_pa	in<5>	in<4>	vdd_pa	vdd_sk	vdd_buf	vref_adc	vdd_adc	vddd	vdd_tdc	gndd	vss	vss	vss	vss	vss	error	SCL	C
D	Vref_sk	vdd_dac	gnd_pa	in<7>	in<6>								vddd	vddd2	vddd2	vddd2	vddd2	vddd1	daq0_n	daq0_p	D
E	vdd_pad	gnd_dac	gnd_pa	in<9>	in<8>	gnd_pa	gnd_sk	gnd_buf	vcm_adc	gnd_adc	gndd	gnd_tdc	gndd	vss	vss	vss	vss	vss	gndd1	vddd1	E
F	Vref_noinv	vdd_dac	gnd_pa	in<11>	in<10>								vddd	vddd2	vddd2	vddd2	vddd2	vddd1	daq1_n	daq1_p	F
G	vdd_pad	gnd_dac	gnd_pa	in<13>	in<12>	vdd_pa	vdd_sk	vdd_buf	vref_adc	vdd_adc	vddd	vdd_tdc	gndd	vss	vss	vss	vss	vss	rstb_j2c	sipm_calib	G
H	Vref_inv	vdd_dac	gnd_pa	in<15>	in<14>								vddd	vddd2	vddd2	vddd2	vddd2	vddd1	efuse	strobe_ext	H
J	vss	gnd_dac	gnd_pa	in<17>	in<16>	gnd_pa	gnd_sk	gnd_buf	vcm_adc	gnd_adc	gndd	gnd_tdc	gndd	vss	vss	vss	vss	vss	gnd_pll	vdd_pll	J
K	Vref_toa	vdd_dac	gnd_pa	in<19>	in<18>								vddd	vddd2	vddd2	vddd2	vddd2	vddd1	gnd_pll	vdd_pll	K
L		gnd_dac	gnd_pa	gnd_pa	gnd_pa	vdd_pa	vdd_sk	vdd_buf	vref_adc	vdd_adc	vddd	vdd_tdc	vddd	vss	vss	vss	vss	vss	trig_n	trig_p	L
M	Vref_tot	gnd_dac	gnd_pa	in<21>	in<20>	gnd_pa	gnd_sk	gnd_buf	vcm_adc	gnd_adc	gndd	gnd_tdc	gndd	vss	vss	vss	vss	vss	gndd1	vdd_sc	M
N	vss	vdd_dac	gnd_pa	in<23>	in<22>								vddd	vddd2	vddd2	vddd2	vddd2	vddd1	daq2_n	daq2_p	N
P	vbg_lv	gnd_dac	gnd_pa	in<25>	in<24>	vdd_pa	vdd_sk	vdd_buf	vref_adc	vdd_adc	vddd	vdd_tdc	gndd	vss	vss	vss	vss	vss	gndd1	vddd1	P
R	vdd_pad	vdd_dac	gnd_pa	in<27>	in<26>								vddd	vddd2	vddd2	vddd2	vddd2	vddd1	daq3_n	daq3_p	R
T	probe_pa	gnd_dac	gnd_pa	in<29>	in<28>	gnd_pa	gnd_sk	gnd_buf	vcm_adc	gnd_adc	gndd	gnd_tdc	gndd	vss	vss	vss	vss	vss	add<3>	add<2>	T
U	vdd_pad	vdd_dac	gnd_pa	in<31>	in<30>								vddd	vddd2	vddd2	vddd2	vddd2	vddd1	add<1>	add<0>	U
V	ctest	gnd_dac	gnd_pa	in<33>	in<32>	vdd_pa	vdd_sk	vdd_buf	vref_adc	vdd_adc	vddd	vdd_tdc	gndd	vss	vss	vss	vss	vss	PLL_lock	vdd_sc	V
W	vdd_pad	vdd_dac	gnd_pa	in<35>	in<34>								vddd	vddd2	vddd2	vddd2	vddd2	VNEG	probe_toa	probe_tot	W
Y		gnd_dac	gnd_pa	gnd_pa	gnd_pa	gnd_pa	gnd_sk	gnd_buf	vcm_adc	gnd_adc	gndd	gnd_tdc	trig1_ext	trig2_ext	probe_noinv	VH110	probe_inv	probe_dc1	probe_dc2		Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

- ❑ Both CALOROC assembled, top routing (power) started
  - ❑ Latest step before metal filling and submission
  
- ❑ Substrate design will be sent to the packaging company (next week)
  - ❑ For a quote and feasibility
  
- ❑ Submission foreseen beginning of March... some issues need to be cleared before (WIP)

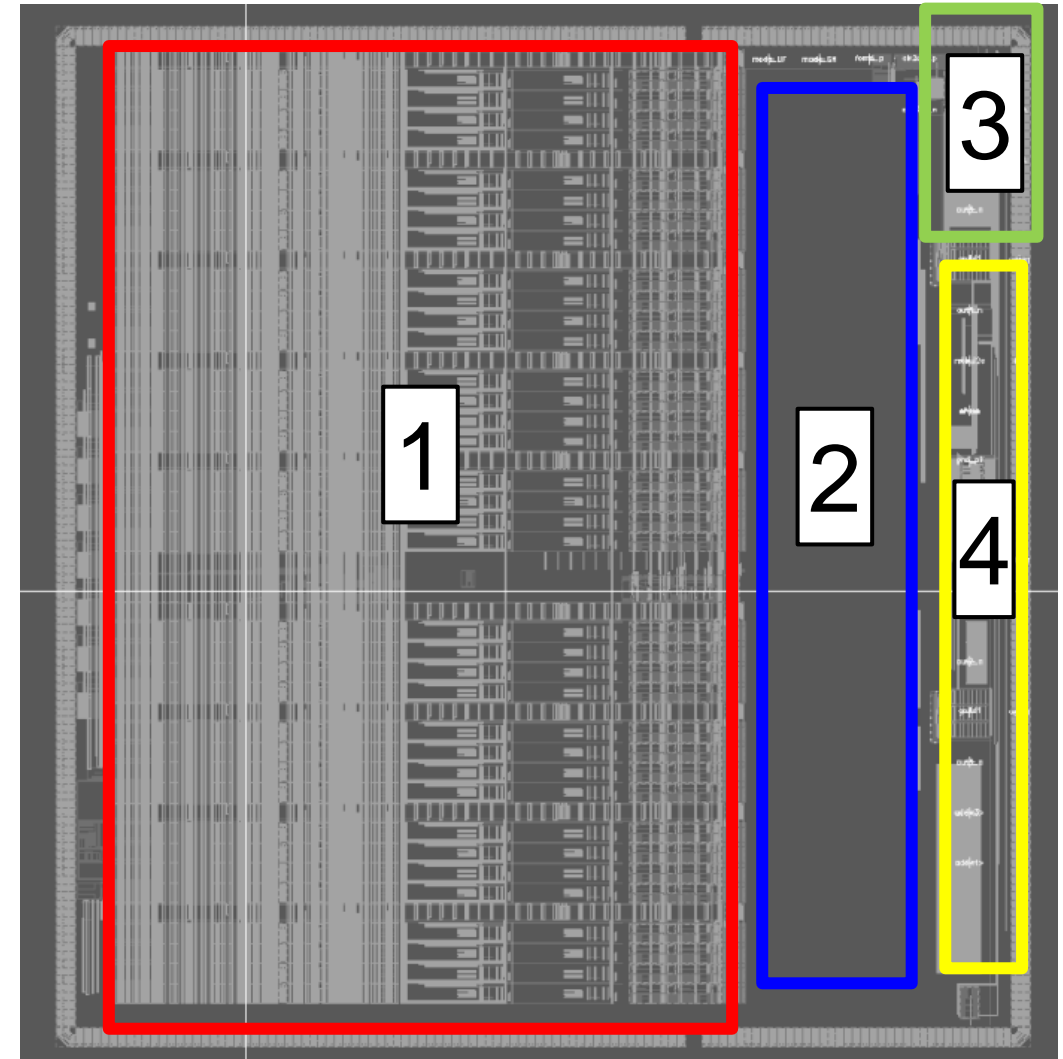
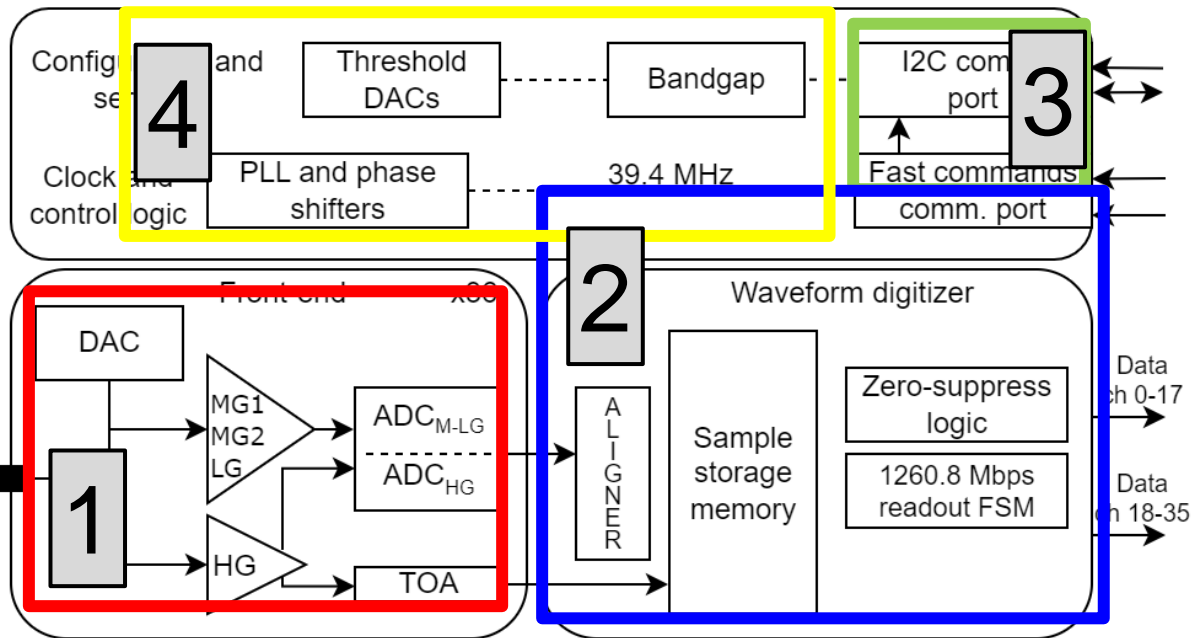


## Fast commands main characteristics:

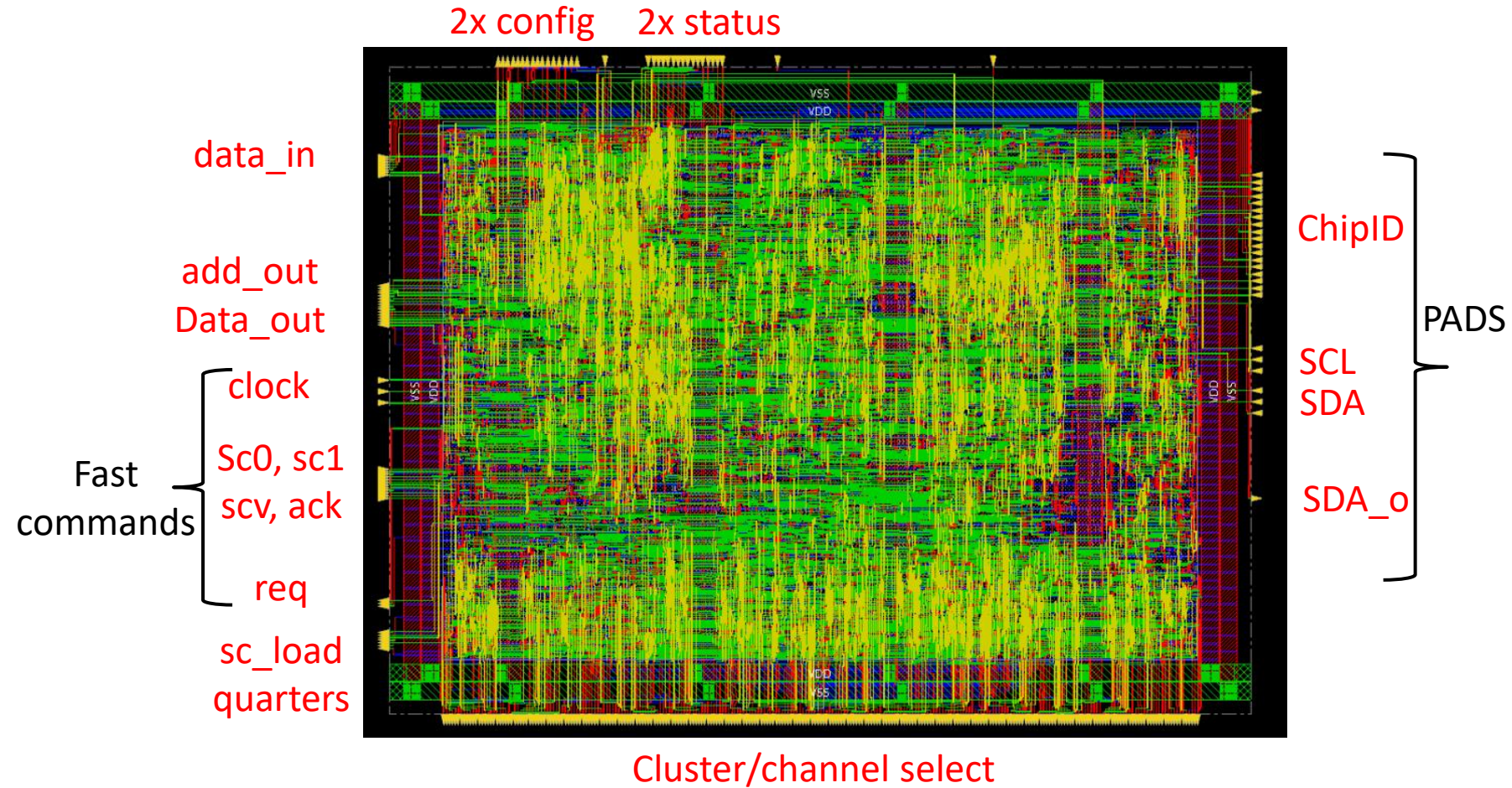
- 8 bits long (fast command “rate” of 39.4 MHz = internal clock of the ASIC)
- Main and only clock needed from the outside: 315.2 MHz
- Some new fast commands... to test I2C over fast commands (CALOROCB only)

Fast commands	Value	Description	Comment	Possible back to back
Idle	00110110	Default command inside	~99% of the time	Y
L1A	01001011	External trigger (all channels)	Calibration	Y
ChipSync	11010010	Reset FSM, buffers and counters		
BCR	00011101	Reset timestamp counter to a default value		
EBR	11010001	Empty readout buffers		
LinkResetROCD	10011010	Transmission of synchronization patterns	~ 400x same pattern	
ROC-Serializer-Reset	10011100	Reset serializer link module only		
CalPulseInt	00101101	800 ns internal calibration pulse		
CalPulseExt	01111000	100 ns external calibration pulse		
SC_0	01011010	Send bit 0 for SLIM	I2C over fast commands	Y
SC_1	01011100	Send bit 1 for SLIM	I2C over fast commands	Y
SC_Valid_Reset	10001011	Send validation to SLIM or a reset transaction (2 consecutives)	I2C over fast commands	Y

- ❑ Digital processing under layout (part 2) – only part missing
- ❑ SEE injection on part 4 (fast commands, I2C) in progress
- ❑ Others: finished waiting part 2 for final assembly



Size 400 x 300 um (part 3)



net	HK buffer	New buff	comments
Sc_load / wb_stb	D24	D16	Entire chip and 25ns pulse → max Dx but no D20 and D24
Decoder 11b	D16	D6	From Pedro, large line RC (1,5k, 1,2 pF) → D6-D16 small diff
Sc_data_out	D24	D8	Same
Sc_addr_out	D24	D8	Same