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# Status report of the eRD109 project on SALSA chip development

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# SALSA CHIP TARGET SPECIFICATIONS

## Versatile front-end characteristics

- Dedicated to MPGD detectors and beyond
- 64 channels
- Large input capacitance range, optimized for 50-200 pF, reasonable gain up to 1nF
- Large range of peaking times: 50-500 ns
- Large choice of gain ranges: 0-50, 0-250, 0-500 fC or 0-5 pC
- Large range of input rates, up to 100 kHz/ch with fast CSA reset (limit assumed for EPIC: 25 kHz/ch)
- Reversible polarity
- Front-end elements can be by-passed

## Digital stage

- Fast sampling ADC for each channel on 12 bits (> 10 effective bits) at up to 50 MS/s
- Possibility under study to double rates by coupling pairs of channels
- Integrated DSP for internal data processing and size reduction, treatment processes to be selected according to user needs
- Continuous readout compatible with streaming DAQ foreseen at EIC, triggered mode also available
- Several 1 Gb/s output data links

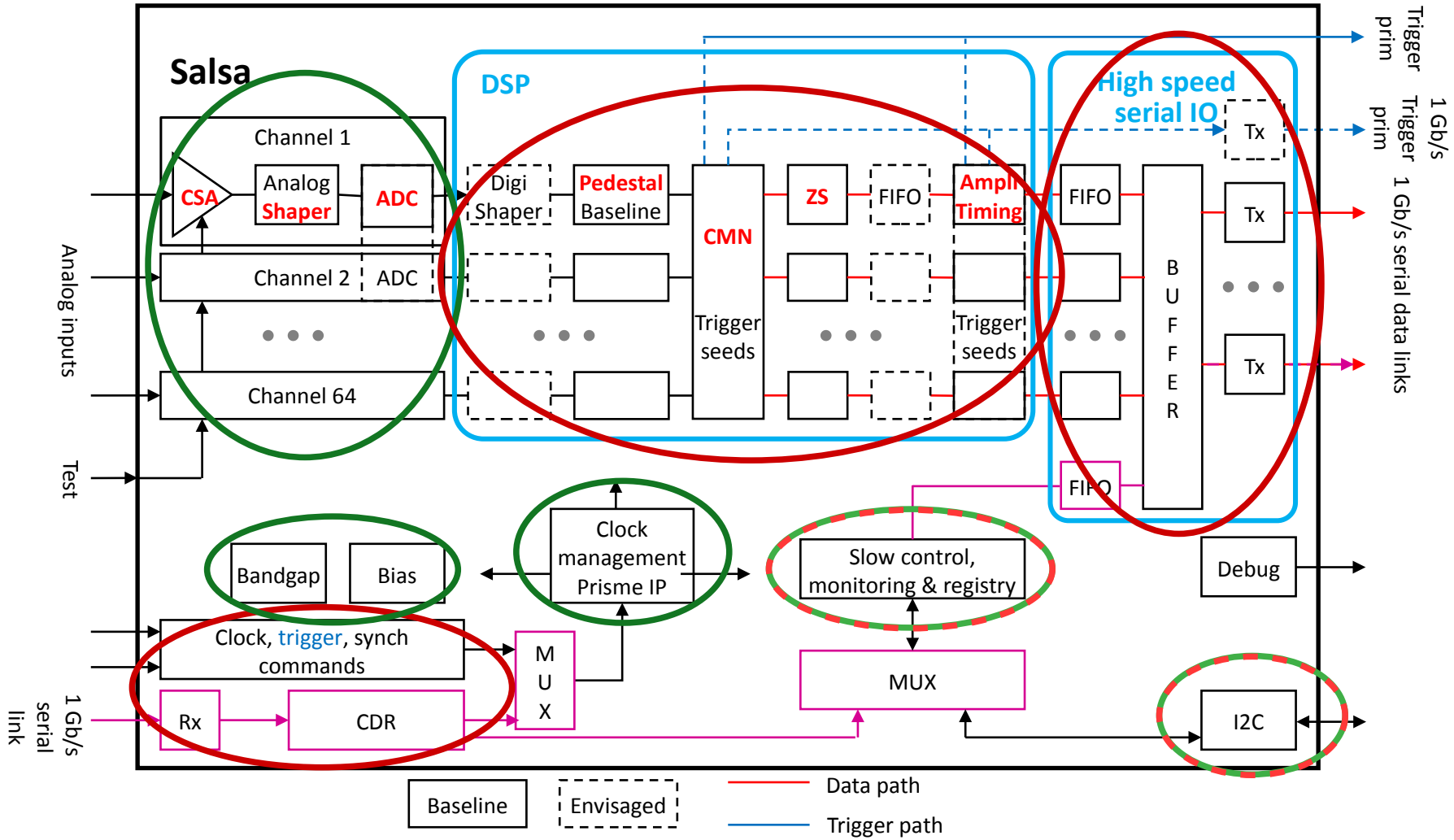
## General characteristics

- ~1 cm² die size, implemented on TSMC 65nm technology
- Low power consumption ~ 15 mW/channel at 1.2V
- Radiation hardened (SEU, TID)

# SALSA CHIP PRELIMINARY ARCHITECTURE

Exists in prototype

Development in progress



# CURRENT STATUS: PRISME

## PRISME block

- PLL IP block in TSMC 65nm technology for clock generation, 4 clock outputs
- Large frequency ranges for input (40-120 MHz) and outputs (up to 1.6 GHz)
- Very low internal time jitter: ~3 ps RMS up to 1 GHz

## PRISME prototype

- Tested from early 2024: PLL block, I2C, high speed I/O, bandgap, probes
- PLL ok with random jitter as low as 2.5 ps RMS, other blocks ok
- But large deterministic jitter, up to 50 ps RMS
- Origin of noise sources understood, fixed in PLL design

## Radiation tests

- X-ray radiation tests at CERN in November 24
- Up to 300 Mrad reached, all blocks except PLL ok
- PLL working nominally up to 160 Mrad, reduced internal frequency above
- Cause of degradation understood, improved transistor sizes

## Next steps

- New PRISMEv1 prototype submitted in December 24
- Several modifications: deterministic jitter, radiation hardness, lower internal frequency, inclusion of CDR for unified input interface, compatibility with lpGBT input frequency
- To be tested before summer

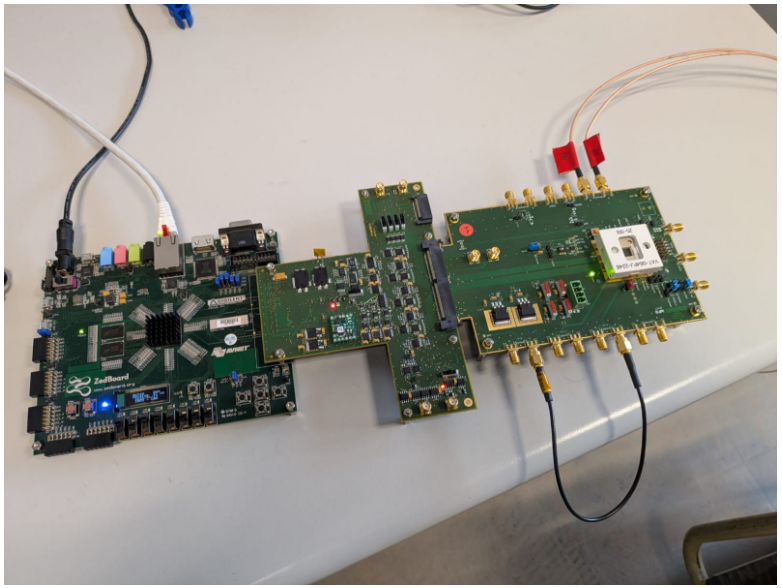
| | |
|---|---|
| Technology | CMOS 65 nm |
| Power voltage | 1.2V |
| Input reference frequency range | 50, 80, 100, 320 MHz ±20% |
| VCO frequency | 1.6-2 GHz |
| Number of output clocks | 4 |
| Output frequency | Programmable fractions of VCO frequency, up to 1 GHz |
| Phase shifter step | < 300 ps |
| Time interval jitter: analog path only | < 10 ps RMS up to 1 GHz with graceful degradation beyond |
| Time interval jitter: with digital paths | ~3 ps RMS up to 1 GHz with graceful degradation beyond |
| Power consumption | < 9 mW, < 12 mW with digital regulation |
| Size | ~0.1 mm² |
| Radiation mitigation | TMR, SEL free, TID up to 4 MGy |

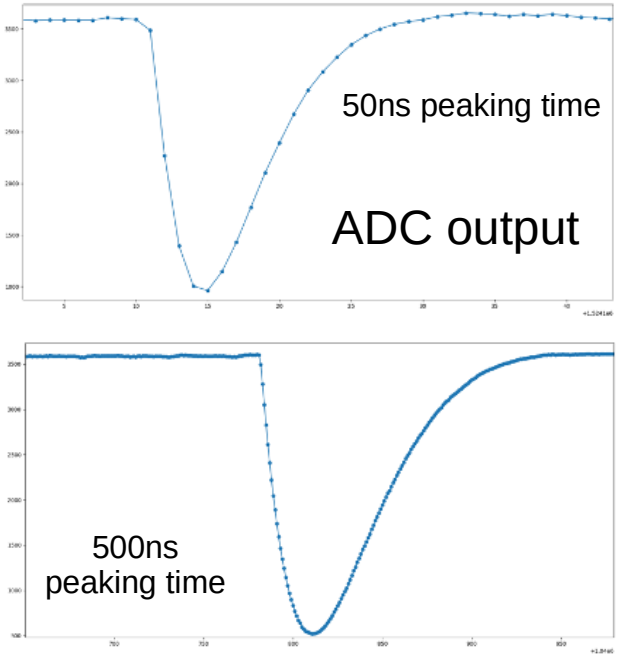
# CURRENT STATUS: SALSA1

## SALSA1 prototype

- 1st prototype with frontend + ADC chained, 4 channels, + 2 ADC alone
- Naked dies received beginning of October 24, packaged ones beginning of November
- Test cards delivered in December, tests started right before Christmas break
- Chip powered on without problem, nominal power current (78 mA)
- I2C interface working, slow-control registers responding correctly
- Both kinds of frontend channels ok, no oscillation as observed with SALSA0 in specific cases
- Sao Paulo ADC digitizing front-end signals correctly
- Next steps: systematic measurements with various configurations

SALSA1 test setup





# CURRENT STATUS: SALSA2

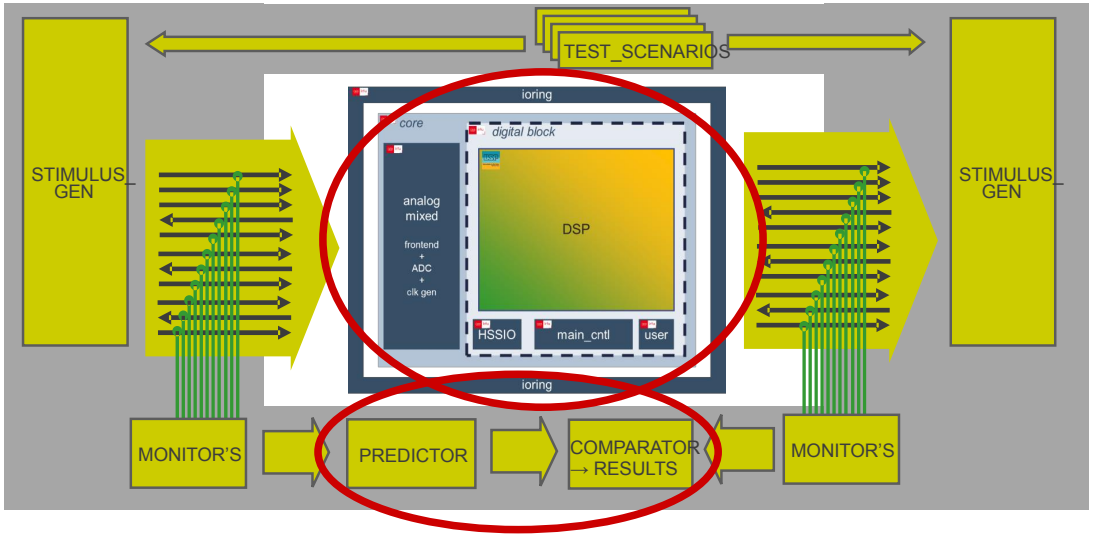
## SALSA2 development status

- Main DSP modules and associated algorithms defined, study still ongoing for peak finding algo
- Work ongoing on HDL code of DSP modules, progresses on several modules: pedestal equalization, common mode correction, baseline following algorithm, zero suppression algorithm, packet building, data formatting, data serialization, serial input and output links
- New PLL version including CDR produced and integrated, to be checked with PRISMEv1
- UVM environment under development for high level verifications
- Packaging under study, planed to be identical to the final SALSA one

## Timeline

- Still a lot of works ahead:
  - code development of missing modules
  - code verification and validation
  - integration of all modules, validation
  - DSP layout generation and validation
  - assembly of all blocks
  - simulations of the whole chip
- Chip submission not expected before October 2025 (last MPW run slot of the year)
- Tests in 2026
- Distribution to users before end 26

UVM environment



# PROJECT MILESTONES AND NEXT STEPS

## eRD109 FY23 project milestones

- Specifications of SALSA1 design → done
- Production of SALSA1 prototypes → done
- Test card production → done
- Performance evaluation → ongoing

## Milestones of generic R&D program for EIC project (new 65nm PLL block)

- PRISME prototype submission → done July 19th 2023
- Packaging and test card production → done February 2024
- Radiation tests → done November 2024

## eRD109 FY24 project milestones

- SALSA2 specifications → July 2024
- SALSA2 submission → foreseen October 2025
- Beginning of SALSA2 tests → 1st semester 2026

## Very next steps

- SALSA1 tests → ongoing
- New PRISMEv1 chip → expected in Spring
- SALSA2 development → in progress