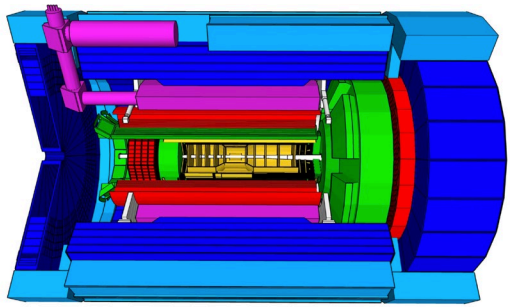


eRD109 update: dRICH RDO

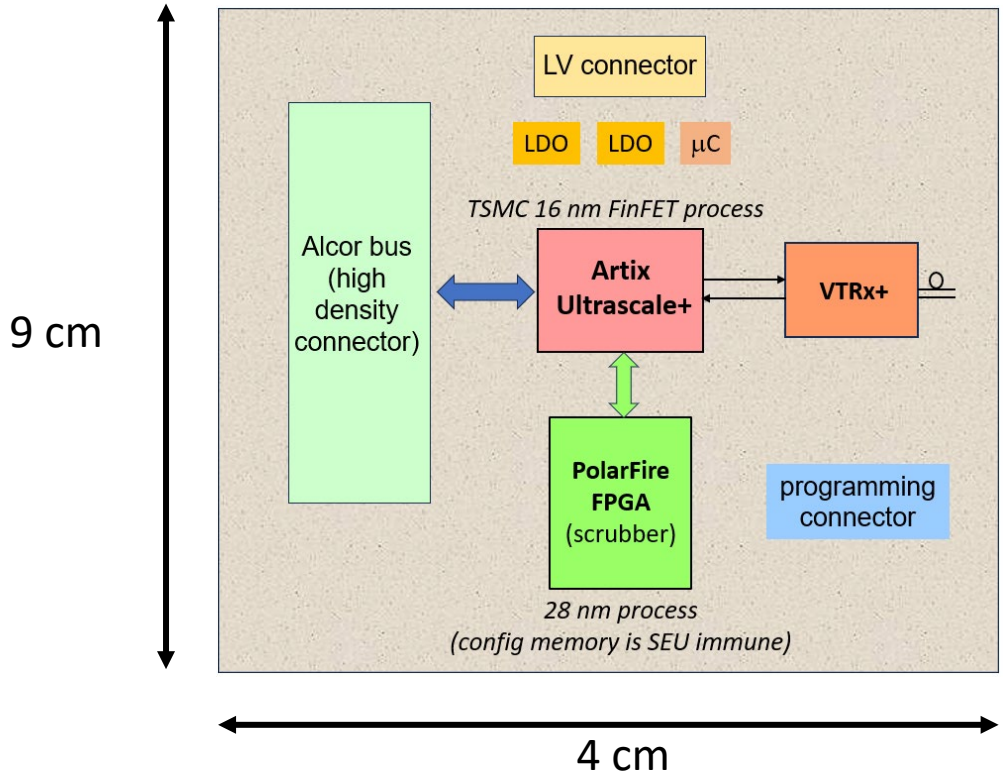
Pietro Antonioli, Davide Falchieri
on behalf of the INFN Bologna RDO team

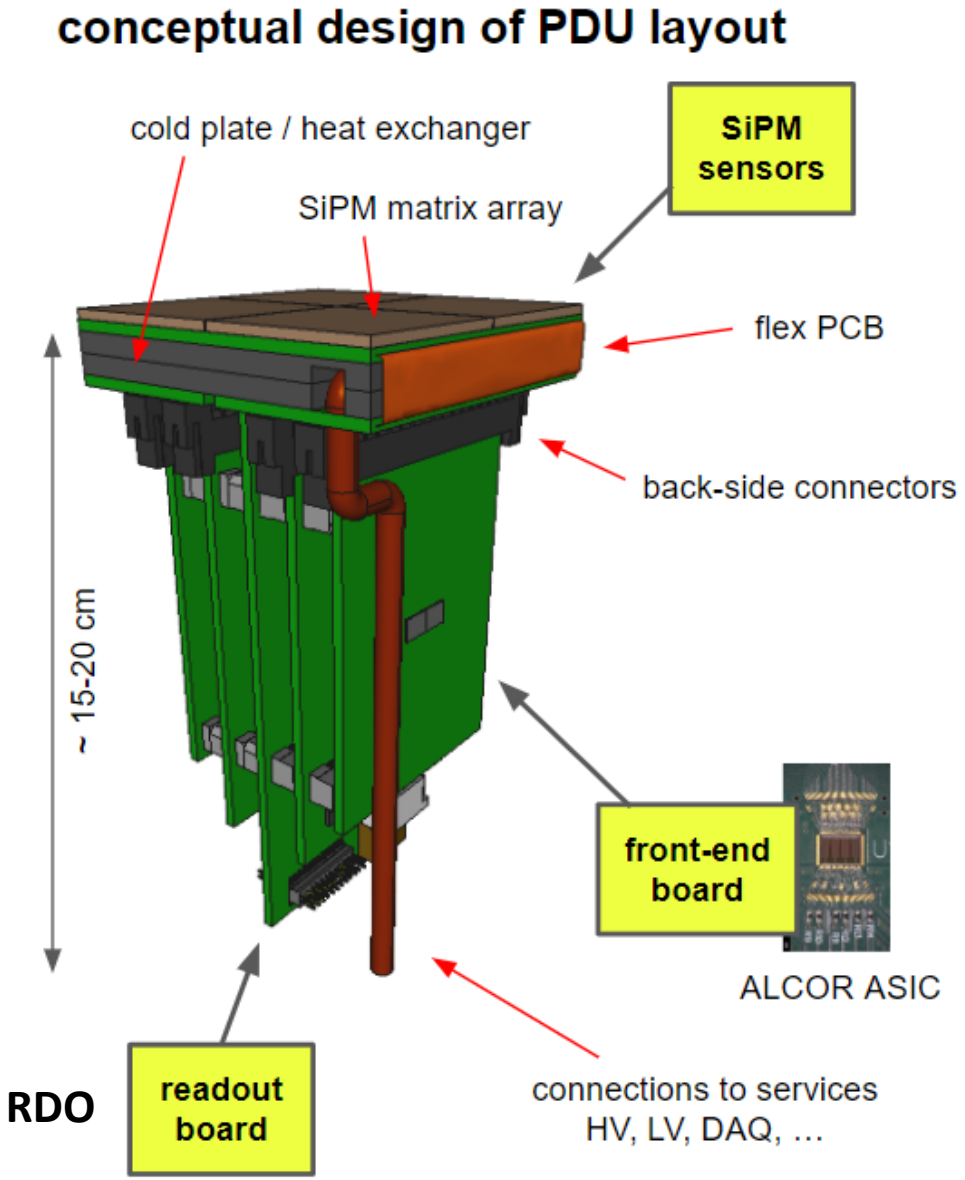
EPIC Electronics & DAQ WG meeting
06 February 2025

RDO news

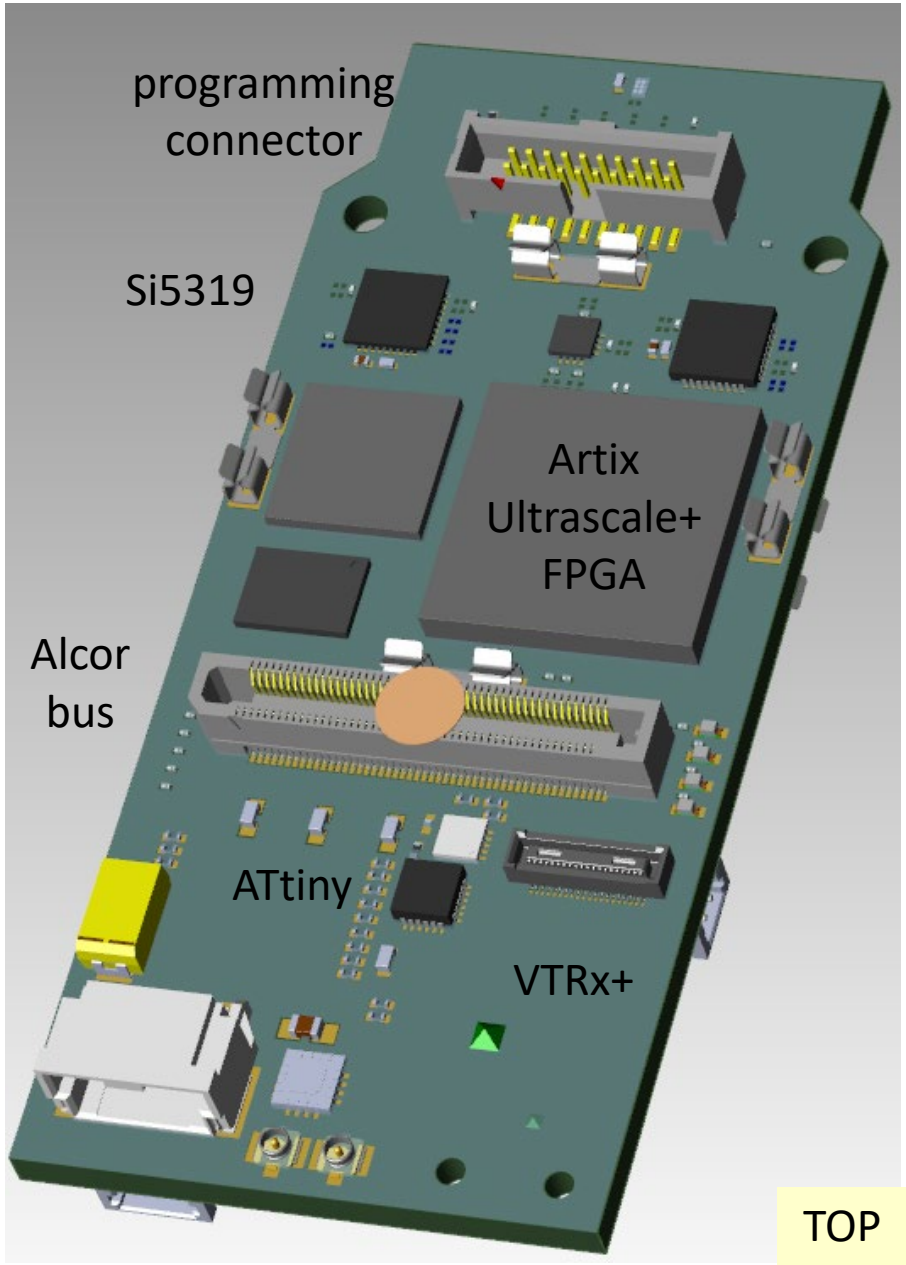
Current RDO design status:

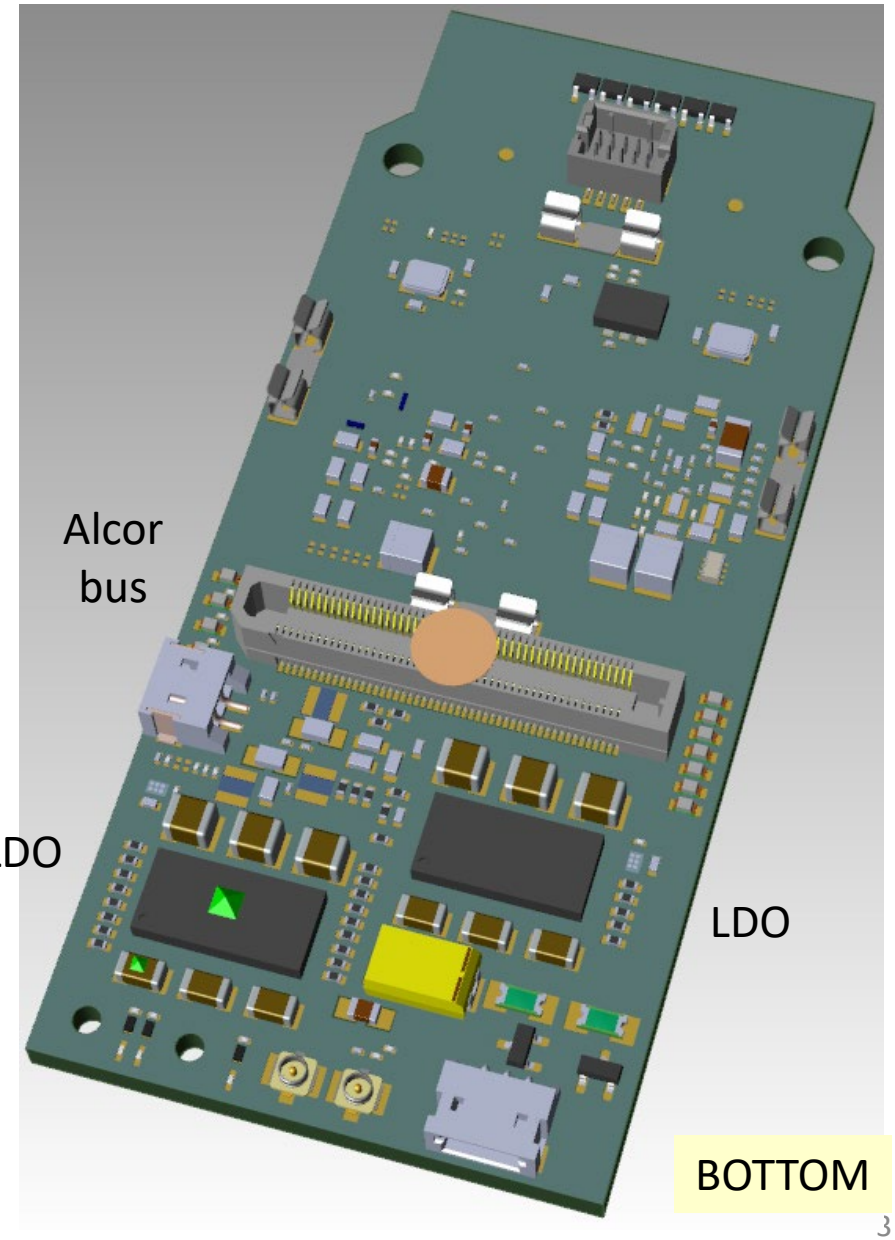
- components placement finalized, starting the PCB routing
- firmware design & test on an Alinx FPGA board
- irradiation tests of some RDO components at Trento





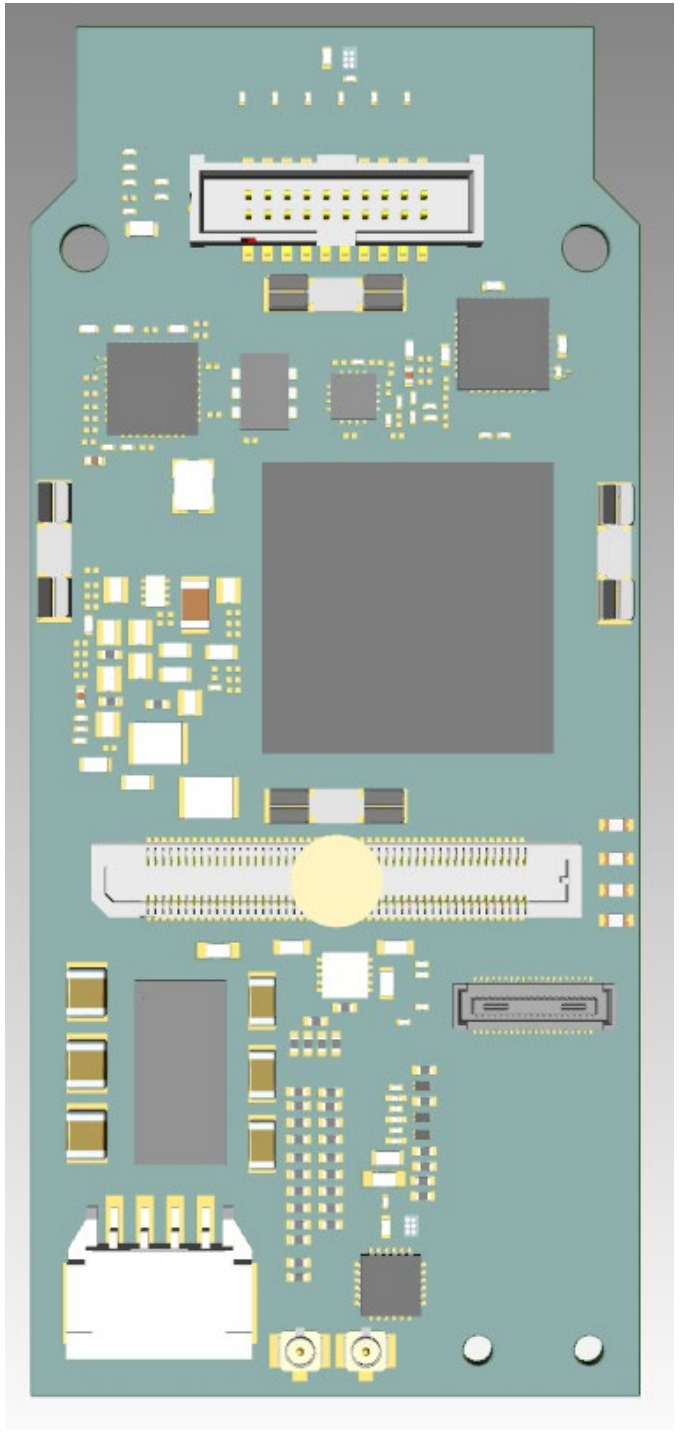
Towards RDO final placement





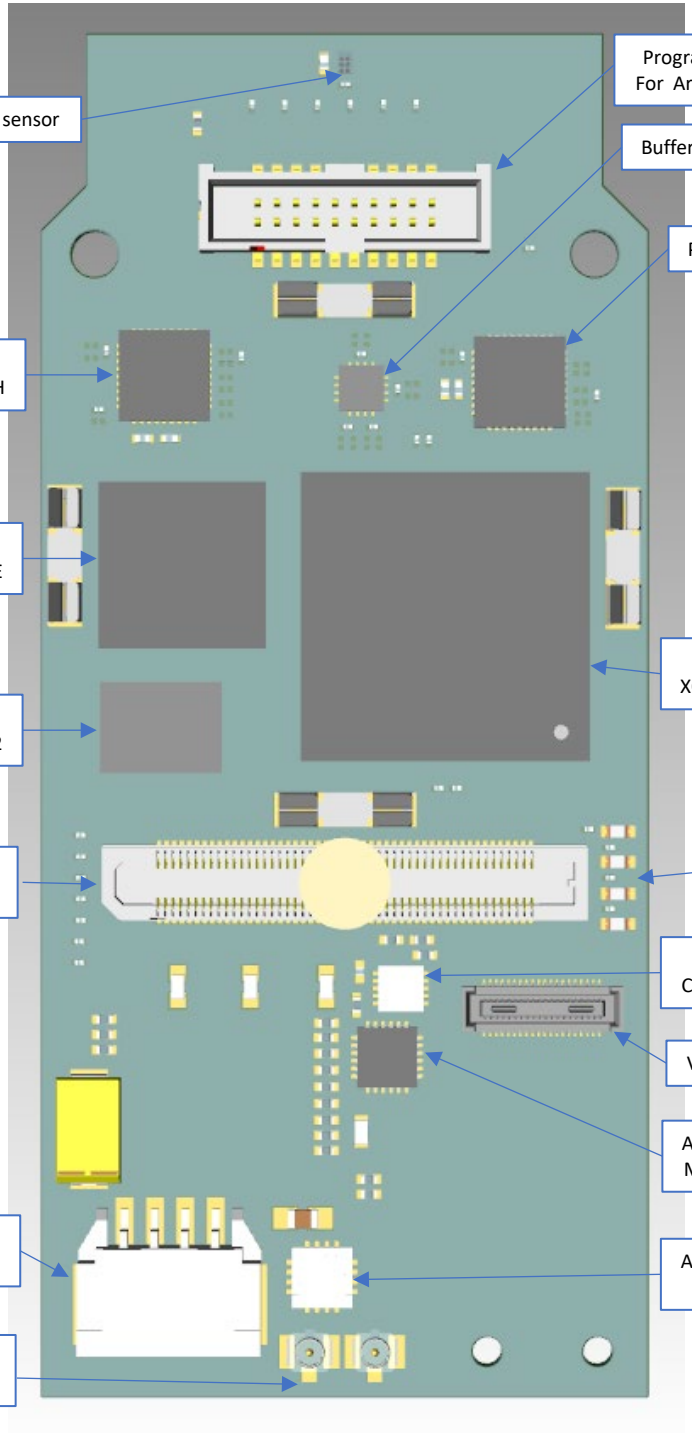
RDO layout

TOP



Before

Now

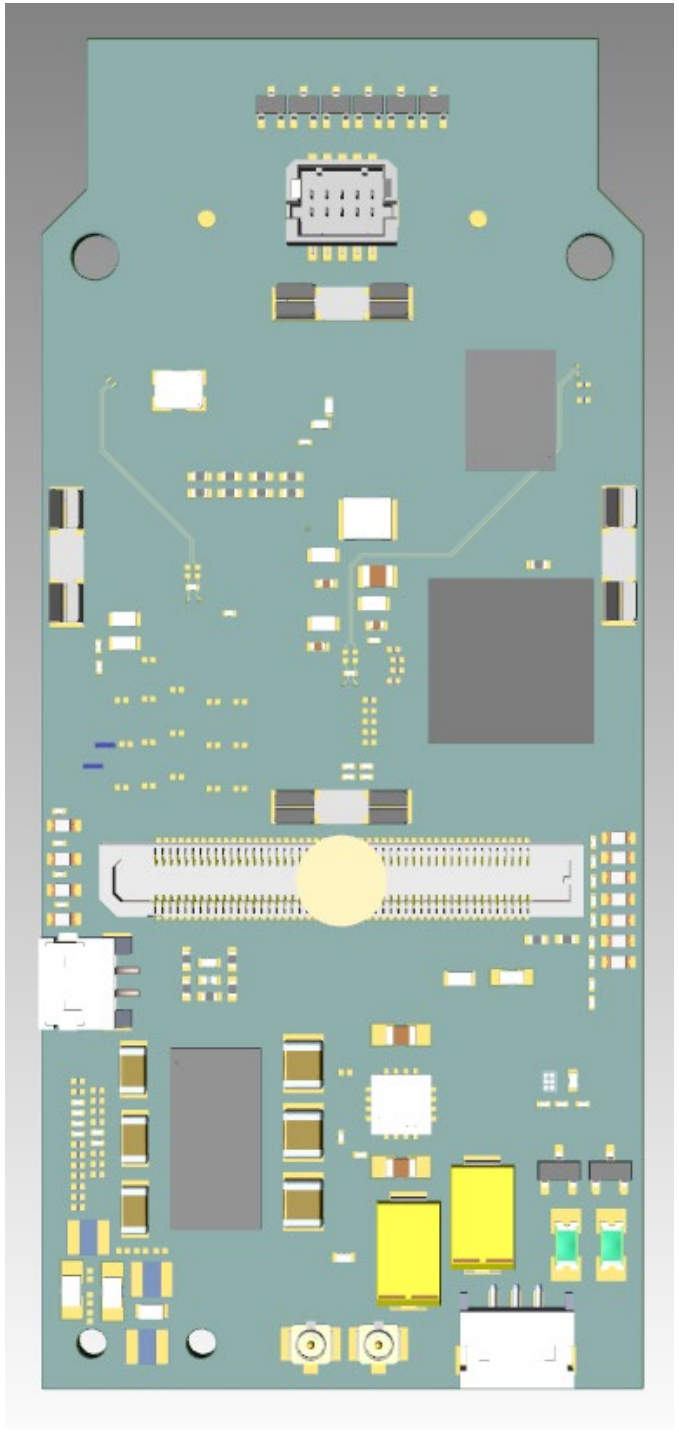


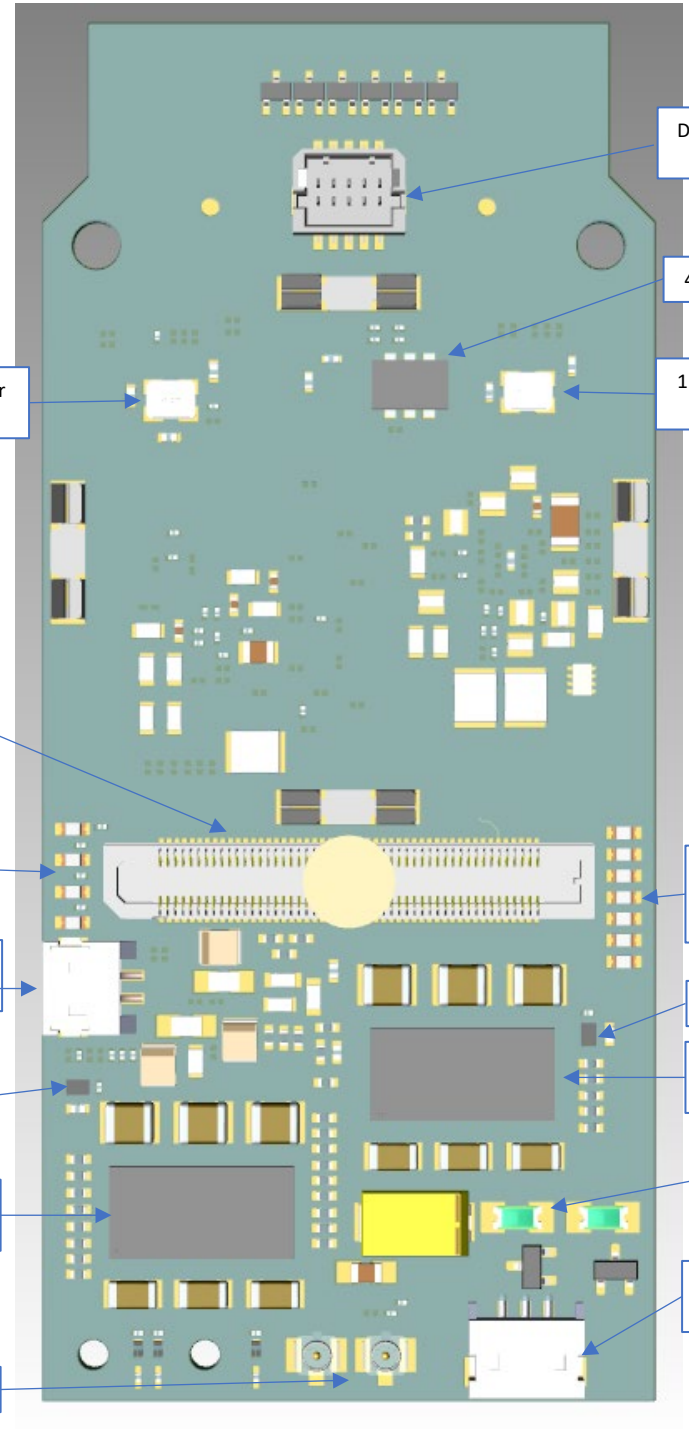
RDO layout

BOTTOM

Before

Now



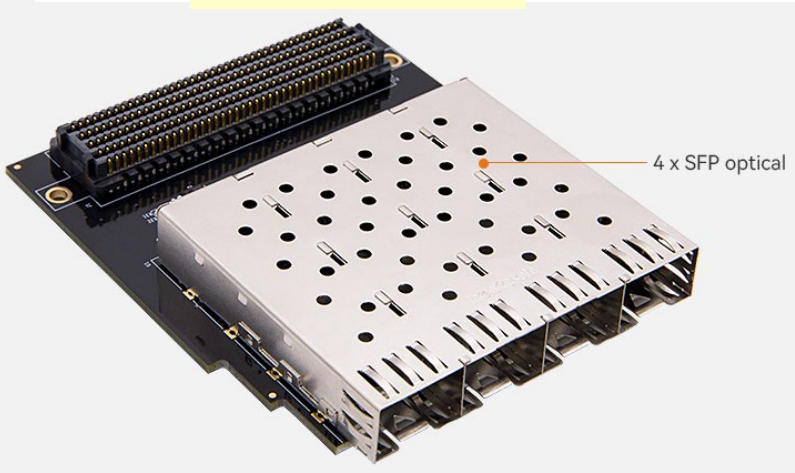


Firmware design

AXAU15 FPGA Dev Board & Kit with AMD Artix US+ XCAU15P

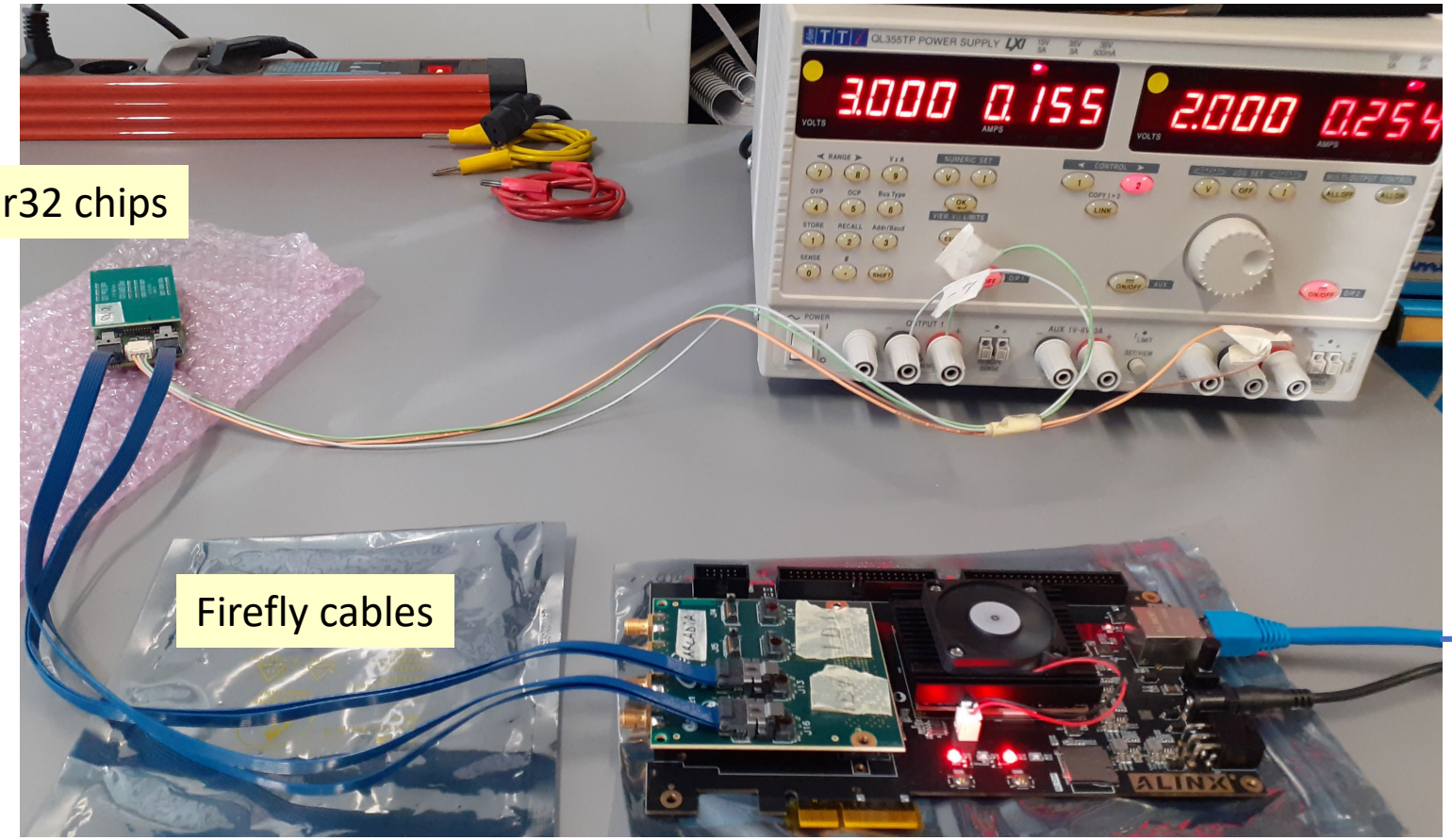
Alinx

FMC SFP board



This commercial board hosts the same FPGA as the RDO (AU15P), but with a different package: we are using it to perform firmware design and test before the first RDO board is available

Firmware design: Artix – Alcor interface

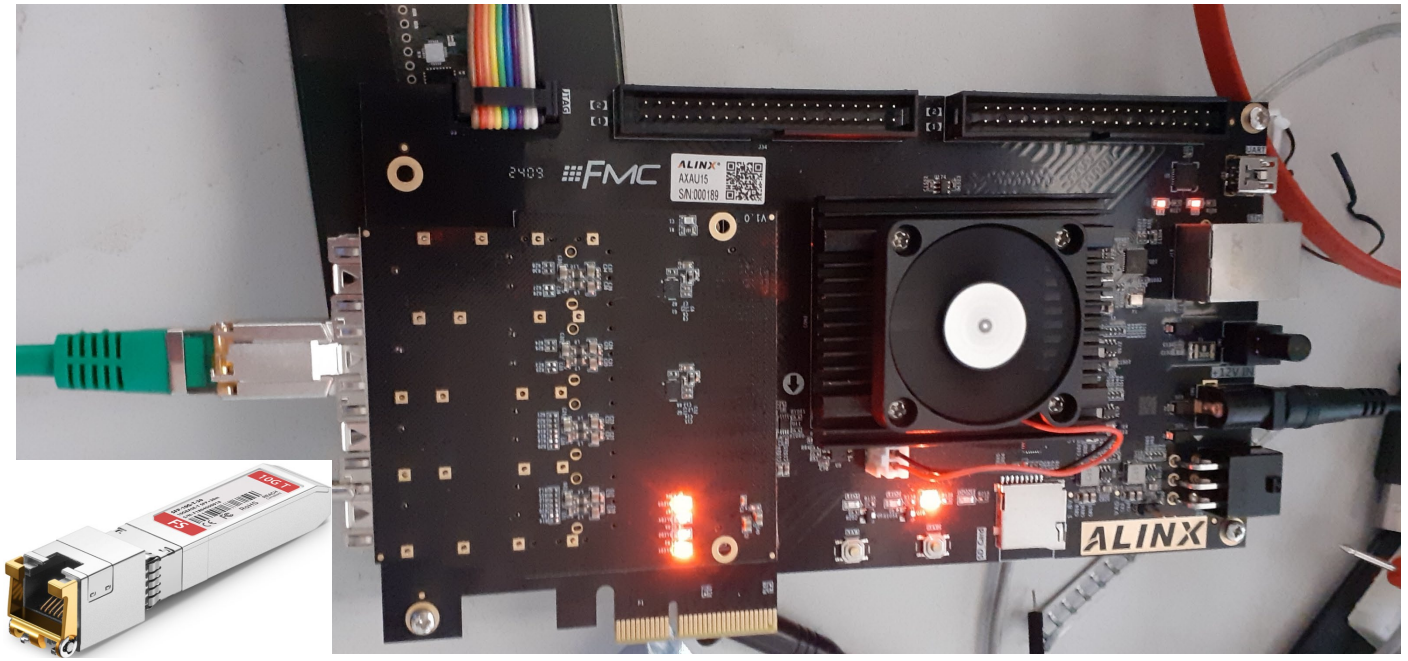


In order to test the Artix – Alcor interface, we implemented the IPbus firmware on the FPGA. Now we can program the Alcor registers via SPI, but we still cannot correctly receive the data (next to-do task)

Firmware design: Artix – SFP interface

Ethernet cable

Alinx + FMC SFP board

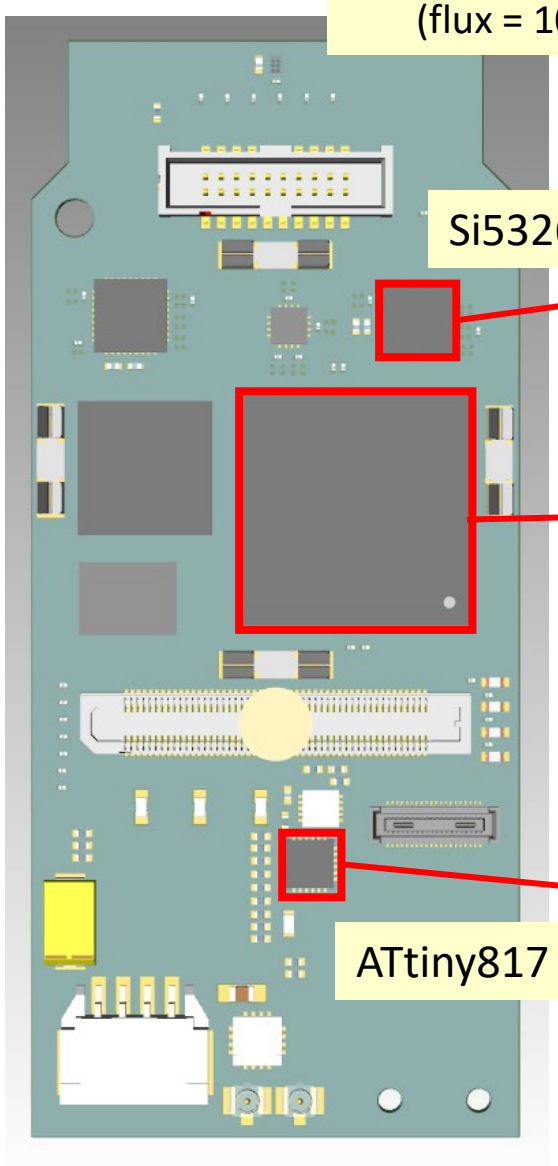


GBIC SFP with RJ45 connector

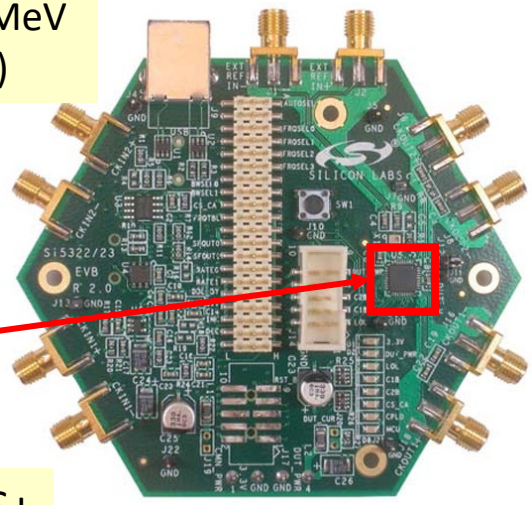
In order to mimic the Artix – VTRx+ interface, we implemented the IPbus firmware on the FPGA and tested it

Proton irradiation campaign at proton irradiation facility (Trento)

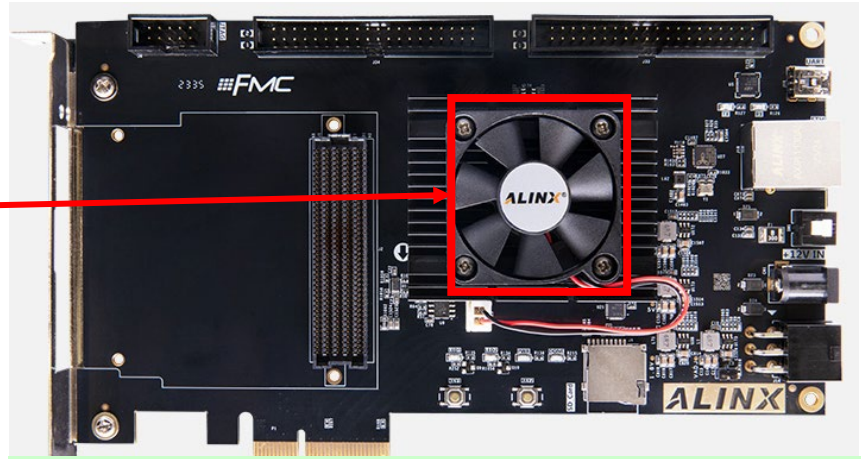
proton beam @ 100 MeV
(flux = 10^8 Hz/cm^2)



Si5326

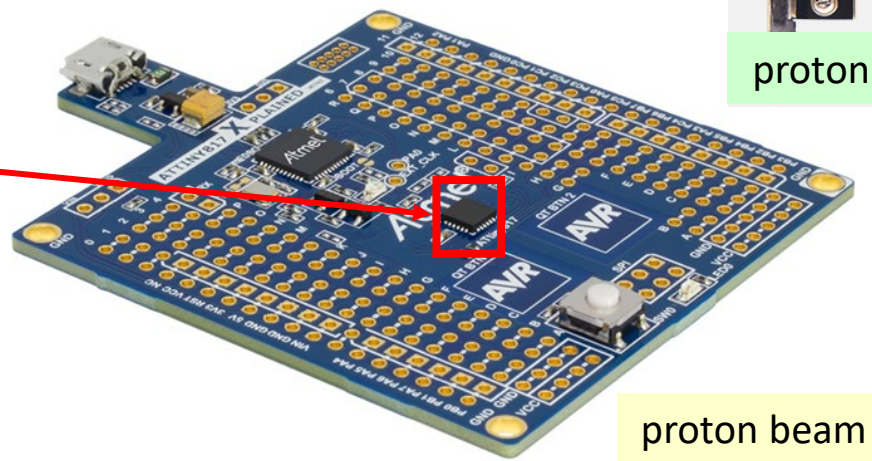


Artix US+



proton beam @ 70 MeV (flux = 10^6-10^7 Hz/cm^2)

ATtiny817



proton beam @ 100 MeV (flux = 10^8 Hz/cm^2)

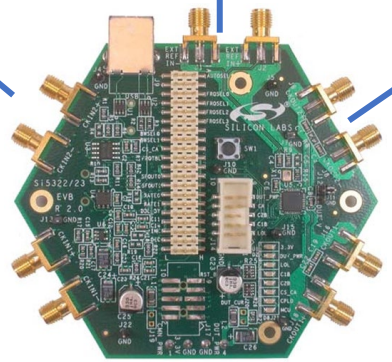
https://agenda.infn.it/event/43344
for more details

Proton irradiation: Si5326

jitter measurement

looking for SEL

looking for SEUs



Si5326

beam

proton beam @ 100 MeV (flux = 10^8 Hz/cm^2)

2007/2048 bits of configuration memory monitored

TID = 42 krad (dose rate 1-2 krad/min)

 # SEUs = 19
 # SELs = 0
} in 1553 s

$$\sigma_{SEU} = (2.11 \pm 0.50)10^{-14}\frac{cm^2}{bit}$$

MTBF in the dRICH system (1248 RDOs) for each Si5319 and Si5326:
3.8 hours

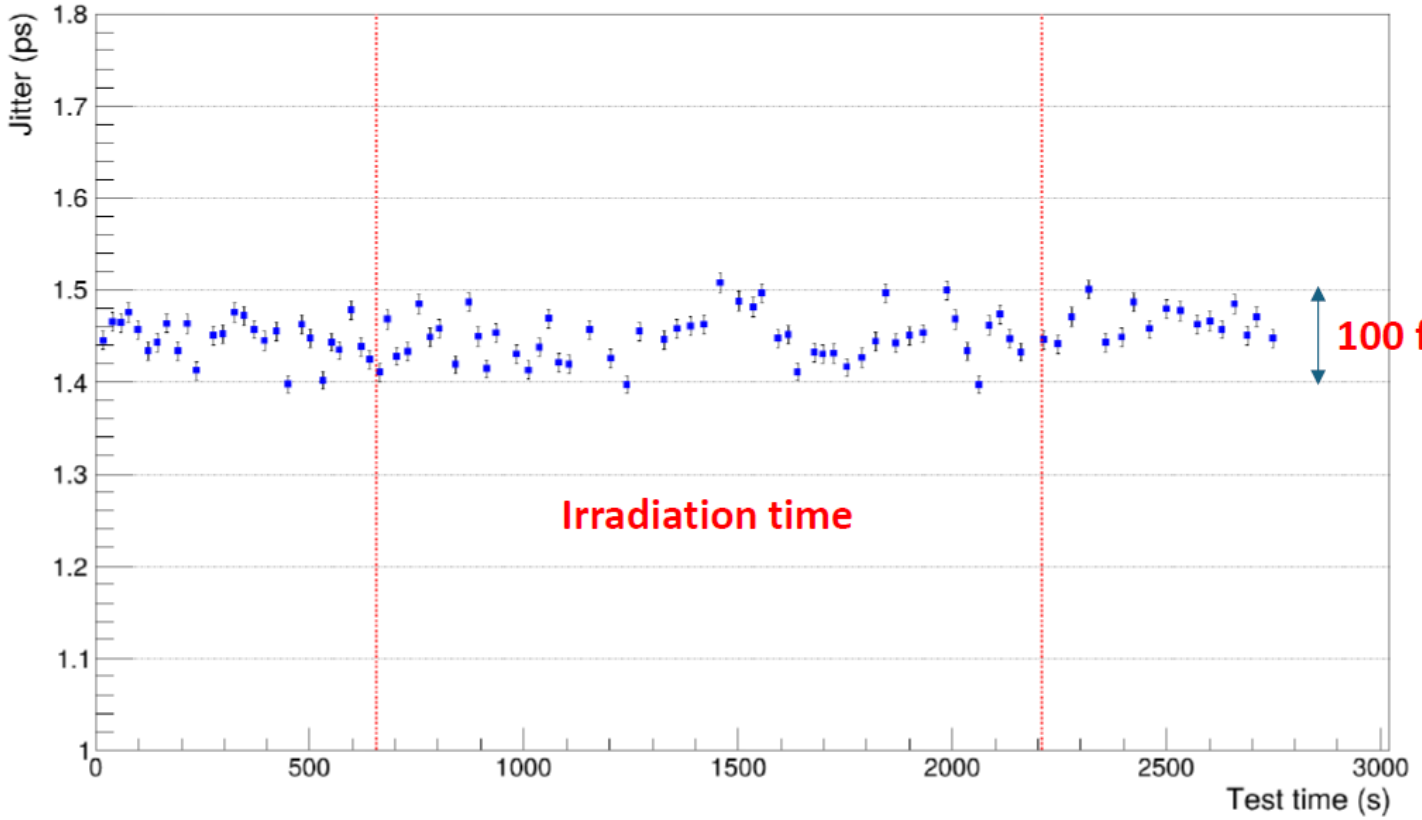
PLL lock signal was never lost

Proton irradiation: Si5326

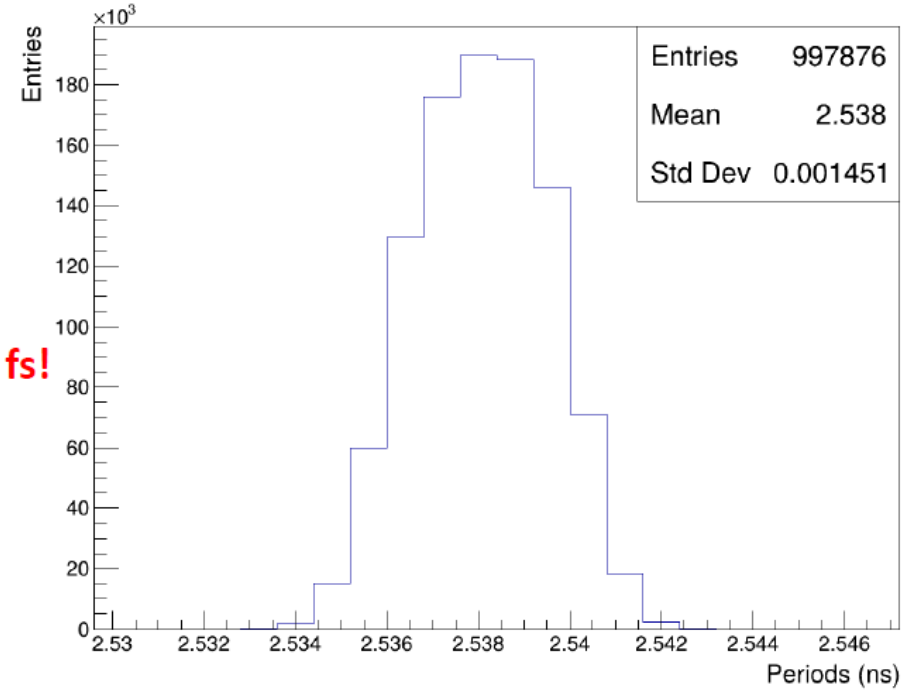
Jitter and period of the output clock

Si5326 RMS jitter plot

$$\text{Jitter} = \frac{\text{RMS jitter}}{\sqrt{2}}$$



Output clock period measurements

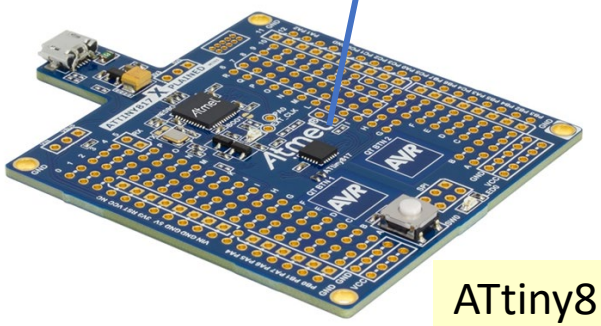


$$f_{ALCOR} = f_{EIC} \cdot 4 = 394\ \text{MHz}$$
(T = 2.538 ns)

Proton irradiation: ATtiny

looking for SEUs

looking for SEL



ATtiny817

beam

proton beam @ 100 MeV (flux = 10^8 Hz/cm^2)

6.6/8 Kbytes of FLASH memory monitored
450/512 bytes of SRAM memory monitored

TID = 23 krad (dose rate 1-2 krad/min)

 # SEUs on SRAM = 21
 # SEUs on FLASH = 0
 # SELs = 0
} in 1026 s

$$SRAM\ \sigma_{SEU} = (3.89 \pm 0.54)10^{-14}\frac{cm^2}{bit}$$

$$FLASH\ \sigma_{SEU} < 2.32\ 10^{-16}\frac{cm^2}{bit}\ (limit\ @\ 95\%\ C.L.)$$

MTBF in the dRICH system (1248 RDOs) for ATtiny817:
SRAM: 4.0 hours
FLASH > 43 hours

CAUTION

The chip stopped working @ 23 krad

Proton irradiation: Artix Ultrascale+

looking for SEUs

looking for SEL

beam

proton beam @ 70 MeV
(flux = 10^6-10^7 Hz/cm^2)

8/156 kbit of DFFs
3.6/5.1 Mbits of BRAM
33/33 Mbits of CRAM
} monitored

TID = 6.36 krad (dose rate 10-500 rad/min)

 # SEUs on DFFs = 0
 # SEUs on BRAM = 69
 # SEUs on CRAM = 81
(70 corrected, 11 uncorrected, 1 dead link)
} in 2560 s

 # SELs = 0 in 3632 s

$$DFF\ \sigma_{SEU} < 3.5\ 10^{-14}\ \frac{cm^2}{bit}$$ → MTBF > 3.6 min

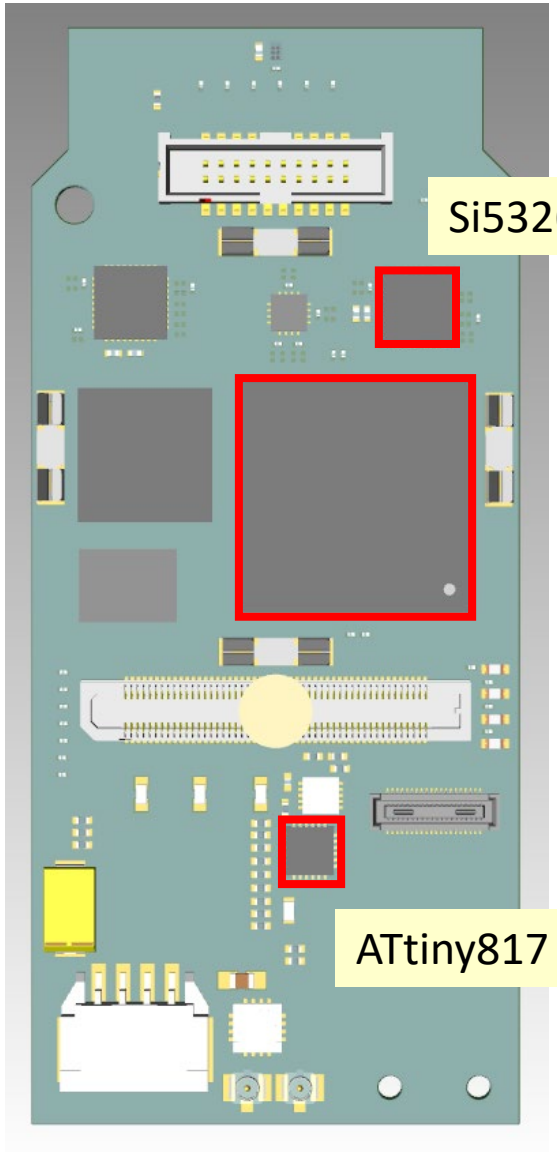
$$BRAM\ \sigma_{SEU} = (1.78 \pm 0.23)10^{-15}\ \frac{cm^2}{bit}$$ → MTBF = 2.1 min

$AMD\ estimate$: $(0.98 \pm 0.18)10^{-15}\ \frac{cm^2}{bit}$

$$CRAM\ \sigma_{SEU} = (2.30 \pm 0.28)10^{-16}\ \frac{cm^2}{bit}$$ → MTBF = 2.5 min

$AMD\ estimate$: $(2.67 \pm 0.48)10^{-16}\ \frac{cm^2}{bit}$

Irradiation campaign wrap-up



Si5326

MTBF: 3.8 h → AU15P will check the chip configuration every few hours

TID = 18 TID_5

Artix US+

DFF MTBF > 3.6 min
BRAM MTBF = 2.1 min
CRAM MTBF = 2.5 min

→ manageable at firmware level using TMR, CRC and reset features

→ we need to implement a fast SEU correction with a scrubber (MPF50T)

TID = 2.8 TID_5

ATtiny817

MTBF: SRAM: 4.0 h, FLASH > 43 h → key RAM registers will be implemented with TMR checks

TID = 10 TID_5

TID_5 (2.3 krad) is the expected TID with a safety factor of 5

Next steps

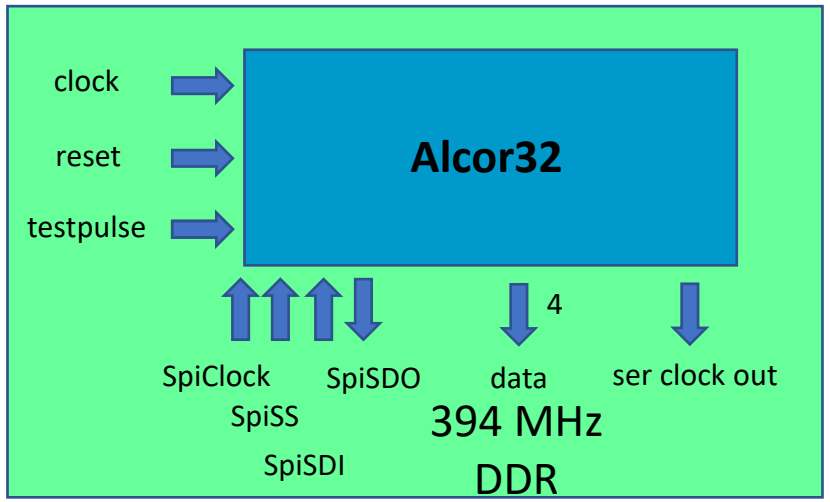
- finalize RDO PCB design
- progress on the firmware with the Alinx until the RDO is available
- perform one more irradiation test in May 2025 with:
    - ATtiny
    - LDO (LTM4709)
    - Artix Ultrascale+

Thanks!

Backup

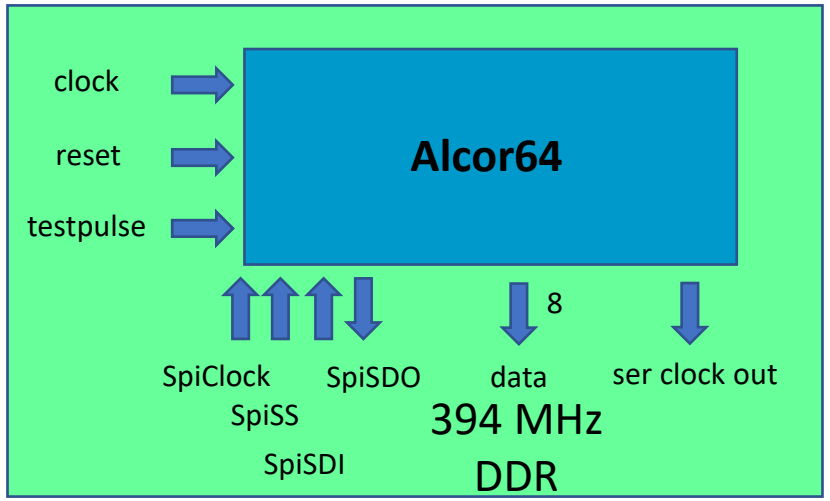
Alcor32 vs Alcor64 I/Os

394 MHz



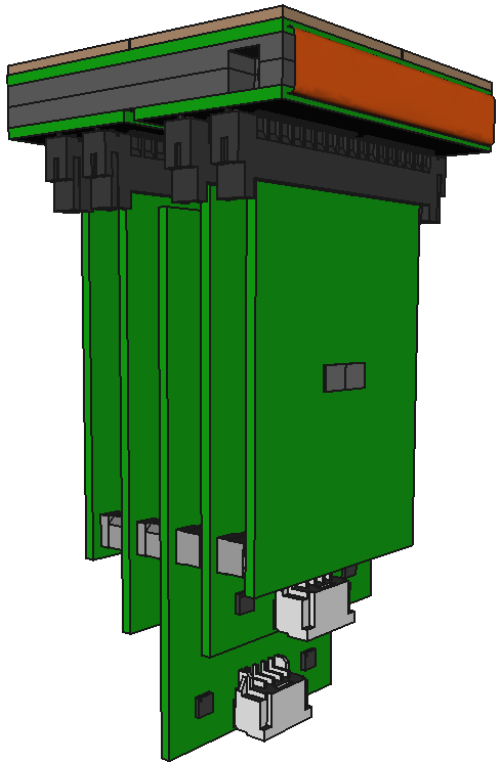
12 LVDS pairs per chip

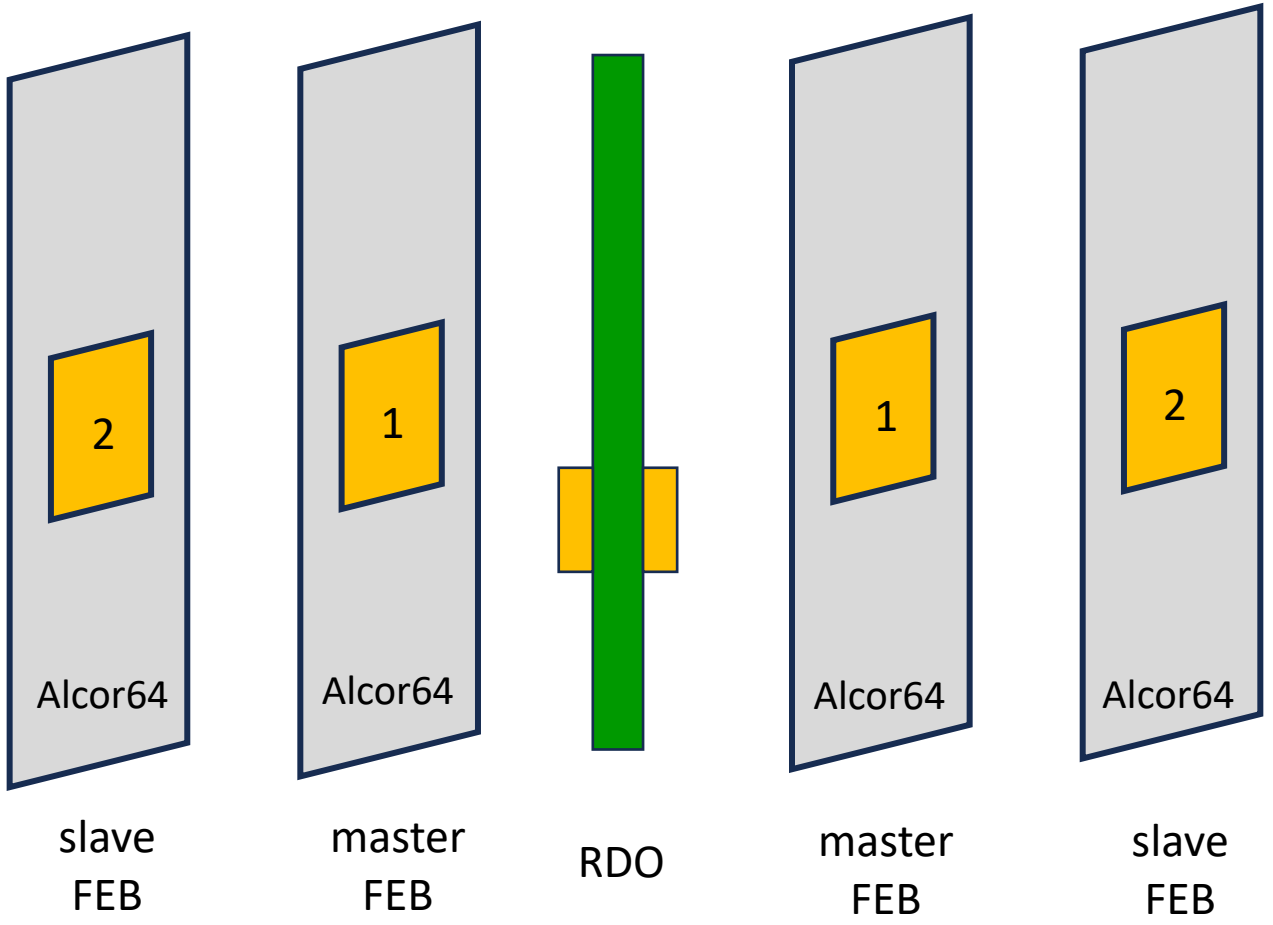
394 MHz



16 LVDS pairs per chip

When ALCOR64 is ready





In a first stage