

ALCOR - dRICH Readout

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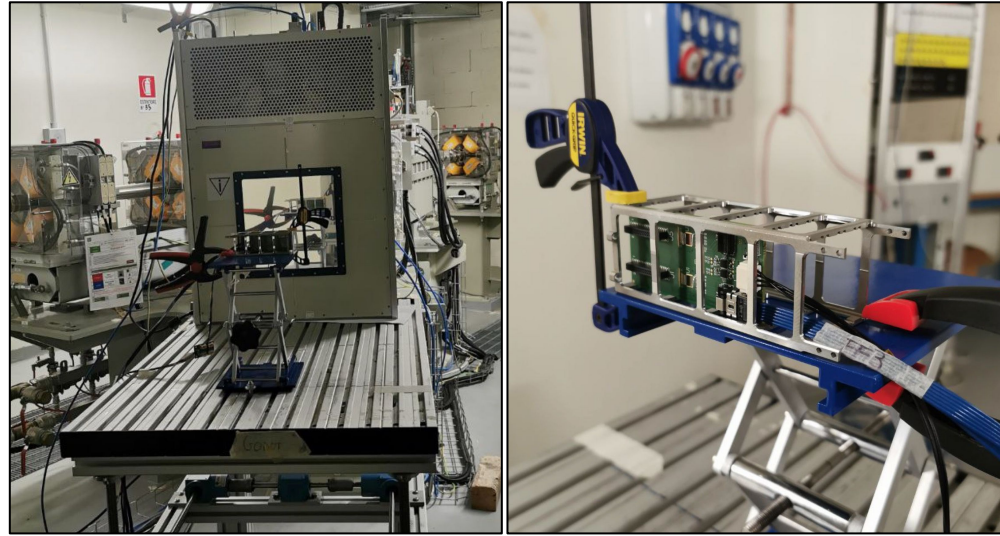
ePIC Electronics & DAQ WG meeting
eRD109 Monthly Progress Reports

06.02.2025

ALCOR irradiation tests

SEU/SEL and TID tests at Centro of Proton-Therapy in Trento (TIFPA) with ALCOR v2.1 (July 2024 and **December 2024**)

- Beam: 100 MeV proton
- Intensity: 10 - 100 nA
- Runs: typically 600 s
- Fluence collected per run: 10^{11} - 10^{12} p/cm²



Detailed results presented at the 29th Jan 2025 dRICH Meeting:
<https://indico.bnl.gov/event/26313/>

- **Total fluence: $4.64 \cdot 10^{12}$ p/cm²** (Jul 2024)
and **$3.2 \cdot 10^{12}$ p/cm²** (Dec 2024)
- **Total TID: 436 krad**

TID expected for the dRICH \approx **2.3 krad** (for 1000 fb⁻¹, **safety factor of 5** included)

SEU/SEL results (July 2024)

ECCR/BCR/PCR registers checked against SEU (every second)

- ECCR $\sigma = (9.4 \pm 1.8) \cdot 10^{-14} \text{ cm}^2/\text{bit}$ periphery register → no TMR in ALCOR v2.1
- BCR $\sigma = (7.6 \pm 1.1) \cdot 10^{-14} \text{ cm}^2/\text{bit}$ periphery register → no TMR in ALCOR v2.1
- PCR $\sigma = (3.3 \pm 0.5) \cdot 10^{-15} \text{ cm}^2/\text{bit}$ pixel register → TMR (with auto-correction bug)

SEU rate in ePIC:

- dRICH Flux = 140 ($h > 20 \text{ MeV}$) / ($\text{cm}^2 \text{ s}$)
- ALCOR bits: (2048 + 192) = 2240 → ALCOR-64 bits will be 4480
- Total ALCOR: 4992
- Total bits: 4992 · 4480 = $2.2 \cdot 10^7$ bits

↓
*SEU due to accumulating bit flips
in triplicated registers over time*

➤ $\sigma = 3.3 \cdot 10^{-15} \text{ cm}^2/\text{bit}$ → **MTBF = $9.8 \cdot 10^4$ seconds → every 27 hours**

➤ No latchup events (from power supply currents monitoring)

SEU/SEL results (December 2024)

ECCR/BCR/PCR registers checked against SEU (every second), **PCR re-written every 10 seconds to “mask” TMR auto-correction bug**

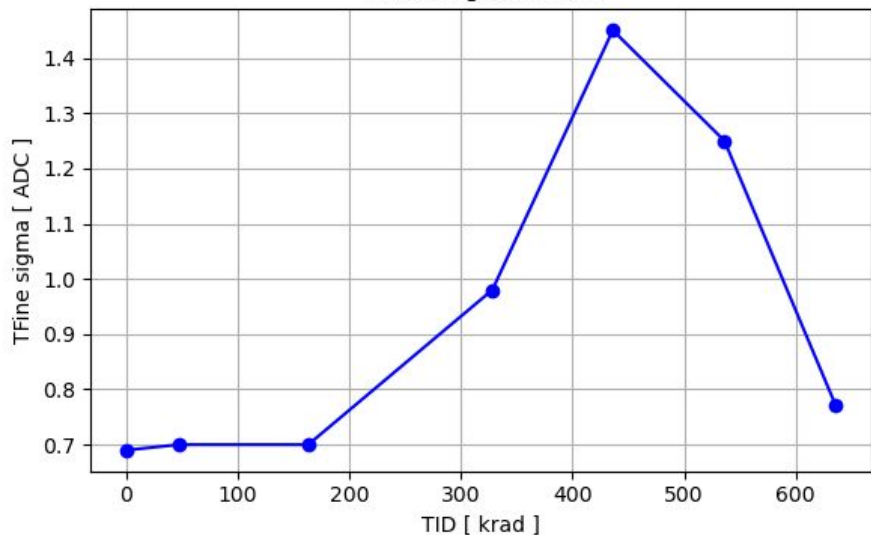
- ECCR $\sigma = 9.8 \cdot 10^{-14} \text{ cm}^2/\text{bit}$ periphery register → no TMR in ALCOR v2.1
- BCR $\sigma = 6.1 \cdot 10^{-14} \text{ cm}^2/\text{bit}$ periphery register → no TMR in ALCOR v2.1
- PCR **no SEU detected** re-written every 10 seconds to avoid TMR auto-correction bug

ALCOR v3: TMR SEU protection added also for periphery registers (used *CERN TMRG tool* for all registers, now feedback from the output of the voter correctly provides auto-correction and protects against accumulating errors due to SEU over time), Hamming code SEU protection for FSMs

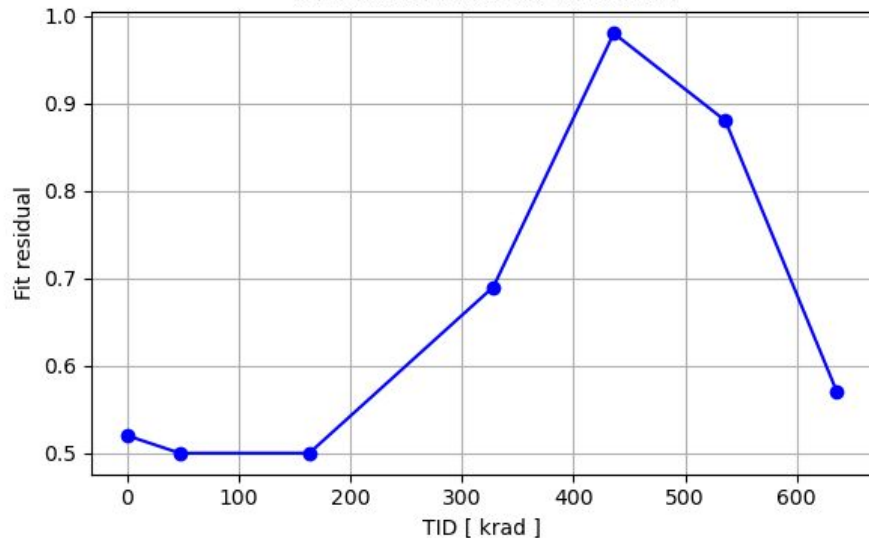
TID results - TDC sigma & fit residual

$$S_{res} = \sqrt{\frac{\sum (Y - Y_{est})^2}{n - 2}}$$

TFine Sigma Mean

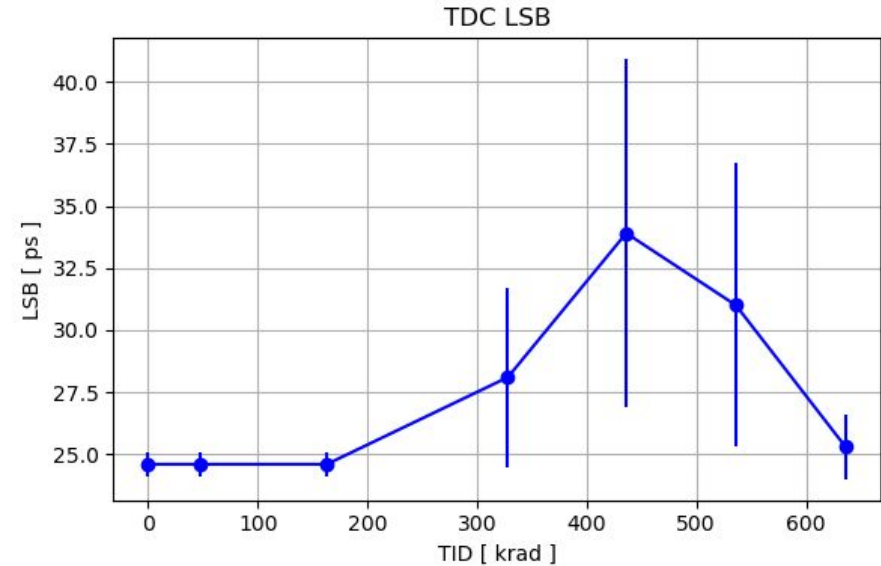
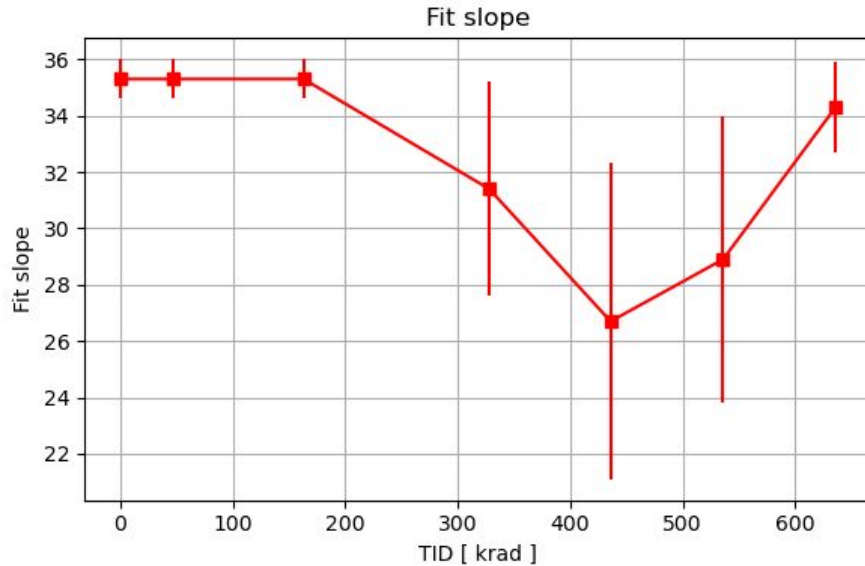


Fit residual standard deviation



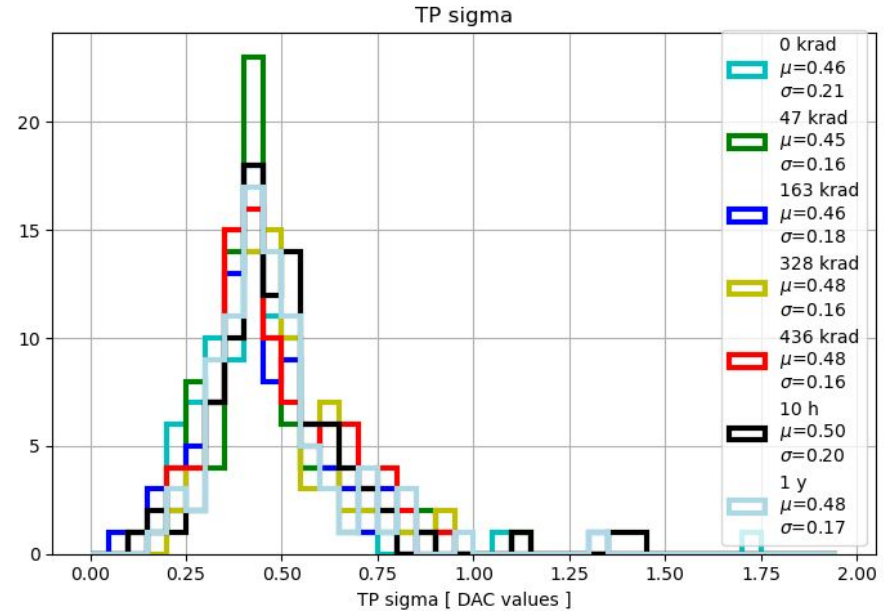
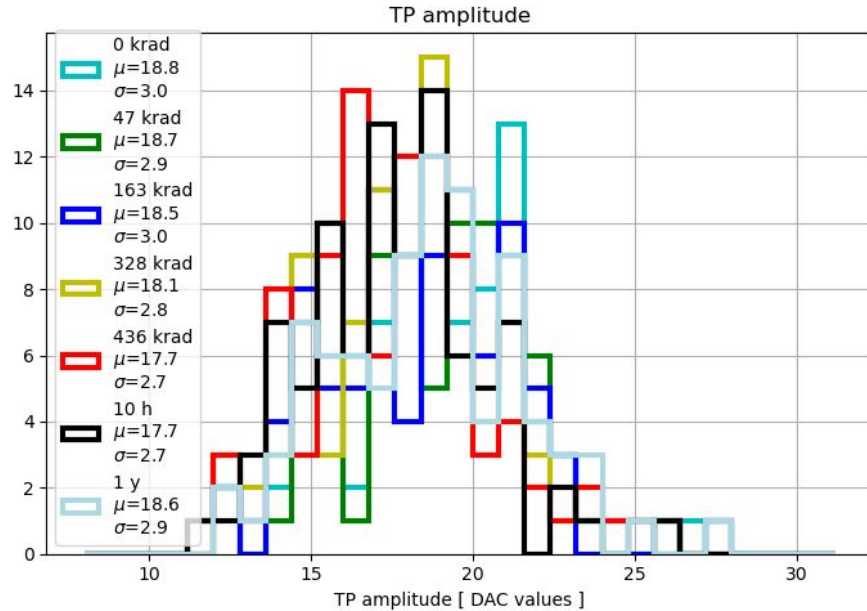
- **TFine sigma** starts to increase after 328 krad, >2 ADC after 436 krad on several pixels/TDCs
- **Fit residual** shows linearity degrading after 328 krad, much worse after 436 krad
- Last two points show good recovery from radiation damage with time (not complete)

TID results - TDC fit slope and LSB



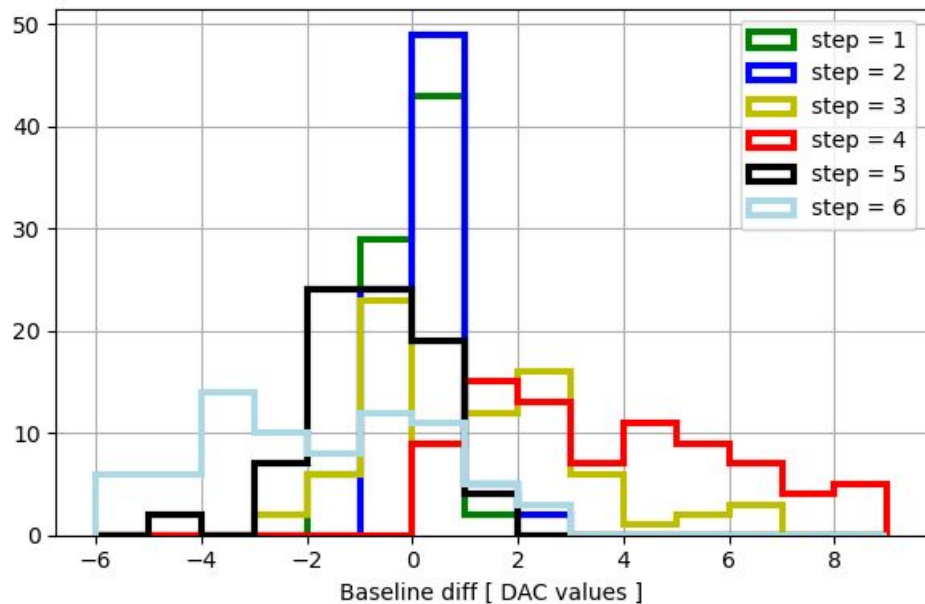
- Fit slope degraded after 328 krad → worse **linearity** and very broad **LSB** distribution
- Last two points show good recovery from radiation damage with time (not complete)

TID results - Front-End (Vth scan + test-pulse)

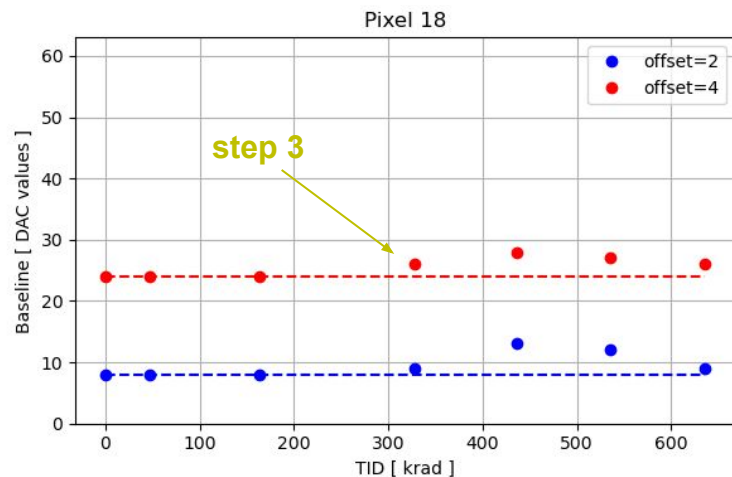
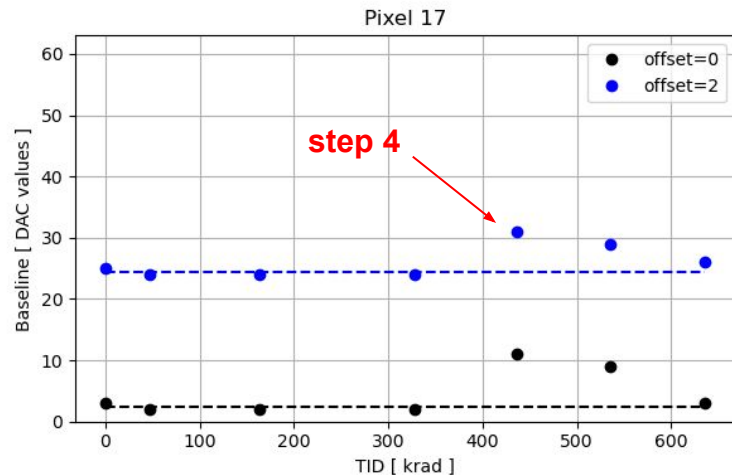


- Very small decrease in **signal amplitude** (almost completely recovered with time)
- Very small increase in **signal sigma** (almost completely recovered with time)

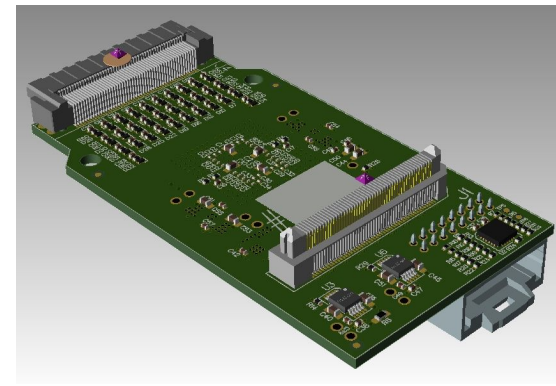
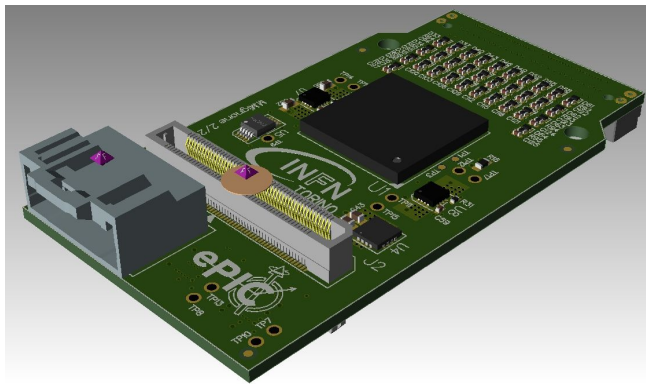
TID results - Front-End baseline



Signal baseline moving up after **step 3** (328 krad) and/or **step 4** (436 krad), returning down after **step 5** (after 10 hours) and **step 6** (after 5 months)



2025 Milestones



- ❑ Completion of the design of the final FEB first version (May 2025)
 - Functionalities defined, components selected, schematic done
 - Layout ongoing: many constraints already finalized to match RDO and ALCOR designs, PCB traces routing ongoing
 - “Fake FEB” version submitted in Dec 2024, allows integration of RDO with 2023-2024 PDU modules (with ALCOR v2.1), expected to be delivered by the end of Feb 2025, will be used for 2025 beam tests

- ❑ Electrical characterization and test of the new functionalities of ALCOR v3 with the socket test board (September 2025)
 - Delay on ALCOR v3 tapeout due to MPW run canceled by UMC: November 2024 → 31st March 2025
 - This will introduce some delay for this milestone

