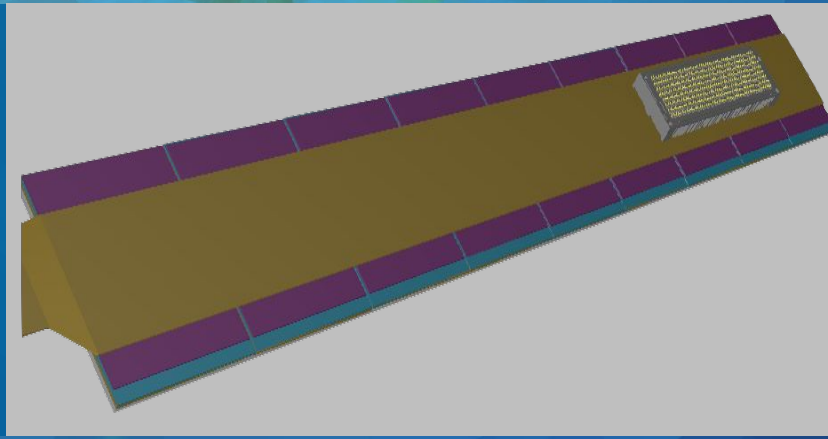
The ePIC Barrel Imaging Calorimeter

AstroPix Wafers, Modules, and Staves



Manoj Jadhav
Argonne National Laboratory

4th BIC In-person Workshop
April 09-11, 2025

Biographical Sketch

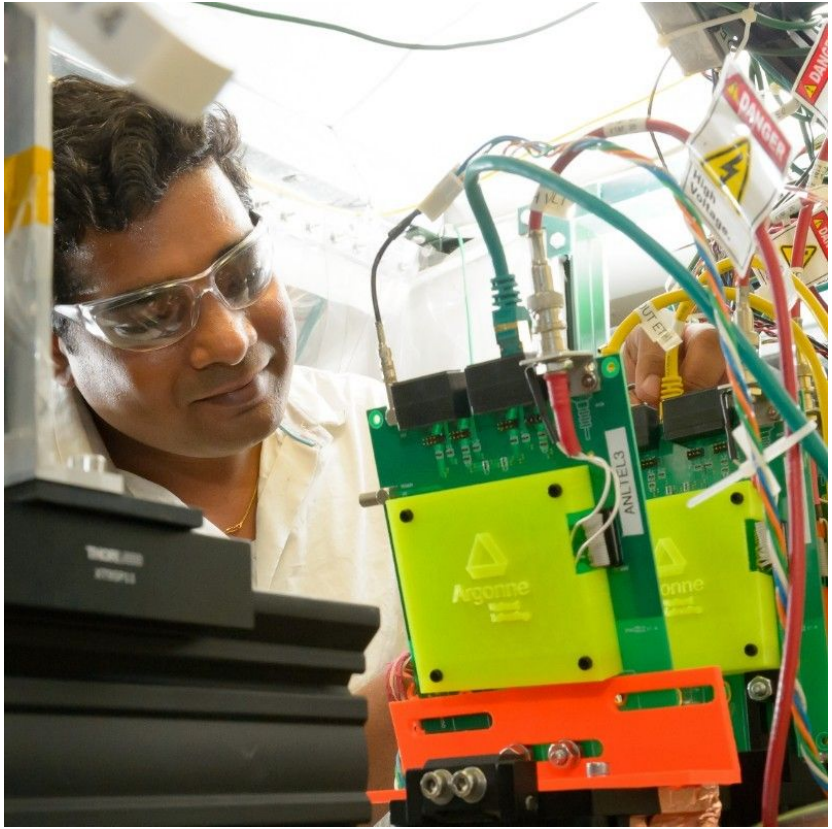
GTL - AstroPix Wafers + BIC Modules and Staves

Argonne Micro-Assembly Facility Technical Project Leader
High Energy Physics Division at
Argonne National Laboratory

Interest:
Silicon detectors R&D, UFSD-LGADs, CMOS-MAPS, Thin film detectors

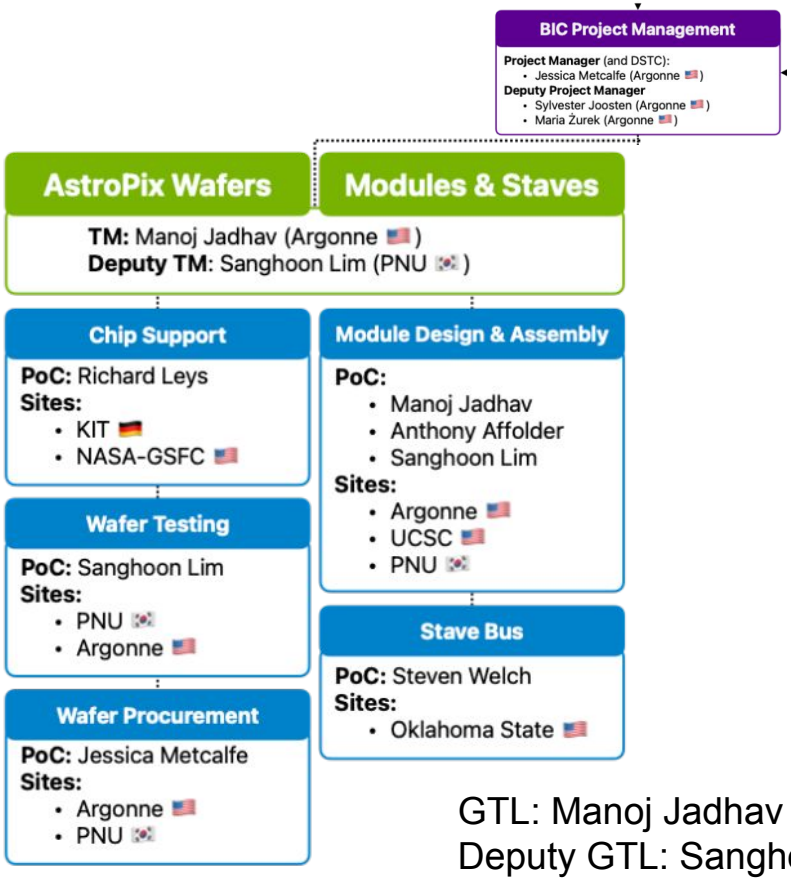
Collaboration:
BIC-ePIC
ITk Pixel Modules - ATLAS Inner Tracker
Tracker - ComPair2 and AMEGO-X - NASA

Past Experience:
Argonne Postdoc - Oct 2018 to May 2022
PhD - Indian Institute of Technology Bombay, India (ALICE Experiment)



Green Team

GTL - AstroPix Wafers + BIC Modules and Staves



GTL: Manoj Jadhav
Deputy GTL: Sanghoon Lim

Work Package Scopes:

- **Chip Support**
  - Chip design
  - Version 5 for PREP and Version 6 for Production
- **Wafer Testing**
  - QC procedure
  - wafer/chip QC
  - Wafer dicing and metrology
- **Wafer procurement**
  - wafer procurement
- **Module/Stave Design and Assembly**
  - assembly, loading, and QC procedure
  - Handling and carrier toolings
  - Module assembly and QC
  - Stave loading and QC
- **Stave Bus (actually Module Hybrid-PCB - AstroLinx)**
  - AstroLinx design and fabrication (v3 and v5)
  - Update to AstroLinx for Production (v6)
  - AstroLinx QC

Outline

Subtitle

- Test Article evolution - AstroPix versions, QC test stand, Module test article, readout PCB, Staves, handling and loading tools, QC procedure, assembly and loading procedure, production database

- Status overview - Ongoing activities on wafer/chip testing, Module and Stave Design, chip wirebonding and handling tools, readout PCB, 9chip board testing, assembly mockups

- PED/preliminary design(60%) phase & deliverables → August 2025
  - schedules, what is needed, and when

- PED/final design (90%) phase & deliverables → Spring/Summer 2026
  - detailed QC plan, preliminary production-like procedures (scaling)

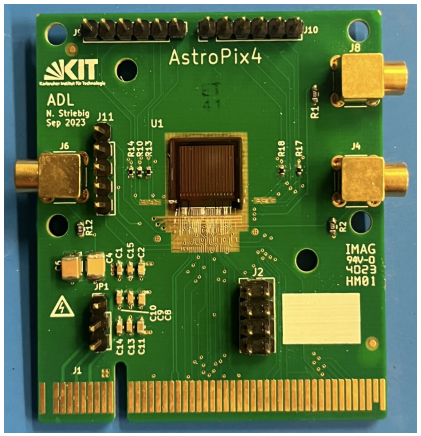
- Preproduction plans (PREP) (99%/100%)
  - practice of production

Test Article Evolution

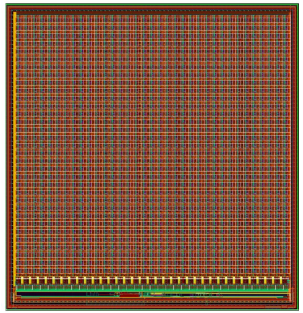
AstroPix

BIC PED
AstroPix v3 (1.87 cm × 1.96 cm)
First full size design
Pixel pitch: 500 µm
Pixel matrix: 35 × 35
Row/Column readout
0.88 mW/cm^2 analog, 12 mW digital
2.5 MHz timestamp, 200 MHz ToT

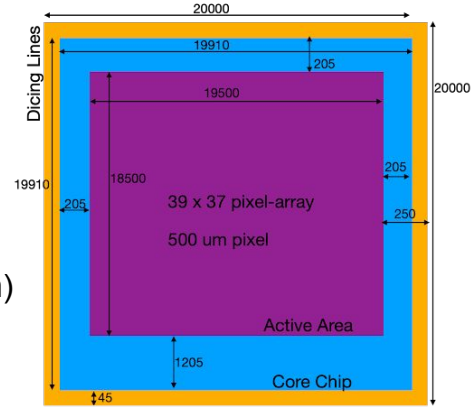
AstroPix v4 (1 cm × 1 cm)
Final design engineering run
Pixel pitch: 500 µm
Pixel matrix: 13 × 16
Individual pixel readout
0.96 mW/cm^2 analog, 3 mW digital
3 timestamps, 3.25ns time resolution
TuneDAC for pixel-by-pixel thresholds



BIC PREP
AstroPix v5 (1.87 cm × 1.96 cm)
Final design run
Pixel pitch: 500 µm
Pixel matrix: 36 × 34
Individual pixel readout
0.96 mW/cm^2 analog, 3 mW digital
3 timestamps, 3.25ns time resolution
TuneDAC for pixel-by-pixel thresholds



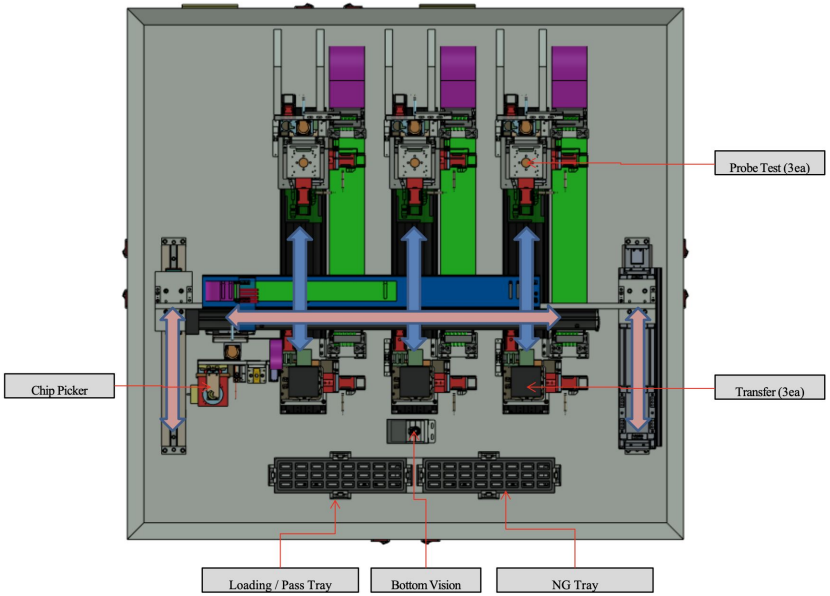
*Engineering run of v6 during PREP



BIC Final Chip Design
AstroPix v6 (2 cm × 2 cm)
Pixel pitch: 500 µm
Pixel matrix: 39 × 37
Individual pixel readout
2 mW/cm^2
3 timestamps, 3.25ns time resolution
TuneDAC for pixel-by-pixel thresholds

Test Article Evolution

Wafer/Chip QC Test Stand

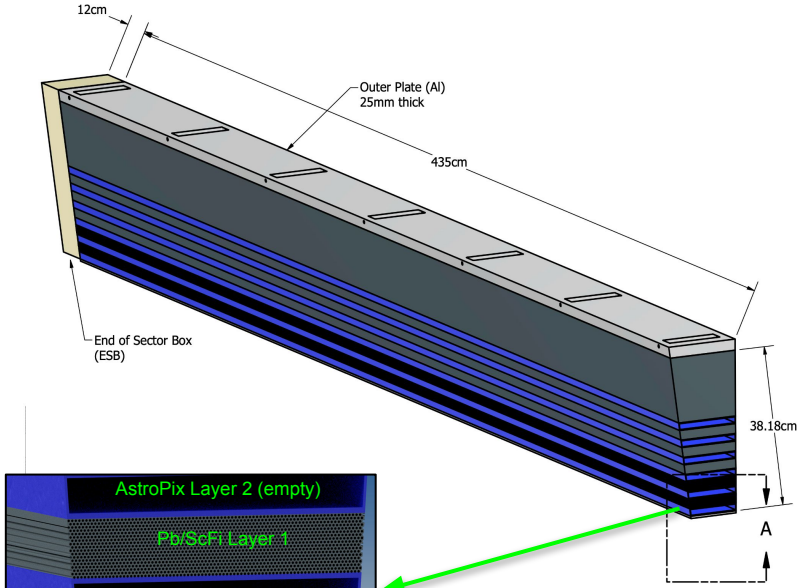


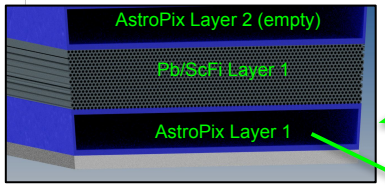
- Goal
  - Identify defective chips
  - Avoid rework and minimize efforts
  - Achieve best detector performance
- PED
  - Chip QC test stand
  - Design and fabricate probe card (v3)
  - Set initial QC procedure
  - Chip QC on 80 AstroPix chips (v3)
- Milestones
  - Commissioning of test stand
  - **Decision of Chip vs. Wafer QC**
  - QC of 80 chips required for PED
- PREP (Pre-Production)
  - Commissioning of wafer-prober/chip-teststand (at 2 sites)
  - Finalize wafer QC procedure and develop testing FW/SW
  - Establish production workflow for AstroPix chips delivery
  - Test QC on 7500 chips (125 wafers)

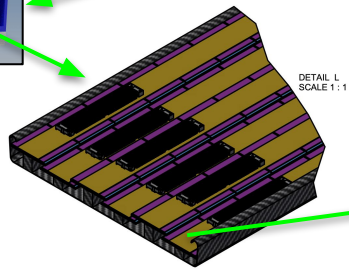
Test Article Evolution

Modules and Staves

48 sectors
192 Trays
56 Staves/sector
2688 Staves
32256 Modules



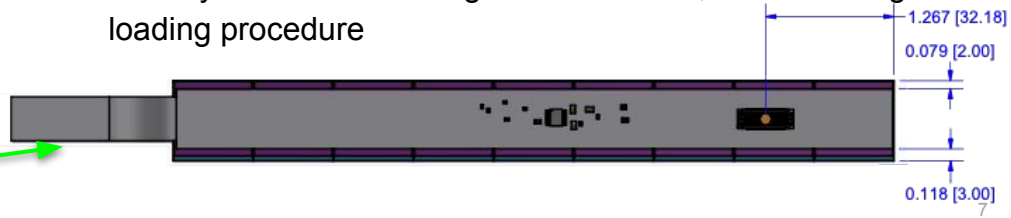




Goal:

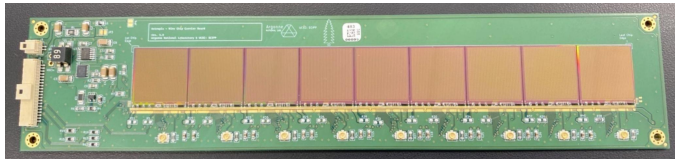
32256 Modules

- Four imaging layers in a Sector
  - ~435 cm active length
  - Total 48 Sectors
- Tray is a structure holding the AstroPix Staves for a single layer (217.5 cm long)
  - Tray consist of 6-7-7-8 Staves (x2) in a sector
- **Stave consist of 12 AstroPix Modules**
  - Module is an electrically testable elementary unit consist of **9 AstroPix chips** with Hybrid-PCB readout (~18cm)
  - Total 31104 Modules
- Total 279936 AstroPix chips will be used to build the imaging layers
- All Trays will be built using same Modules, standardizing the loading procedure



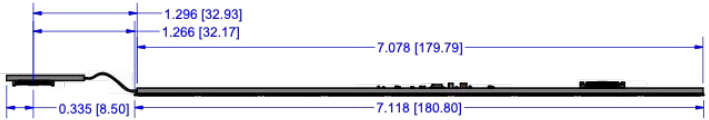
Test Article Evolution

Modules and Staves



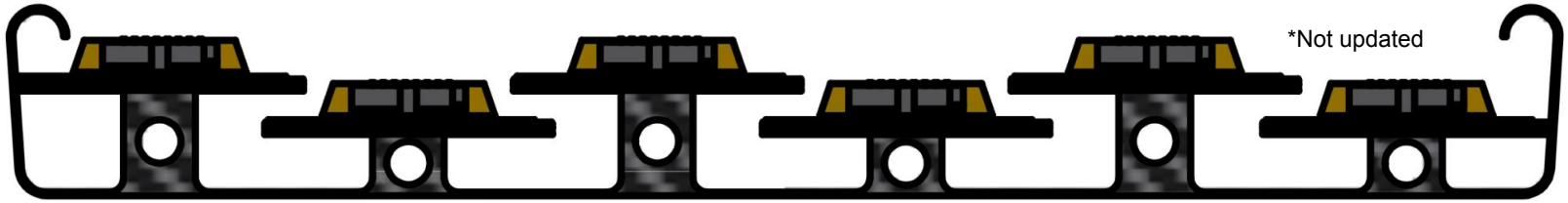
1.7 mm - Connector
1.7 mm - AstroLinx
0.1 mm - Glue
0.525 mm - AstroPix
0.1 mm - Glue
1 mm - Module Baseplate

Not Scaled



PED:

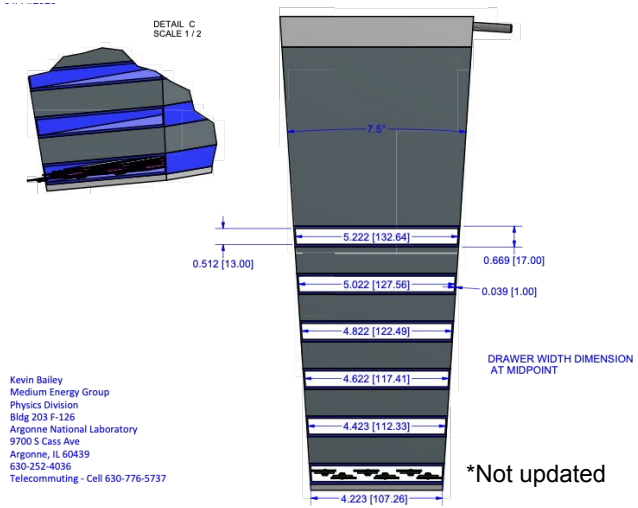
- Proof of principle: daisy-chaining
  - Quadchip board testing (talk by Bobae and Dan)
  - 9-chip PCB (Bobae's talk)
- Build and validate design concept - mechanical support test articles for Modules and stave loading (Sylvester's talk)
  - evaluate and update the design
- Develop Hybrid PCB for module readout (v3) - AstroLinx
- Module assembly mockups with dummy chips
- Module assembly (6 modules) with v3 chips
- Module QC initial procedure
- Load them on Tray through Stave railing
  - - Lanky teenage BCAL (Maria's talk)



*Not updated

Test Article Evolution

Modules and Staves



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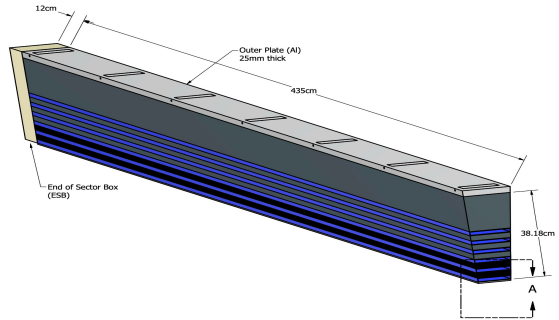
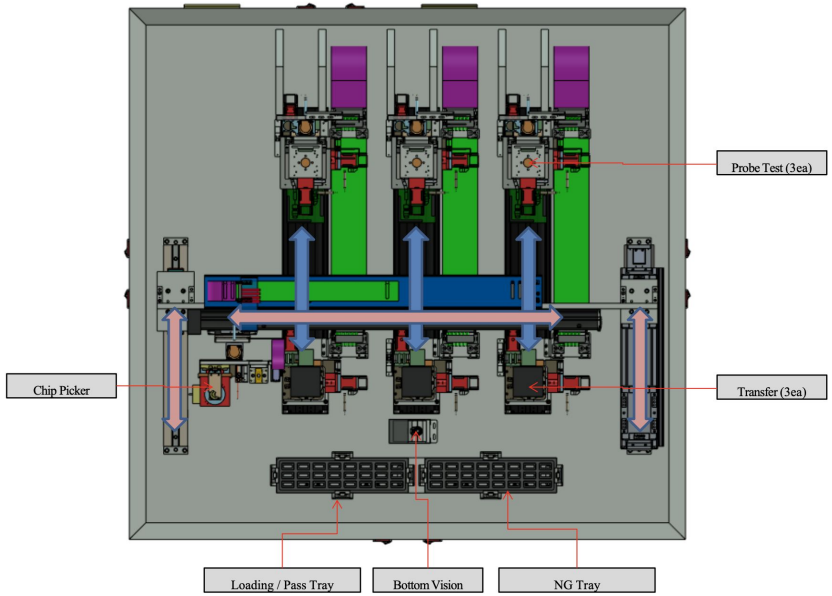


PREP:

- Building half sector (~217 cm)
  - all 6 layers of tracker (6+7+7+7+7+8 Staves)
  - Total 50 Stave - 600 Modules
- Finalize the assembly, loading, and QC procedure
- Update the Hybrid-PCB design for AstroPIx v5
- Design and fabricate handling/carrier tools
- Commissioning of pick and place machine for automation of assembly
- **Assembly and Loading procedure**
  - assembly of 600 modules at 3 sites
  - loading modules to Tray
  - QC
- Development of electric and mechanical test articles for AstroPix v6 (final design)
  - Module assembly (v6 engineering run)
  - Stave loading and QC

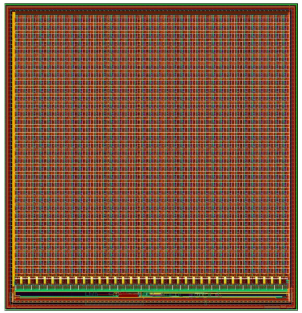
Status Overview

AstroPix Wafers and QC



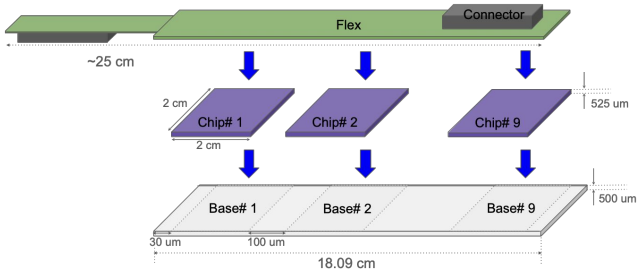
- AstroPix v5 is ready and waiting for submission (engineering run)
- Final chip (v6) dimensions is 2 cm x 2 cm
- Test stand design finalized at PNU, - (Sanghoon's talk tomorrow)
  - procurement under process
  - v3 probe card design in progress
- In discussion with vender for wafer prober estimates
- v3/v4 chip testing to set QC procedure

AstroPix v5



Status Overview

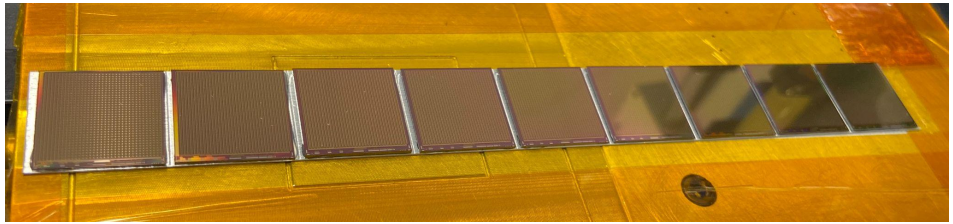
Module and Staves



Not Scaled

1.7 mm - Connector
1.7 mm - AstroLinx
0.1 mm - Glue
0.525 mm - AstroPix
0.1 mm - Glue
1 mm - Module Baseplate

- **Module design**
  - Base Plate (Aluminum)
  - Nine AstroPix Chips
  - Hybrid PCB
- **Mechanical design**
  - Finalized base plate design
  - Topic of discussion - locking mechanics
  - Initial test article under fabrication
- **Mechanical loading procedure**
  - Glass dummies under fabrication
  - Ongoing discussion on adhesive selection and glueing procedure
  - Wire-bonding procedure under discussion



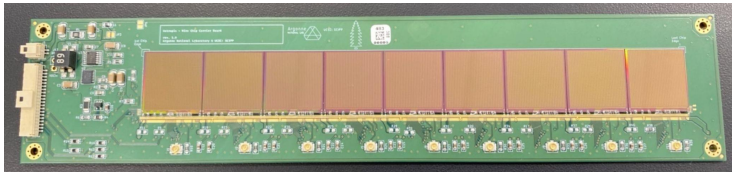
Status Overview

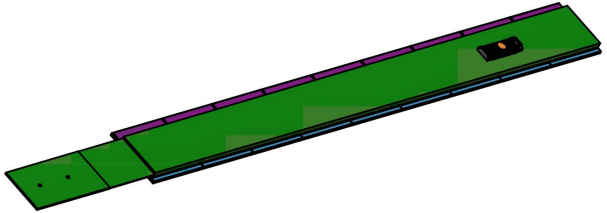
Module and Staves

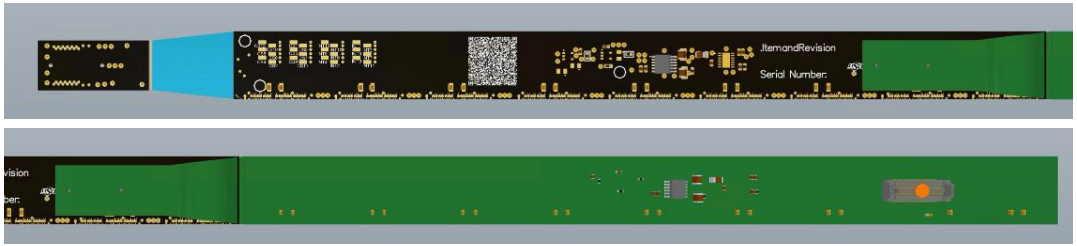
Not Scaled

1.7 mm - Connector
1.7 mm - AstroLinx
0.1 mm - Glue
0.525 mm - AstroPix
0.1 mm - Glue
1 mm - Module Baseplate

- **AstroPix testing**
  - AstroPix v3 will be used for PED
  - ongoing quadchip and 9chp board testing
- **Hybrid PCB Design (AstroLinx)**
  - Schematic completed
  - work ongoing on layout design
  - Will be presented tomorrow by Blake



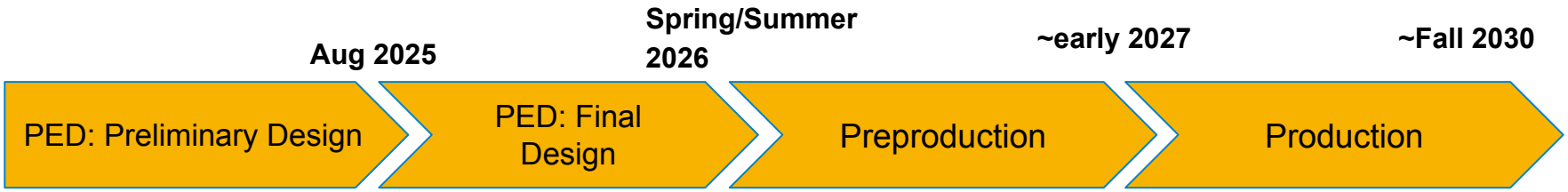




More in talk by Blake and Greg (OSU)

PED Design and Pre-production Plans

Milestones - Wafer QC

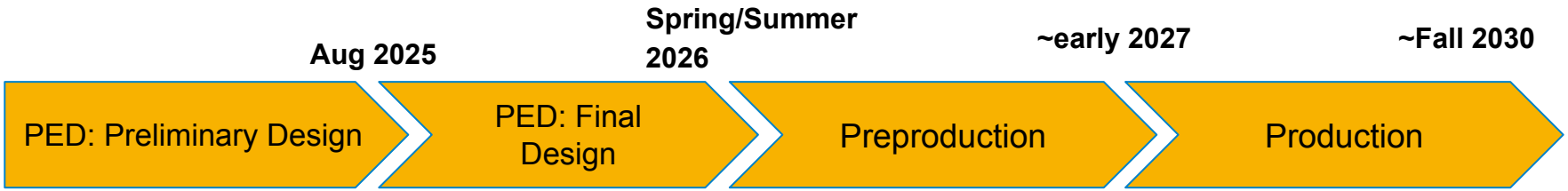


- *Fully commissioned chip test stand at PNU - July 7, 2025*
- QC testing of priliminary tests of AstroPix v3 chip - July 15, 2025
- *AVAIL: wafer vs. chip testing decision - July 21, 2025*
- *QC tested v3 chips for Module PED - Aug 20, 2025*

- *AstroPix v5 delivery - July, 2026*
- Wafer/chip prober - July, 2026
- *Wafer QC procedure - Apr, 2026*
- *Wafer QC on first preproduction v5 wafer - Aug, 2026*
- *Start receiving diced QC'ed chips - Sep 2026*
- *AstroPix v6 for Production - Aug 2027*

PED Design and Pre-production Plans

Milestones - Modules and Staves



- *Proof of Principle Daisy-Chained 9-chip Module PCB for PDR - 28 July, 2025*
- AVAIL: 3 fully QC'ed 9-chip PCB board - Aug 25, 2025
- *Final sign-off on the AstroLinx v3 design - May 15, 2025*
- *First QC'ed v3 module - July 29, 2025*

- *Updated test articles (Mechanics) - Dec, 2025*
- v3 Module test articles (6 Modules) - Mar 2026
- *v3 Module loading on the Stave test articles Lanky-Teenager-BIC - Apr 2026*

- *Handling and Carrier tools ready for preproduction - July, 2026*
- Review AstroLinx PCB v5 - Oct 2025
- *REQD: Start receiving QC'd v5 AstroPix chips - Oct 2026*
- *Gantry system commissioned - June 2026*
- *Final Production pipline defined - Aug 2026*
- *Review of QC procedure - Dec 2026*
- *Start receiving QC'ed v5 modules - Dec 2026*
- *Preproduction phase 1 assembly completed (v5 chips) - Jan 2027*
- *Finish Loading of Staves - Feb 2027*
- *AVAIL: Remaining Trays ready for System Testing - May 2027*

BACKUP

AstroPix Coverage

Active area of the imaging layers

- AstroPix chip size = 2 cm × 2 cm
- **Active area = 1.95 cm × 1.85 cm**
- Total Sector length = 435 cm
- Length to cover with single Stave = 217.5 cm
- AstroPix chip + gap = 2.01 cm
- Number of chips required = 217.5/2.01 = 108.21

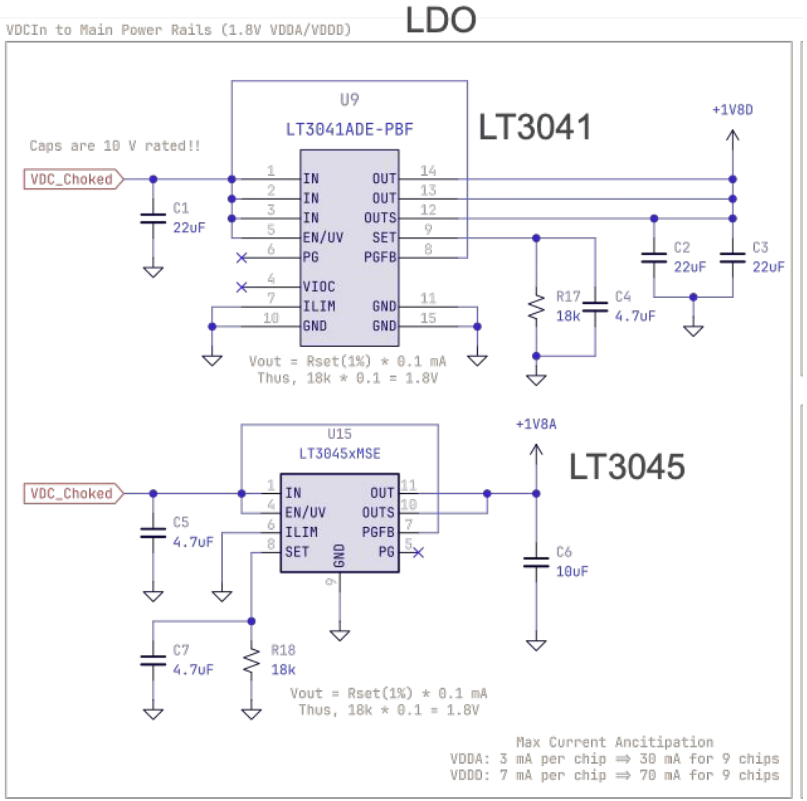
- 12 Module with 9 chips = **108 AstroPix Chips**
- Length of the Module = 9*2.01 = **18.09 cm**
- Length of the Stave = 9*2.01*12 = **217.08 cm**
- Length of Imaging Sector = **434.16 cm**

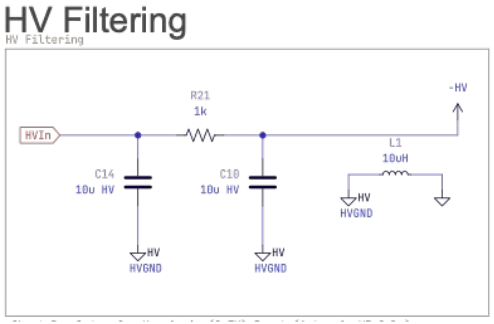
Inactive area percentage along Stave = **2.99%**

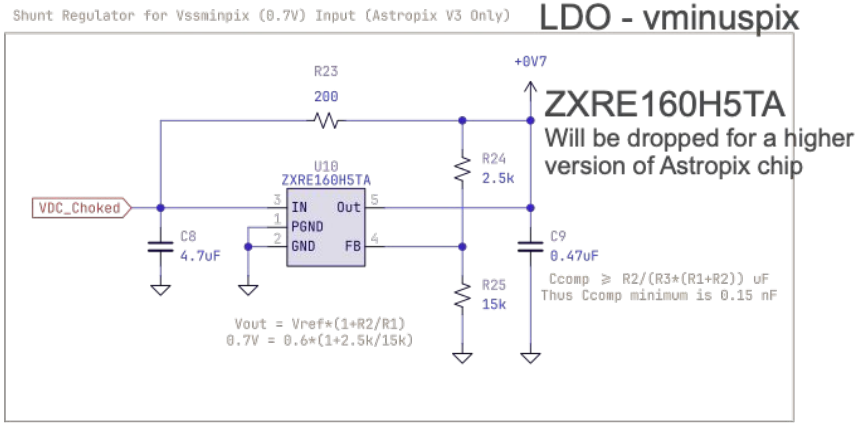
Transverse Coverage of imaging layers

	Length (mm)		Overlap or Inactive (mm)	Overlap/Inactive per Stave (mm)	Overlap/Inactive per Gap (mm)	Inactive (%)
1	107.257	6	4.243	0.707	0.8486	0.47
3	117.411	7	12.589	1.7984	2.0982	0.43
4	122.488	7	7.512	1.073	1.252	0.41
6	132.642	8	15.858	1.982	2.2654	0.38

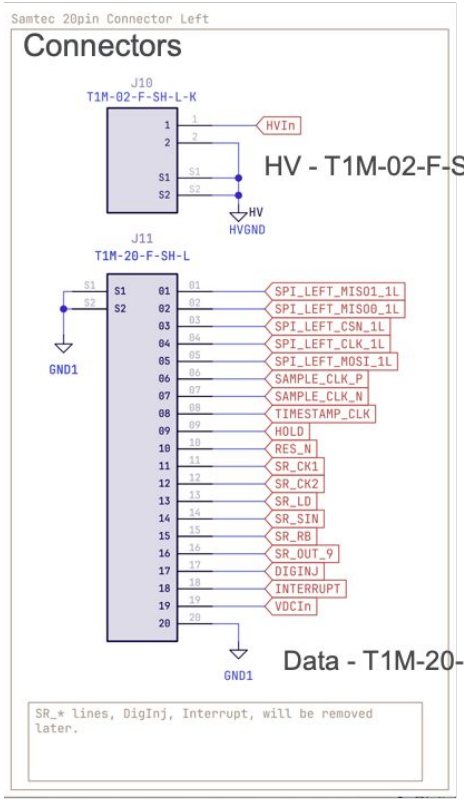
AstroPix Module Test PCB







AstroPix Module Test PCB



List of I/O		
	V3	V5 (Not Final - need in)
Power	HVin	HVin
	HV GND	HV GND
	VDCIN	VDCIN
SPI	MISO0	MISO0
	MISO1	MISO1
	CSN	CSN
	CLK	CLK
	MOSI	MOSI
Sample Clk	SAMPLE_CLK_P	SAMPLE_CLK_P
	SAMPLE_CLK_N	SAMPLE_CLK_N
Shift Register	SR_Ck1	
	SR_Ck2	
	SR_LD	
	SR_SIN	
	SR_RB	
	SR_OUT	
Other	DIGINJ	
	INTERRUPT	
	TIMESTAMP_CLK	TIMESTAMP_CLK
	Hold	
	RES_N	