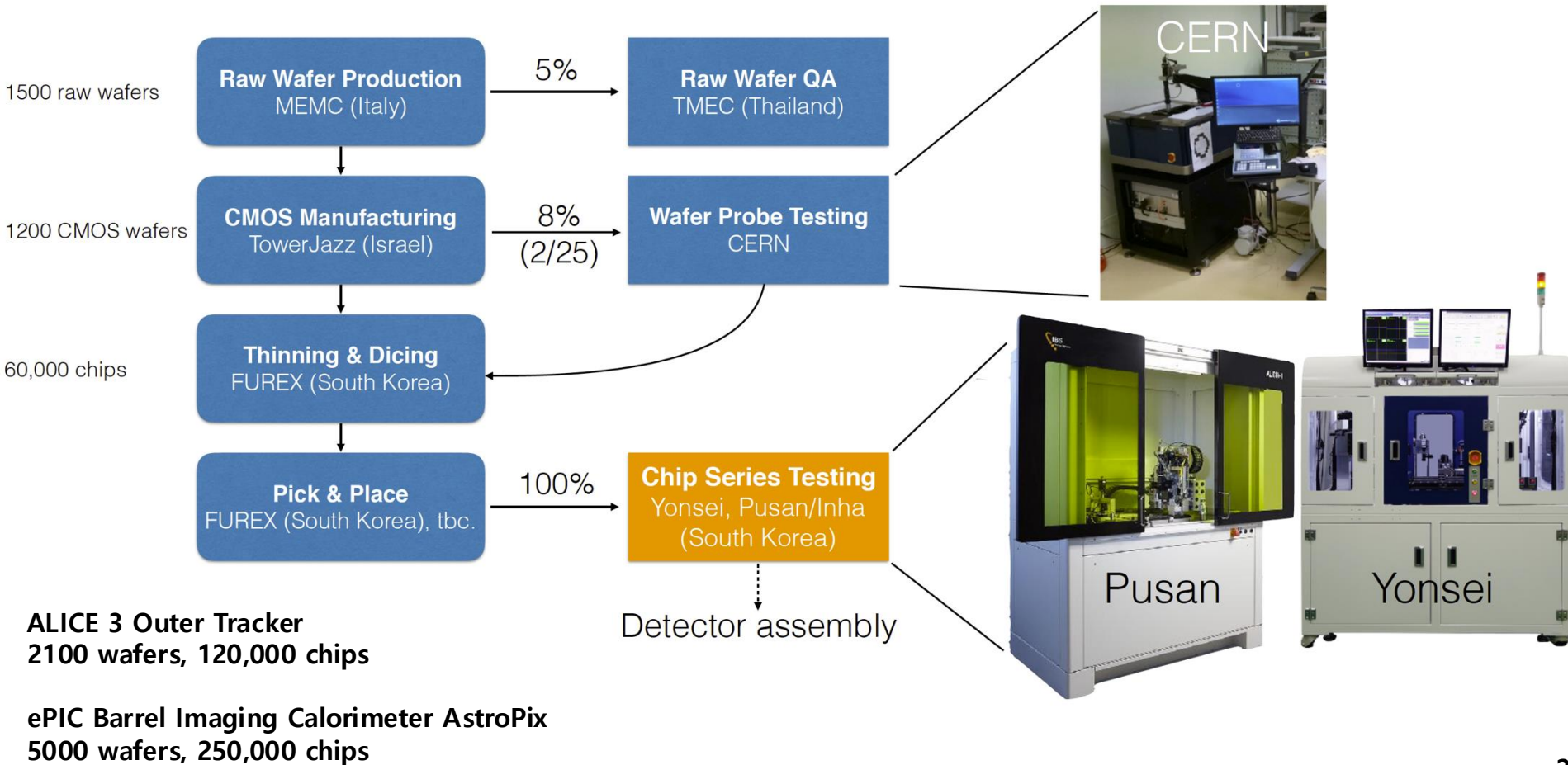


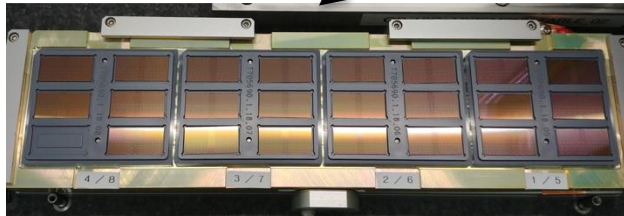
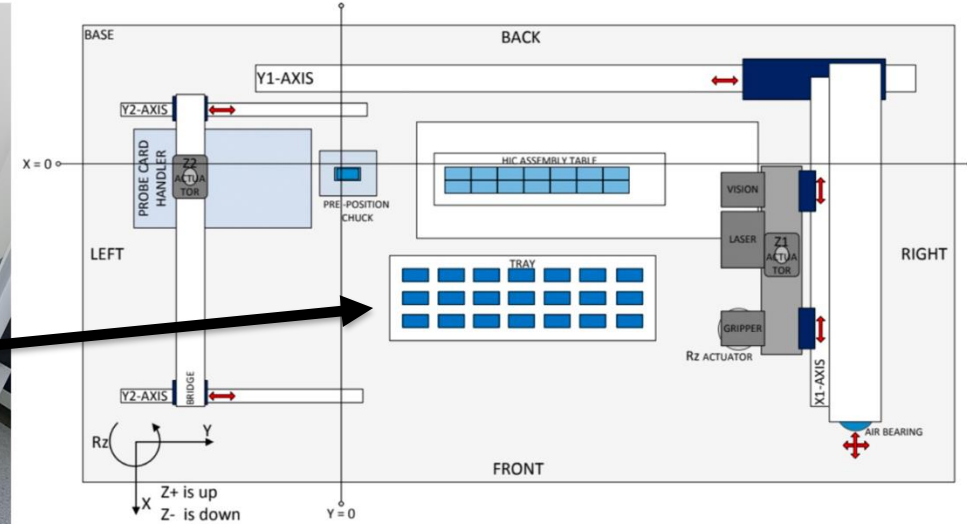
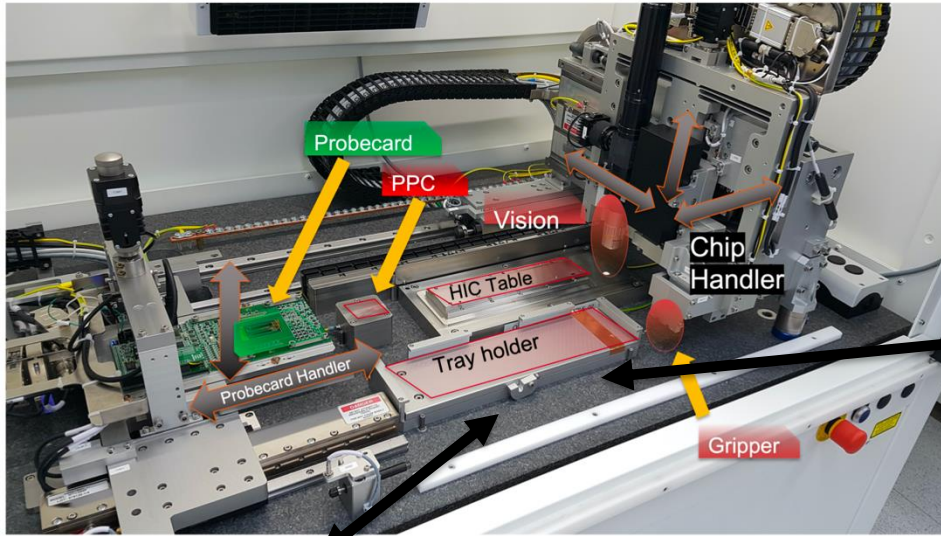
# **Wafer/Chip testing Progress/Plans**

**Sanghoon Lim**  
**Pusan National University**

# Overview of chip production and test for ALICE ITS2

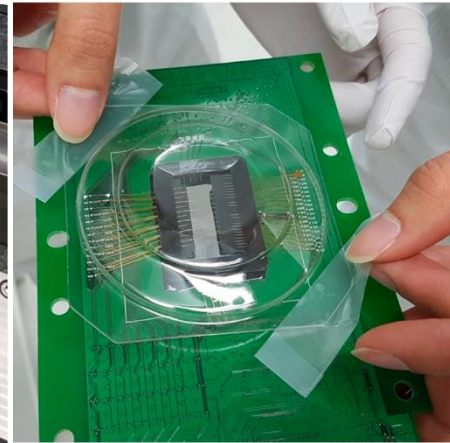
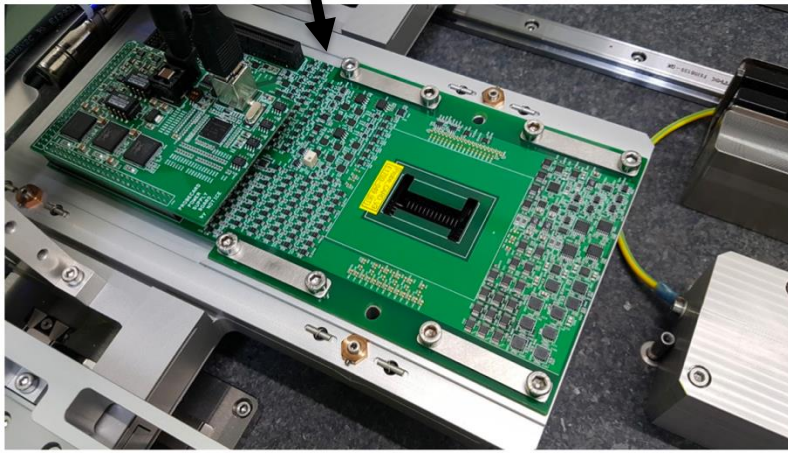
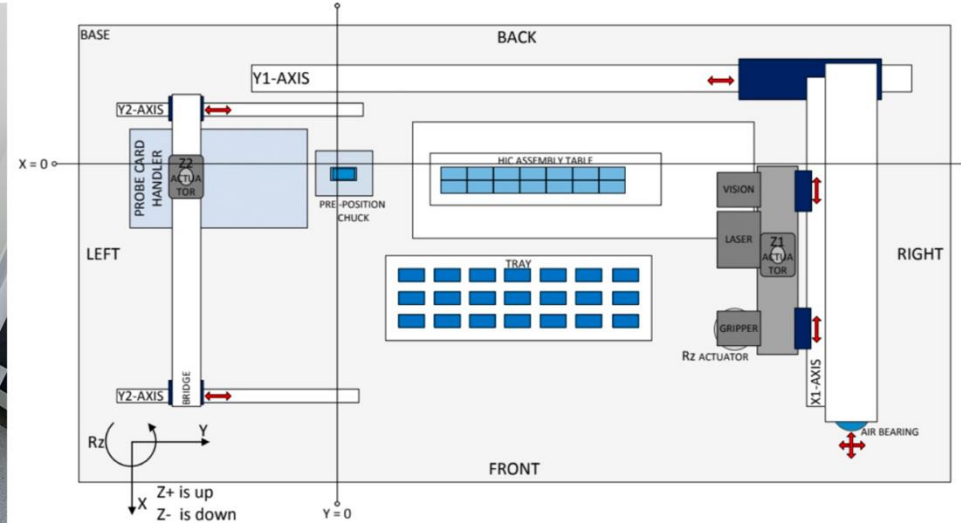
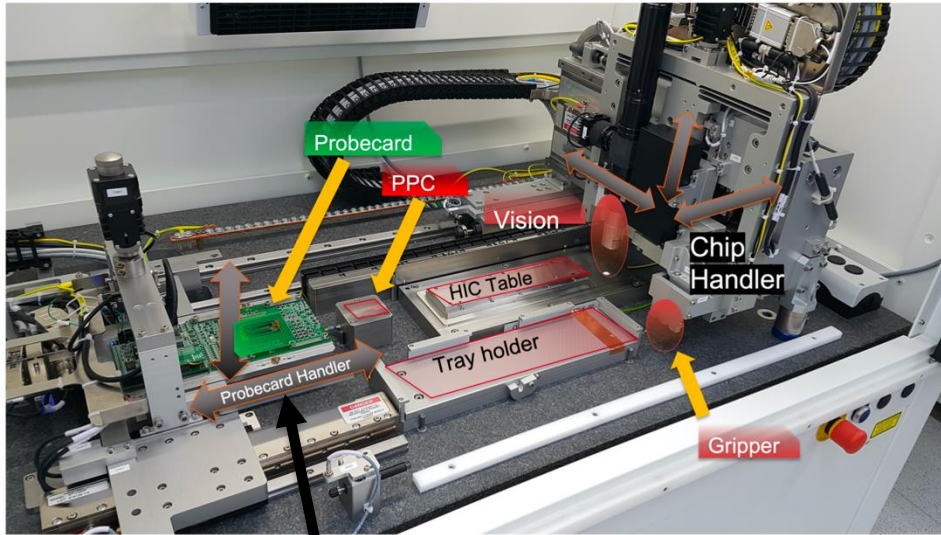


# Chip test machine (ALICE ITS2, ALICIA)



- After post-processing, sensors are contained in waffle packs and shipped to the testing facilities (PNU, Yonsei)
- The barcode on the waffle pack to keep track of wafer ID and fabrication run...
- After testing, chips are shipped to the assembly sites

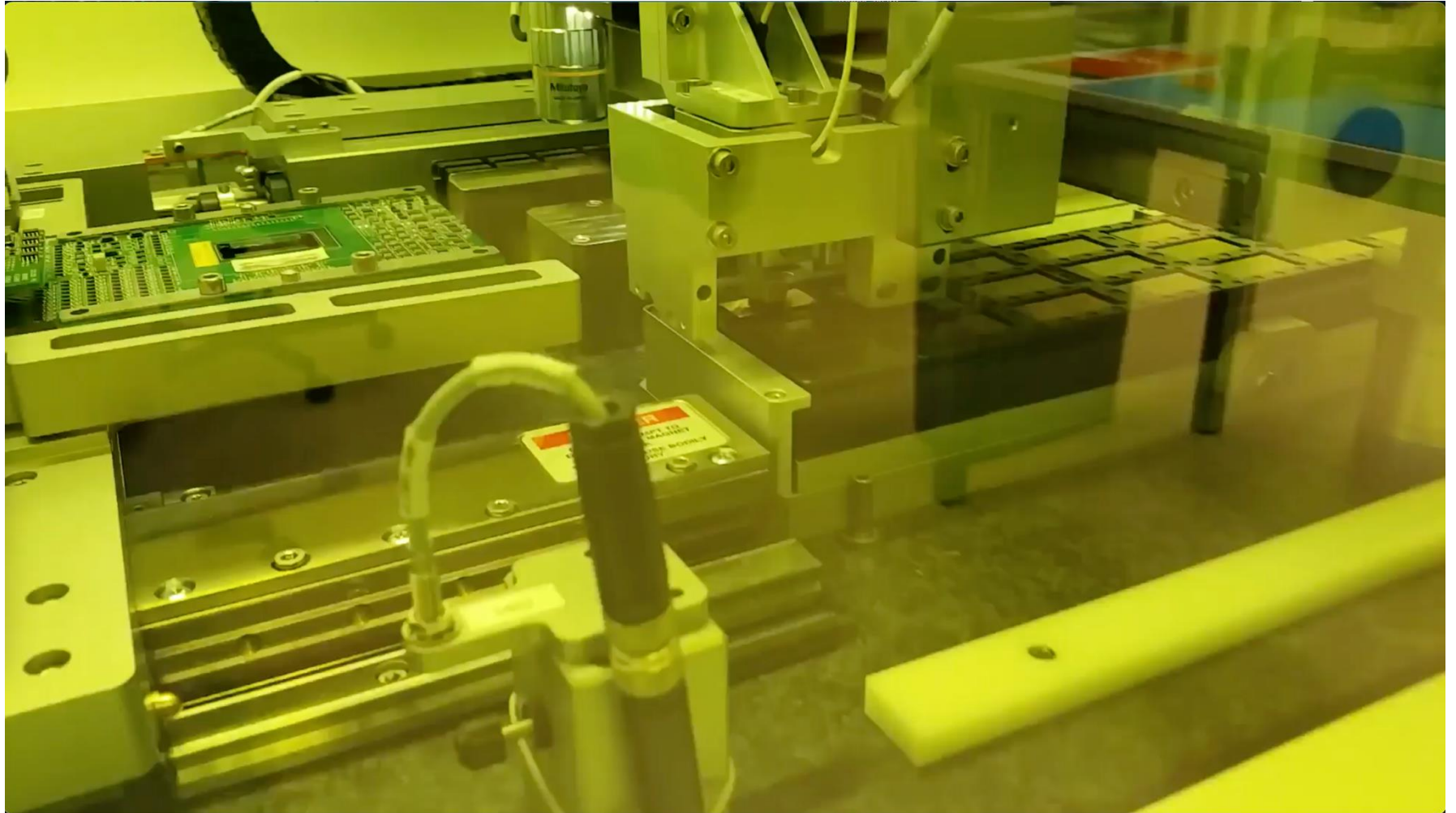
# Chip test machine (ALICE ITS2, ALICIA)



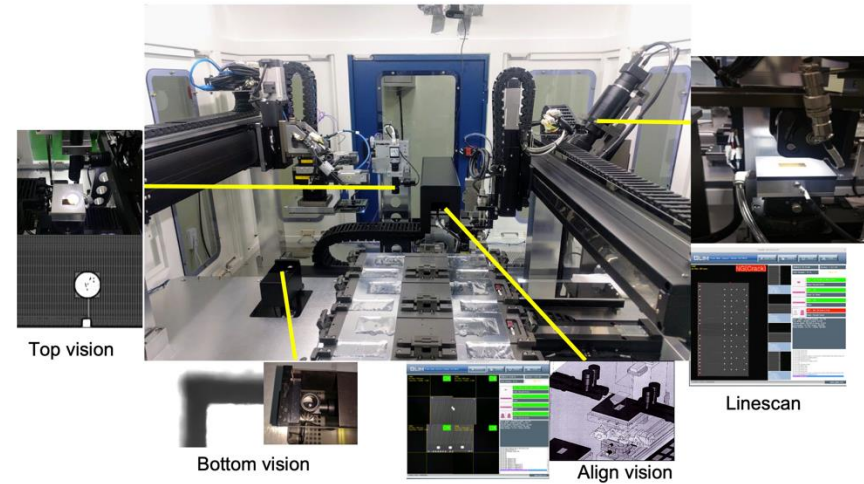
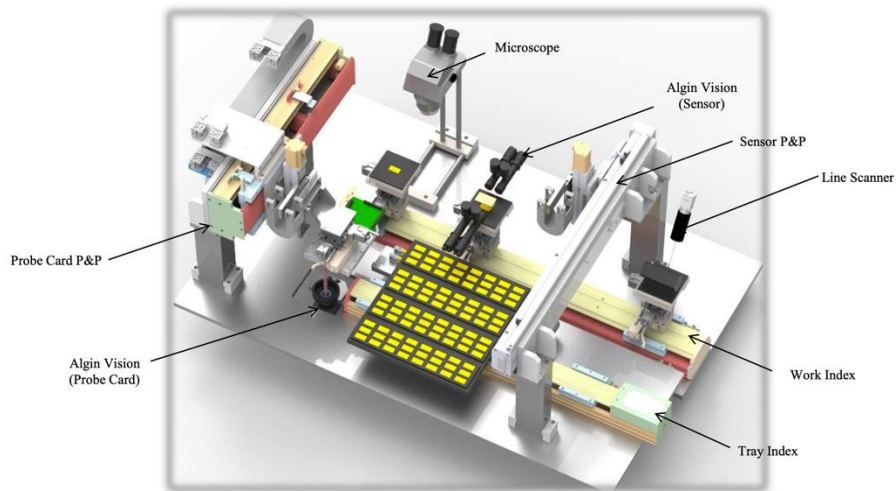
## ALPIDE single-chip test bench



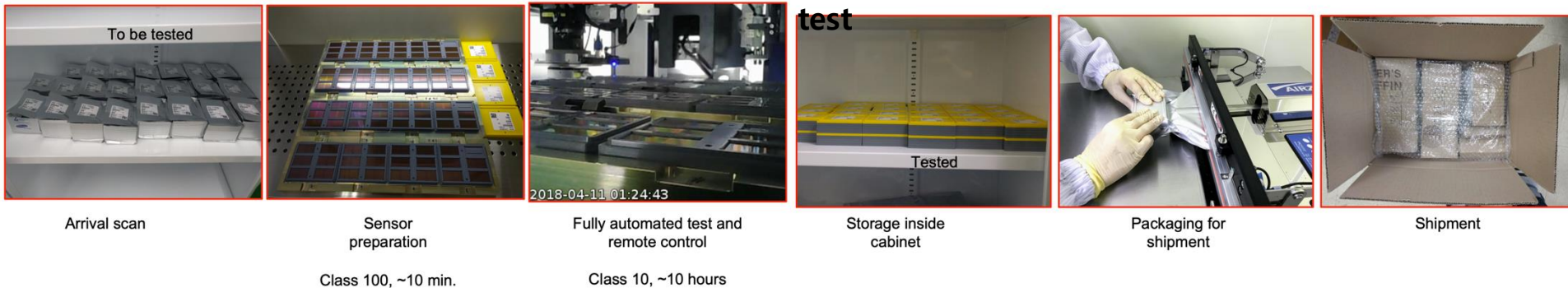
# Chip test machine (ALICE ITS2, ALICIA)



# Chip test machine (ALICE ITS2, COREA-YS-01)

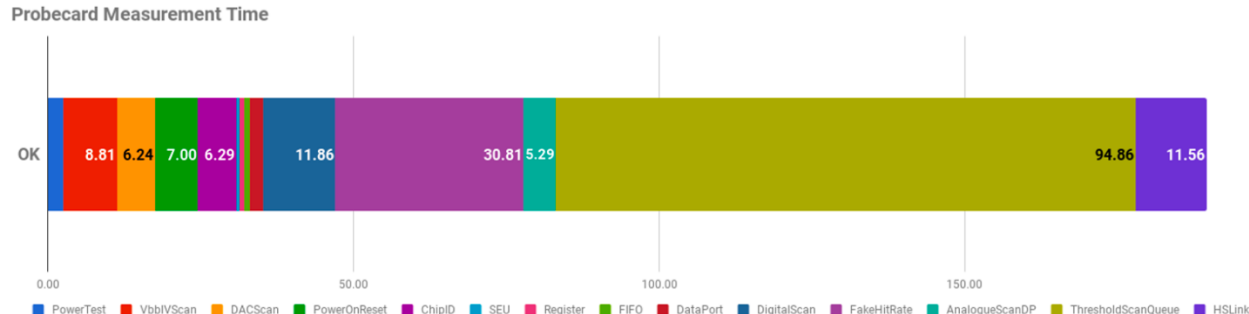


## A simpler version of the machine dedicated to chip test

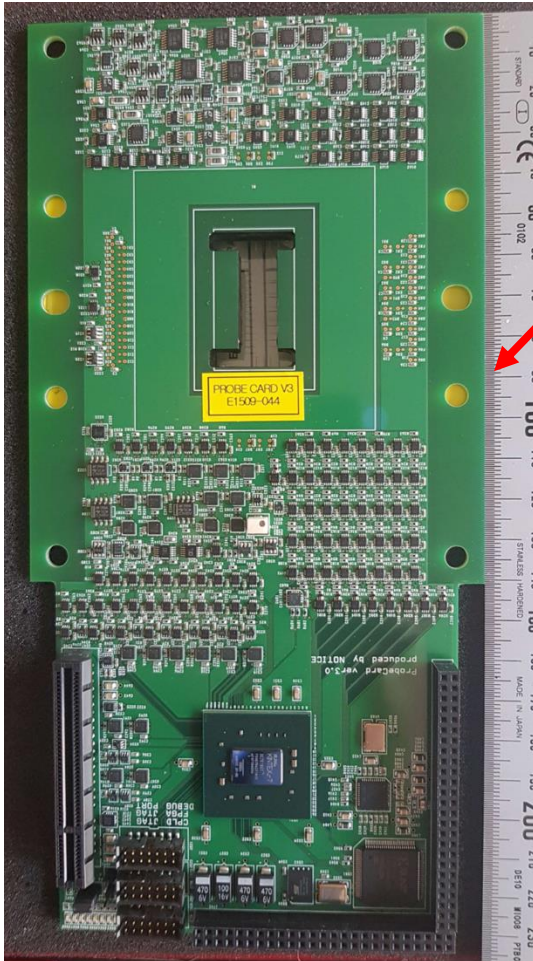


# Chip test procedure (ALPIDE)

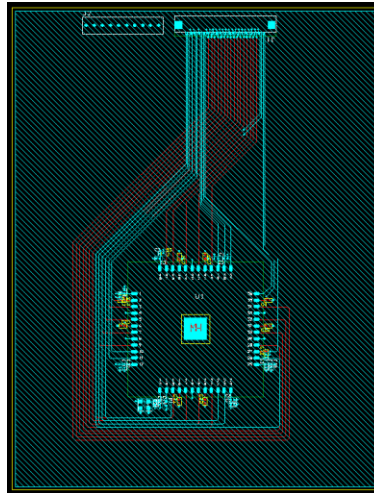
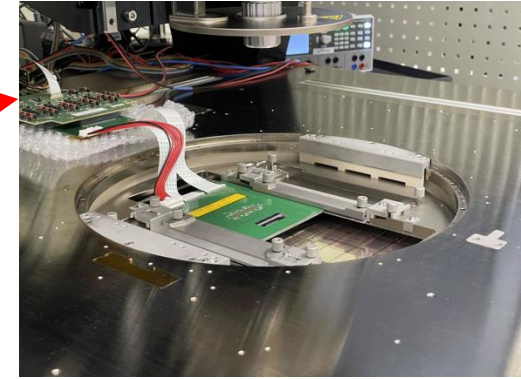
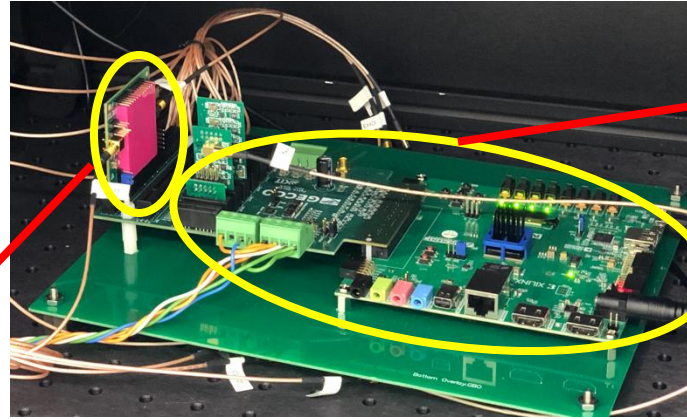
- **Powering test:** just power on/off
- **V<sub>bb</sub> I-V test:** apply the reverse substrate bias from 0 V down to -6 V
- **DAC scan:** verify that each DAC is working by scanning through all its code words
- **Power-on reset test:** check the functionality of the power-on reset
- **SEU check:** monitor the SEU counter and the flag bits on idle operation
- **Register test:** check all registers by writing and reading back to find stuck bit
- **FIFO test:** check all the generated memory blocks
- **Data port test:** verify its functionality to send quasi-static patterns in case of the readout test failure
- **Digital scan:** inject single hits directly into the in-pixel memories and read back
- **Fake hit rate:** measures the number of noisy pixels and faulty front ends
- **Analog scan DP:** exercise the analog front-end and the full readout chain of ALPIDE
- **Threshold scan:** test all analog front-ends/pixels by using analog pulse injection
- **High-speed link check:** check its functionality



## Probe card for AstroPix v3



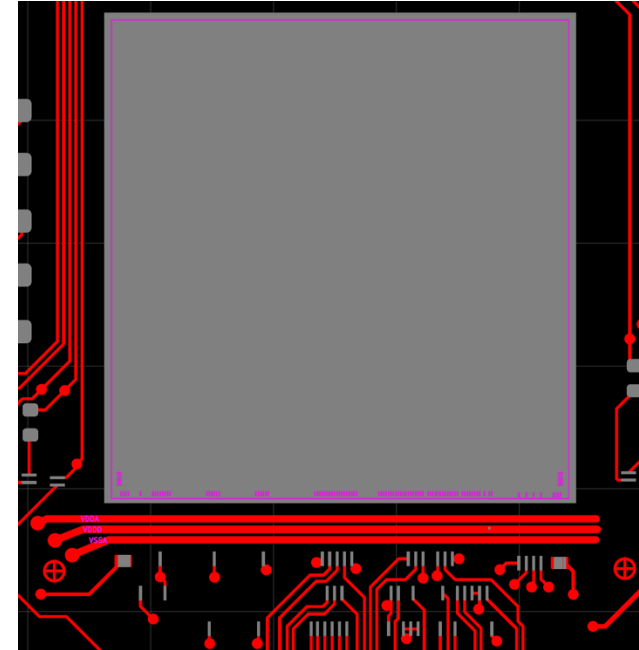
Probe card for ALPIDE (ITS2) Probe card for babyMOSS (ITS3)



- Initial version for AstroPix v3:  
a simple version for the carrier card only
- Considering the same dimension as the ITS2  
probe card to utilize the ALICIA machine for the  
initial test
- GECCO and FPGA development boards can be  
connected with flexible cables
- In addition, a circuit to check needle contacts  
should be added

## Probe card for AstroPix v3

- Connection with a flexible cable has been tested for the test beam at KEK (2025 March)  
Quite noisy when using a cable longer than 15 cm
- Working with a PCB manufacturer to design a probe card  
Convert the v3 chip carrier board design file from Kicad to Orcad  
Re-distribution of bonding pads in the PCB for needles



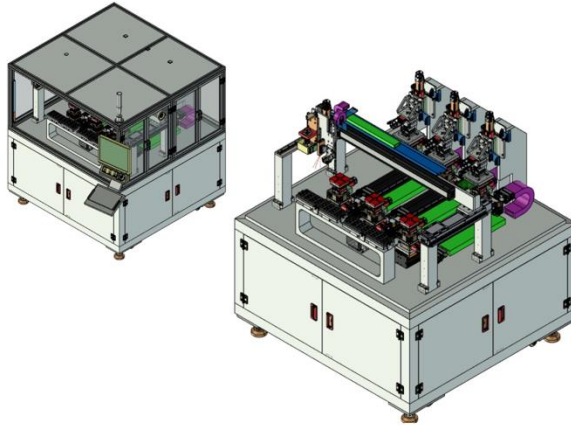
# Development of test system of AstroPix in Korea

- Developing a multi-line single-chip test system with C-ON tech
- Depending on the test procedure and time, one chip handler can cover multiple test stations  
Initial design for the prototype machine with three stations

## Introduction to Equipment

### Description

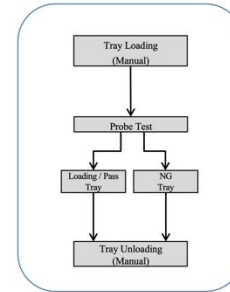
- Probe Test System
- Tray Loading : Manual
- Probe Test Motion : Z Axis - Servo Motor
- Chip Picker Motion : X,Y,Z Axis - Servo Motor
- Transfer Motion : Y Axis - Servo Motor
- Vision : Dispensing Align Top/Bottom Vision
- Main Equipment Size : 1600(W) x 1500(D) x 1700(H)
- Power : 220V 1P 60Hz



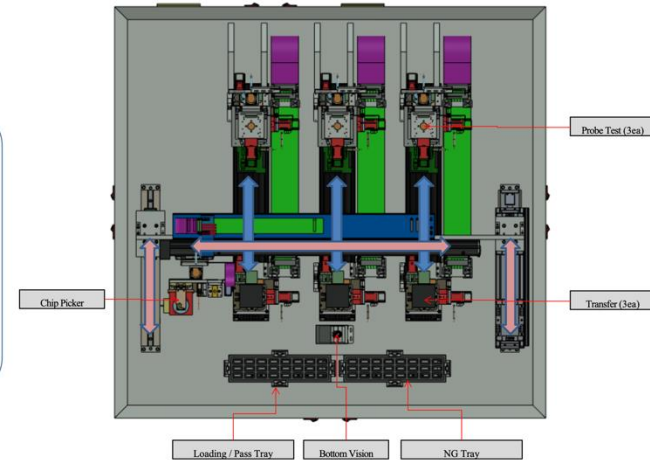
C-ONTECH  
(주) 에이텍

## Process Flow

### Process Flow



Confidential

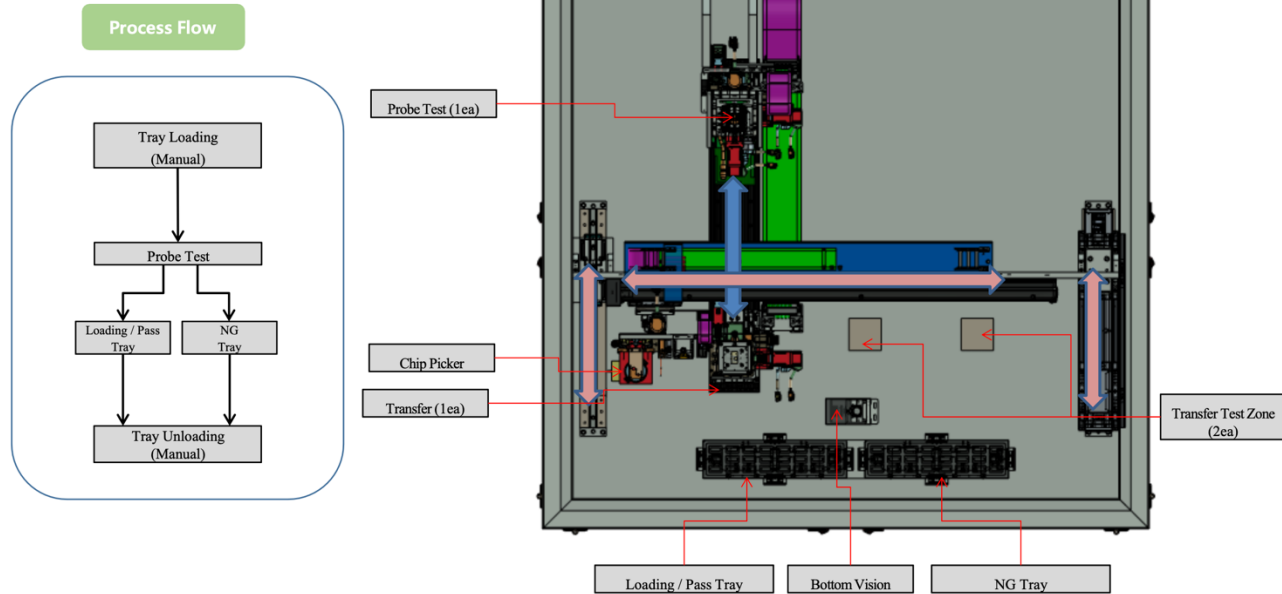


C-ONTECH  
(주) 에이텍

# Development of test system of AstroPix in Korea

- A machine production with a single-line will be started soon

## Process Flow (B TYPE)



Confidential

CONTECH  
(주) 컨텍

# Wafer prober for ALICE ITS3

- Wafer testing system for ALICE ITS3 at CERN

