4th BIC In-person Workshop, Apr 9, 2025

9-Chip PCB Testing

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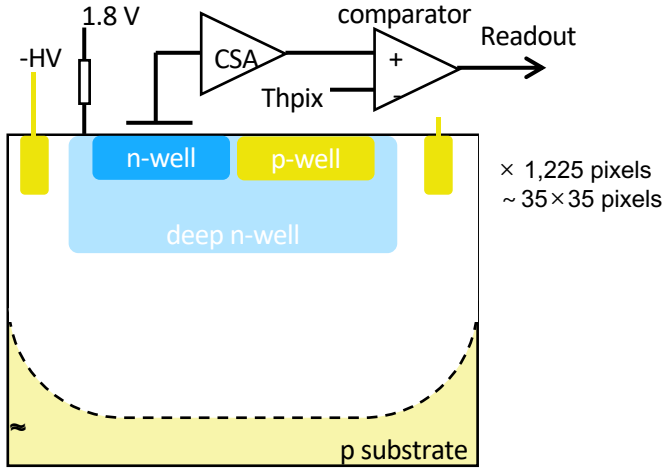
Contents

Overview of AstroPix

High-voltage CMOS monolithic active pixel sensor (HV-CMOS MAPS)

- based on ATLASpix3 [arXiv:2109.13409]
- Originally developed for space-based missions, specifically for gamma-ray astrophysics
  - NASA AMEGO-X space mission and ComPair2 project
- Use as the imaging layers in the barrel imaging calorimeter for nuclear physics applications.



https://arxiv.org/abs/2407.05947

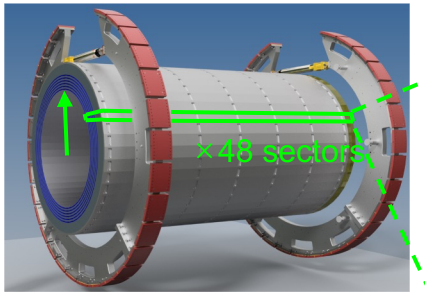
- **Astropix v3 single chips**
  - 2×2 cm^2 -size with 35 × 35 pixel matrix
  - 500 µm pixel pitch, 725 µm thickness
  - Time stamp clock: 8-bit at 2.5 MHz (400 ns)
  - ToT (Time over Threshold) clock: 12-bit at 200 MHz (5 ns)
- **Astropix v4 single chips**
  - 1 x 1 cm^2 -size with 13 × 16 pixel matrix
  - 500 µm pixel pitch
  - Individual pixel readout
  - 3 timestamps, 3.25 ns time resolution
  - TuneDAC for pixel-by-pixel thresholds

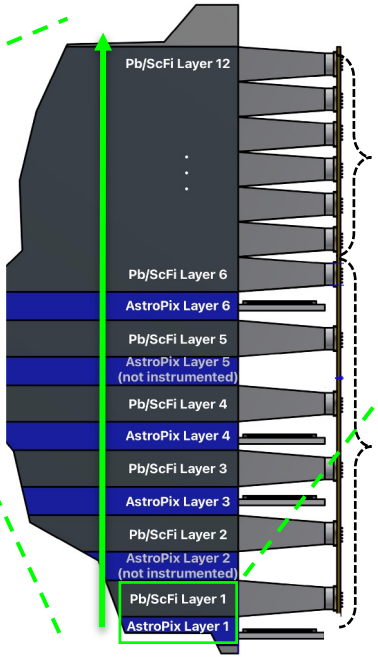
AstroPix v3 - Single Chip

AstroPix v3 - Quad Chip

AstroPix v4 - Single Chip

Structure of Imaging Layer with AstroPix in BIC

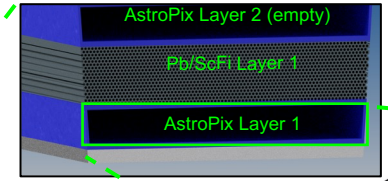


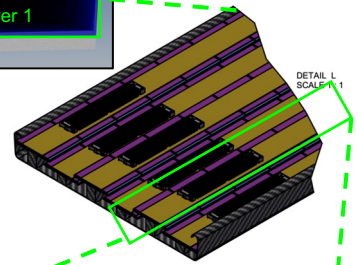


Large **back section of Pb/ScFi**

4(+2) imaging layers with AstroPix sensors interleaved with **5 Pb/ScFi layers**

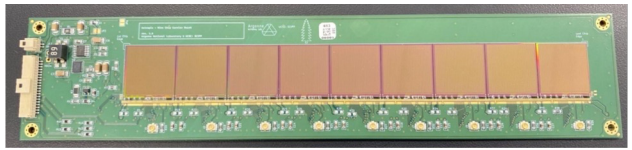
Astropix Layer + Pb/SciFi Layer





Tray
Structure holding the AstroPix staves for a single layer (217.5 cm long).
Consists of 6-7 staves.

Stave
Consists of 12 modules.



AstroPix Module
9 AstroPix sensors daisy-chained together on PCB.

- 4 imaging layers in a Sector
  - Total 48 Sectors
  - 435 cm active length
- Total 279,936 AstroPix chips will be used to build the imaging layers in BIC.
  - Total 31,104 modules
- All Trays will be built using same modules, standardizing the loading procedure
- The first prototype module, built with v3 sensors for initial testing.

AstroPix 9 Chip PCB Test Module

Similar design to quad chip board (no busbar required)

Nine AstroPix Chips, **Daisy-chained on the Module**

Each Module plugs into its adjacent Module

All Modules will be **controlled by the End-of-Tray Card**

The broadcast commands/data readout through **SPI protocol**

One main HV line (~500V) and one (or 2) LV line (3.3V)

Voltage Regulators (LDO) to regulate power on each Module

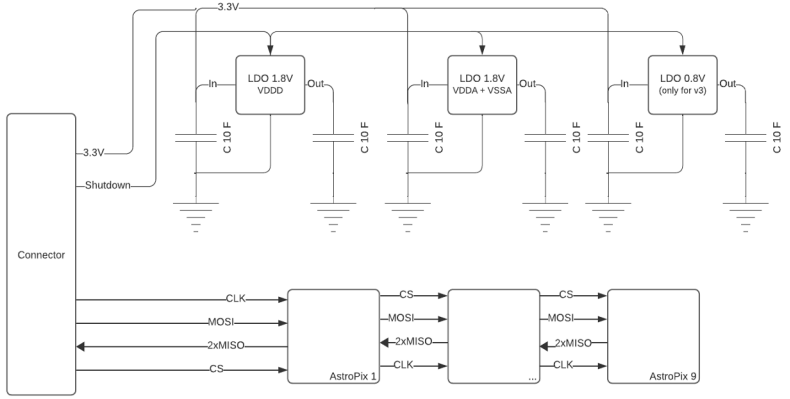
- Analog and digital power of 1.8V at Module

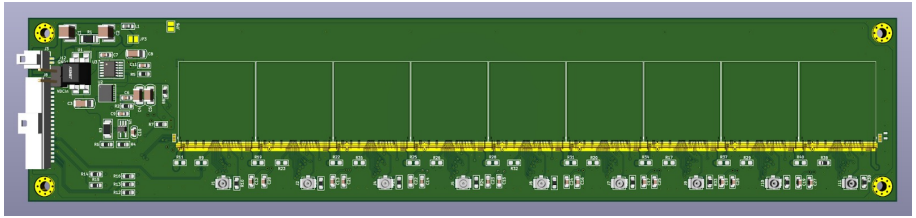
4 **differential data SPI (Clk, MOSI, 2MISO)** common for stave

One **single-ended Chip-select SPI** per Module

Approximately **24 I/O + GND** Pins per Stave

- Exploring connector options (radiation hard, smaller size)





Testing Setup

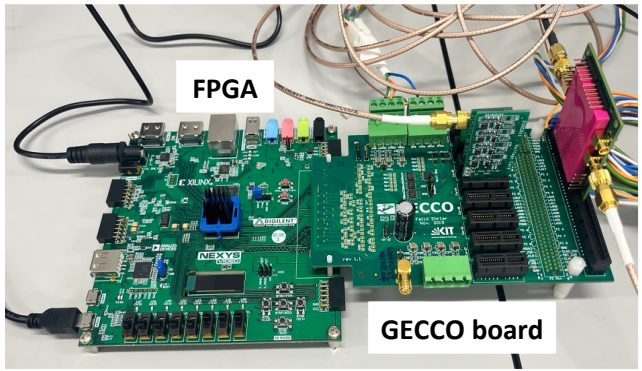
Available Astropix and setup at ANL

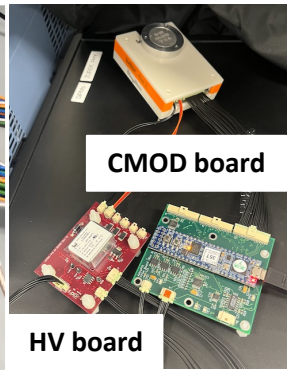
AstroPix + GECCO board

- ✅ v3 single chip testing based on ASTEP sw/fw used in FY24 beam test at FNAL
- ✅ v4 single chip testing based on astropix-python sw/fw

AstroPix + CMOD board + ASTEP sw/fw

- ✅ 1 layer quad chip working
  - 🚧 Available up to 3 layers: work in progress
- 🚧 9 chip PCB: work in progress

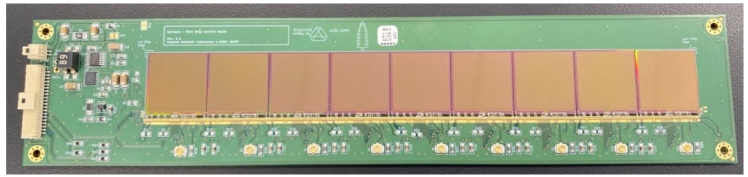




AstroPix v3 quad chips ! HV issue*

- ✅ W112Q07 + v.1.0.0 carrier board
- ! W06Q08 + v.1.0.0 carrier board (Noisy)
- W112Q04 + v.1.0.1 carrier board
- W112Q06 + v.1.0.1 carrier board
- ! W08Q09 + v.1.0.1 carrier board + bus bar
- ! W101Q01 + v.1.0.1 carrier board + bus bar
- ! W101Q02 + v.1.0.1 carrier board + bus bar
- ! W101Q04 + v.1.0.1 carrier board + bus bar
- ✅ W101Q12 + v.1.0.1 carrier board + bus bar (kapton behind chip)

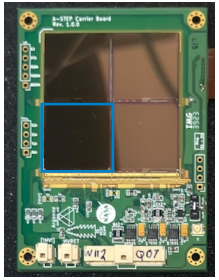
9 chip PCB module (9 Astropix v3 single chips)



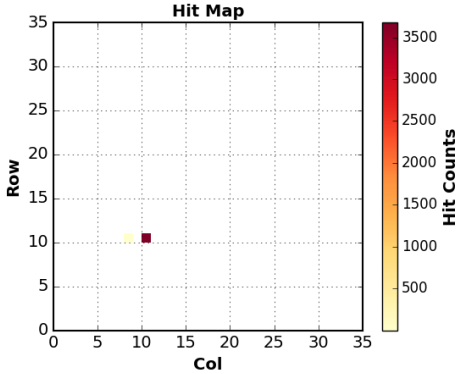
Astropix Testing (0)

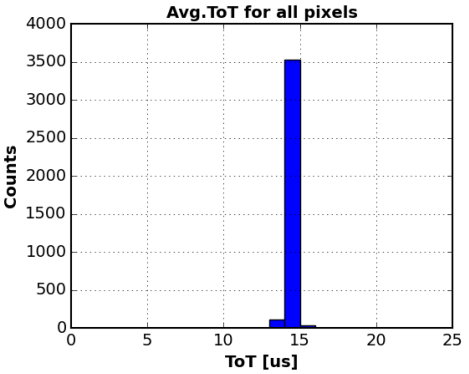
Quad Chip+GECCO board: Injection Test

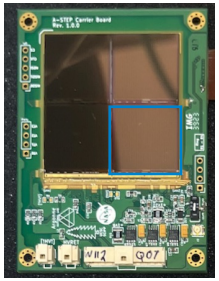
- Injected 300 mV to [10,10] on chip0 and chip1 ; W112Q07



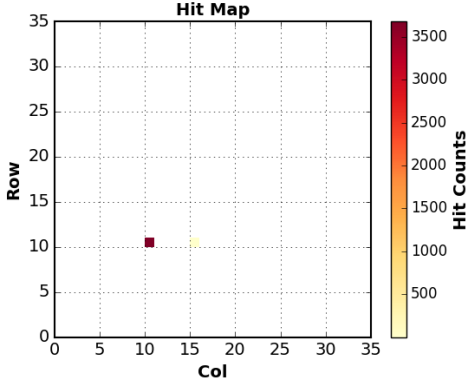
```
/home/daq/AstroPix/2025Feb17_astepfw/astep-fw/sw/, decoded_outputw112q07_quadchipallofftest_injc10r10_1s_20250314-15
Reading in /home/daq/AstroPix/2025Feb17_astepfw/astep-fw/sw/decoded_outputw112q07_quadchipallofftest_injc10r10_1s_20
Reading is done
n_all_rows=7726
   readout  order  layer  ChipID  payload  location  isCol  timestamp  tot_msb  tot_lsb  tot_total  tot_us  fpga_ts
0        1      1      1       0        4        10      0        191        5      146       1426   7.130        0
1        1      2      1       0        4        10      0        148        6       22       1558   7.790        0
2        1      3      1       0        4        10      0        148       13       43       3371  16.855        0
3        1      4      1       0        4        10      1        148        2       80        592   2.960        0
4        1      5      1       0        4        10      0         65       10      226       2786  13.930        0
Index(['readout', 'order', 'layer', 'ChipID', 'payload', 'location', 'isCol',
       'timestamp', 'tot_msb', 'tot_lsb', 'tot_total', 'tot_us', 'fpga_ts'],
      dtype='object')
Max readout value: 251
[Matching but Continue] col.location, row.location = 40,10
[Matching but Continue] col.location, row.location = 40,10
[Matching but Continue] col.location, row.location = 40,10
[Matching but Continue] col.location, row.location = 40,10
... Matching is done!
Summary:
0 of 251 events were found as NaN...
0 of 251 events were found as empty...
251 of 251 events were processed...
Maching # hits = 3680
   col  row        avg
0   10   10  14.064945
1   15   10  11.520000
decoded_outputw112q07_quadchipallofftest_injc10r10_1s_2
```

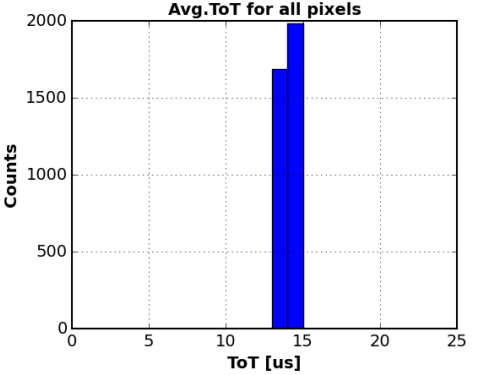






```
/usr/lib/python3/dist-packages/pytz/__init__.py:31: SyntaxWarning: invalid escape sequence '\s'
  match = re.match("^#\s*version\s*([0-9a-z]*)\s*$", line)
/home/daq/AstroPix/2025Feb17_astepfw/astep-fw/sw/, decoded_outputw112q07_quadchipallofftest_injch1c10r10_vinj500_1s_202
Reading in /home/daq/AstroPix/2025Feb17_astepfw/astep-fw/sw/decoded_outputw112q07_quadchipallofftest_injch1c10r10_vinj5
Reading is done
n_all_rows=7658
   readout  order  layer  ChipID  payload  location  isCol  timestamp  tot_msb  tot_lsb  tot_total  tot_us  fpga_ts
0        1      1      1       1        4        10      0        171        8      162       2210  11.050        0
1        1      2      1       1        4        10      0        144       11      177       2993  14.965        0
2        1      3      1       1        4        10      1        143        0      182        182   0.910        0
3        1      4      1       1        4        10      0        156       11      107       2923  14.615        0
4        1      5      1       1        4        10      1        156       11       88       2904  14.520        0
Index(['readout', 'order', 'layer', 'ChipID', 'payload', 'location', 'isCol',
       'timestamp', 'tot_msb', 'tot_lsb', 'tot_total', 'tot_us', 'fpga_ts'],
      dtype='object')
Max readout value: 251
[Matching but Continue] col.location, row.location = 63,10
[Matching but Continue] col.location, row.location = 63,16
... Matching is done!
Summary:
0 of 251 events were found as NaN...
0 of 251 events were found as empty...
Maching # hits = 3678
   col  row        avg
0    8   10   6.425000
1   10   10  14.422935
decoded_outputw112q07_quadchipallofftest_injch1c10r10_vinj
```





Astropix Testing (1)

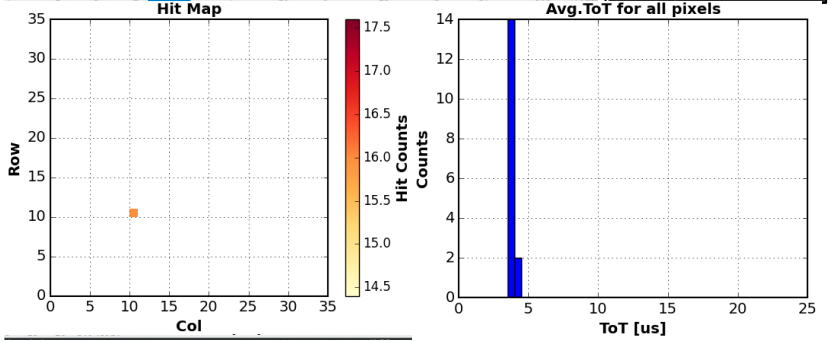
Quad Chip: Injection Test

- Injected 300 mV to [10,10] on chip0/1/2/3; W101Q12

	readout	order	layer	ChipID	payload	location	isCol	timestamp	tot_msb	tot_lsb	tot_total	tot_us
0	1	1	1	0	4	10	1	191	3	24	792	3.960
1	1	2	1	0	4	4	0	138	11	4	2820	14.100
2	1	3	1	0	4	10	0	19	3	30	798	3.990
3	1	4	1	0	4	10	1	187	3	18	786	3.930
4	1	5	1	0	4	10	0	15	3	37	805	4.025

Maching # hits = 16

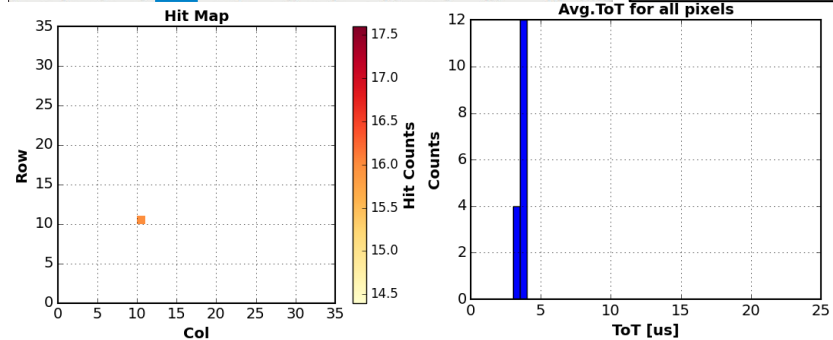
	col	row	avg
0	10	10	3.940937



	readout	order	layer	ChipID	payload	location	isCol	timestamp	tot_msb	tot_lsb	tot_total	tot_us
0	1	1	1	1	4	10	1	108	2	191	703	3.515
1	1	2	1	1	4	10	0	103	2	202	714	3.570
2	1	3	1	1	4	10	1	103	2	184	696	3.480
3	1	4	1	1	4	10	0	178	2	168	680	3.400
4	1	5	1	1	4	10	1	178	2	150	662	3.310

Maching # hits = 16

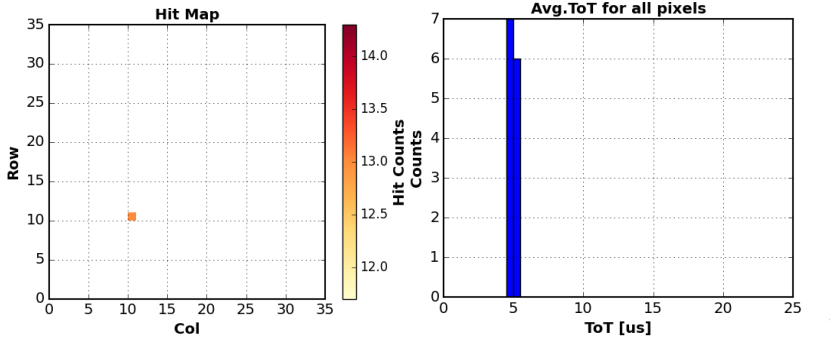
	col	row	avg
0	10	10	3.535938



	readout	order	layer	ChipID	payload	location	isCol	timestamp	tot_msb	tot_lsb	tot_total	tot_us
0	1	1	1	2	4	10	0	203	3	195	963	4.815
1	1	2	1	2	4	10	1	203	3	201	969	4.845
2	1	3	1	2	4	10	0	199	4	0	1024	5.120
3	1	4	1	2	4	10	1	199	3	199	967	4.835
4	1	5	1	2	4	10	0	18	4	59	1083	5.415

Maching # hits = 13

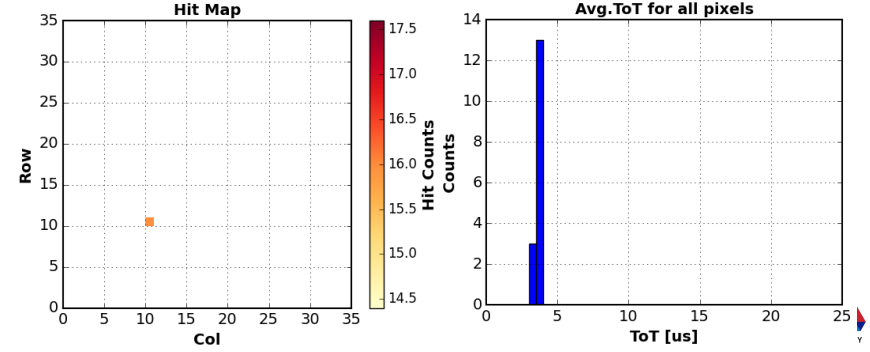
	col	row	avg
0	10	10	5.051923



	readout	order	layer	ChipID	payload	location	isCol	timestamp	tot_msb	tot_lsb	tot_total	tot_us
0	1	1	1	3	4	10	0	147	2	193	705	3.525
1	1	2	1	3	4	10	1	147	2	187	699	3.495
2	1	3	1	3	4	10	0	142	2	205	717	3.585
3	1	4	1	3	4	10	1	142	2	194	706	3.530
4	1	5	1	3	4	10	0	217	2	216	728	3.640

Maching # hits = 16

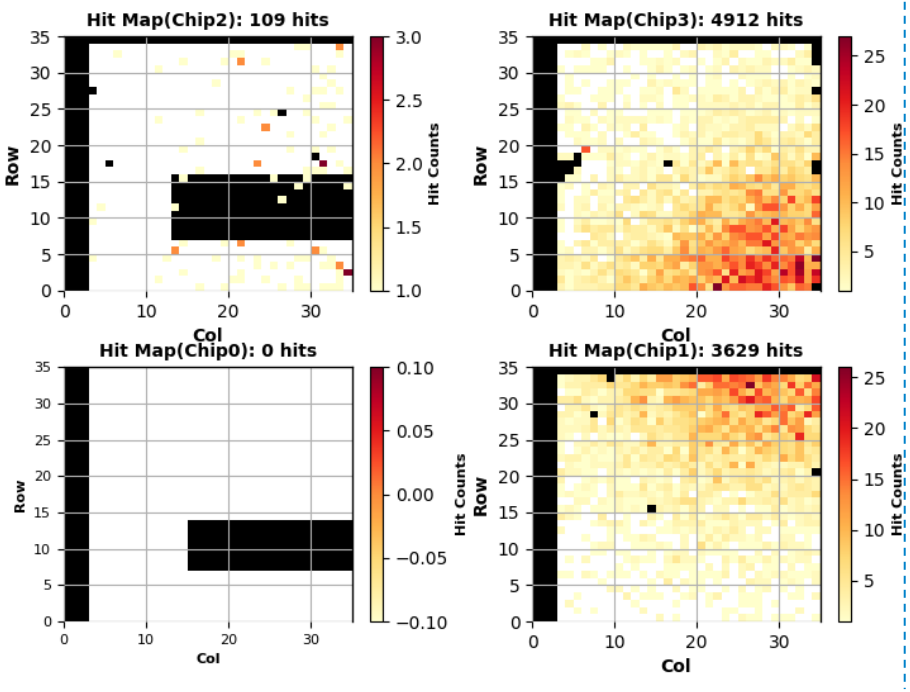
	col	row	avg
0	10	10	3.536563

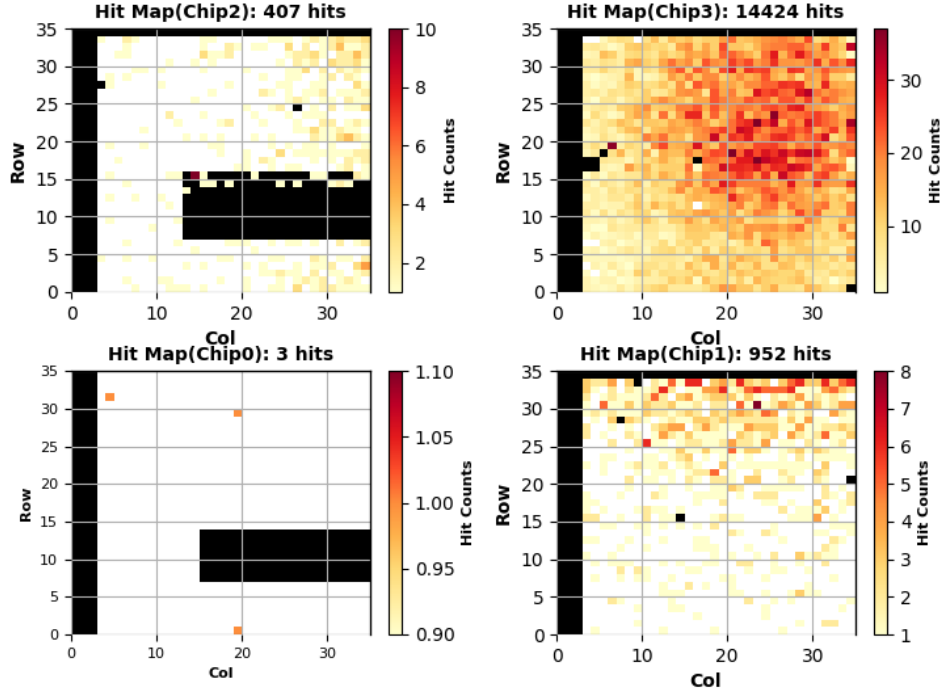


Astropix Testing (2)

Quad Chip: Sr90 Source Test (1)

- Sr90 source test using CMOD board (W101Q12)
- Hit Map looks reasonable with respect to moving source position.

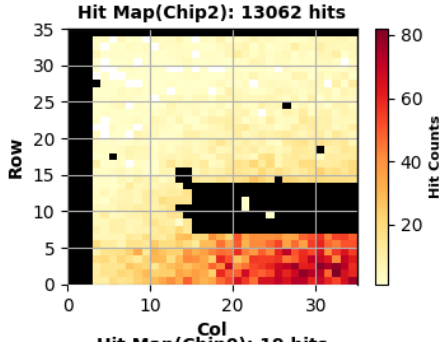


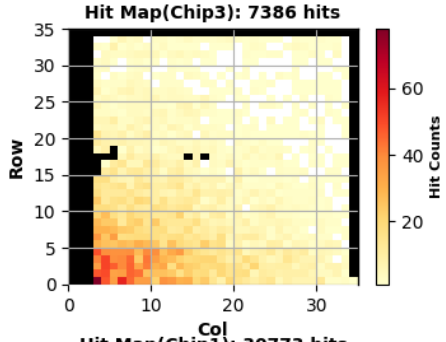


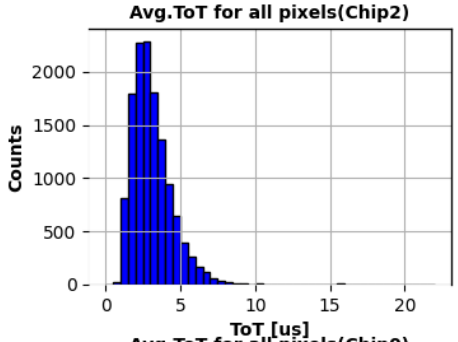
Astropix Testing (3)

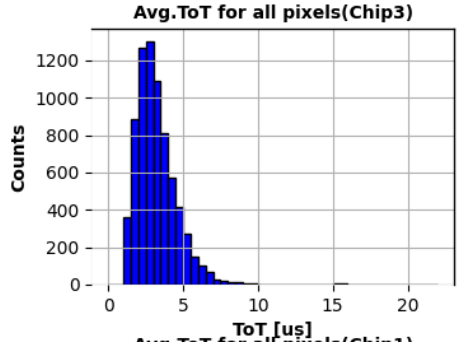
Quad Chip: Sr90 Source Test (2)

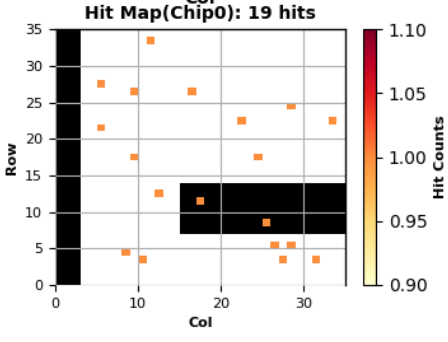
- Sr90 source test using CMOD board (W101Q12)
- The hit map aligns well with the source position at the center of the quad chip.
- The ToT distribution is well-described by a Landau convoluted with a Gaussian function.

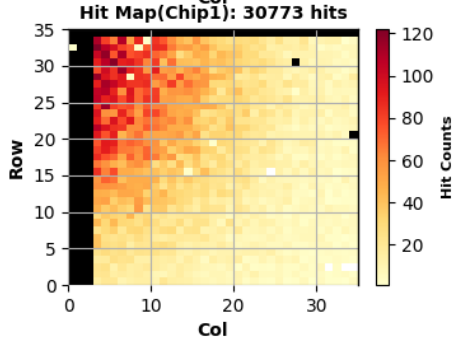


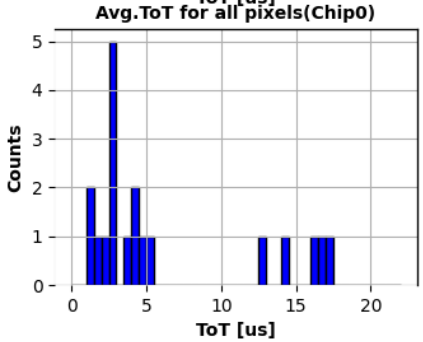


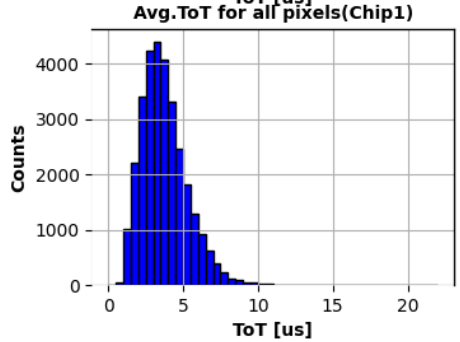








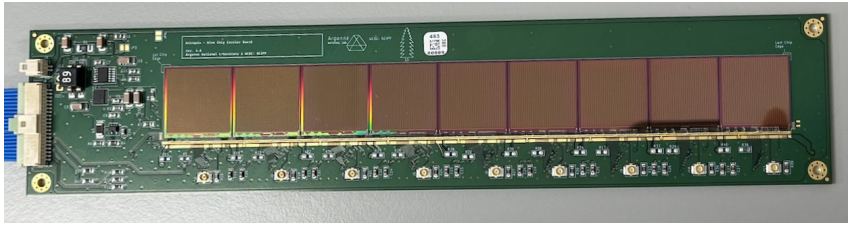


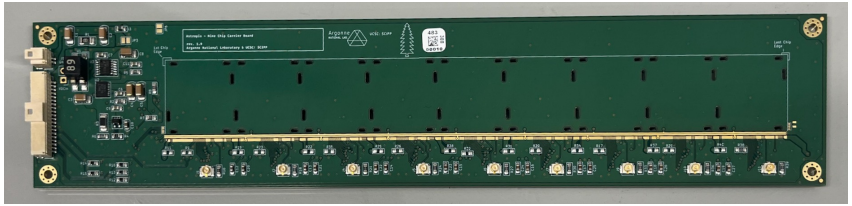


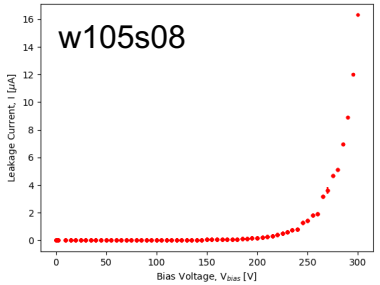
Astropix Testing (4)

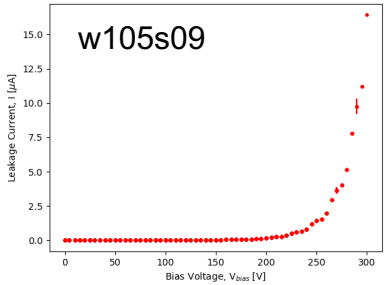
Current Status of 9 Chip PCB: HV issue

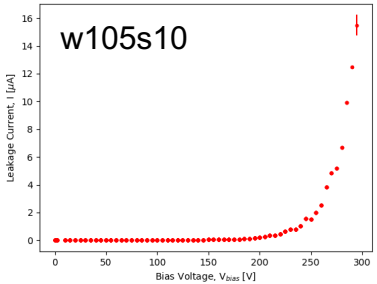
- Unable to apply high voltage to 9 chip PCB due to overcurrent — under investigation 🚧
- High voltage could be applied to the bare PCB (without chips)
- IV measurement of four AstroPix v3 single chips before assembly (w105s08/s09/s10 and w106s01)
- Unable to apply high voltage to 9 chip PCB with four mounted chips

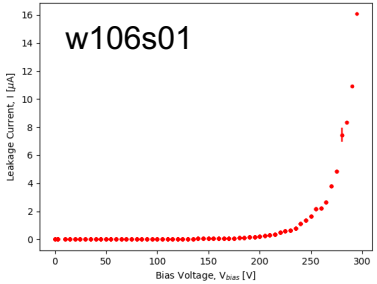






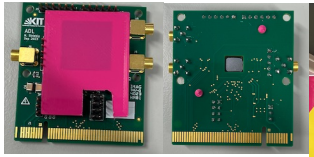


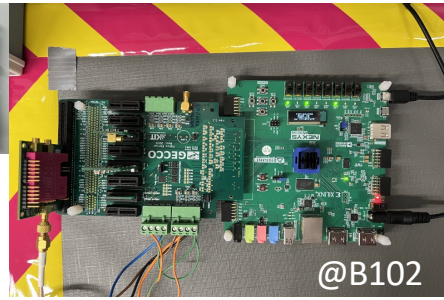




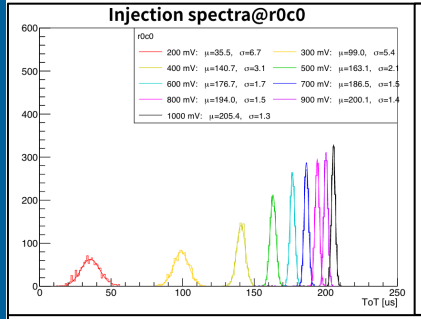
Astropix Testing (5)

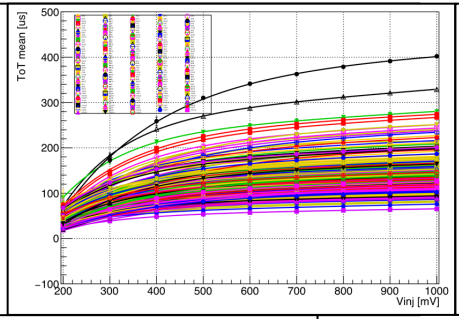
Astropix v4 single chip (YoonHa)

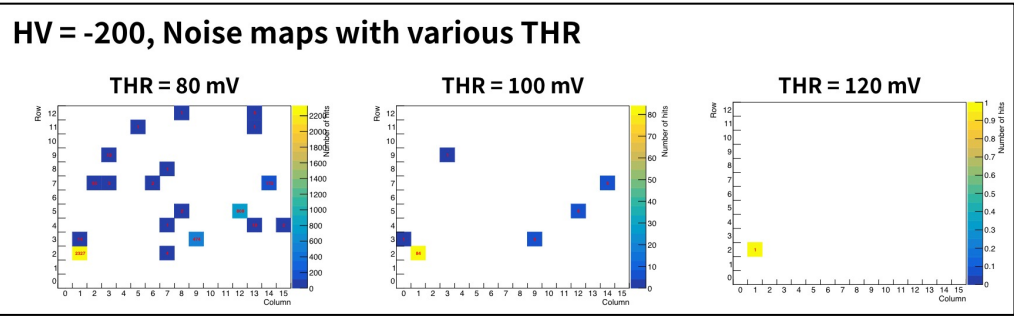




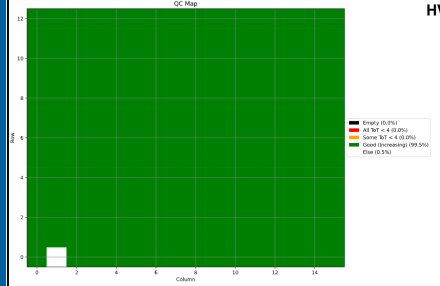
- ✅ Optimized the configuration for v4 testing
- ✅ Injection scan (HV = -200 V, threshold = 130 mV)
- ✅ Noise scan
- 🚧 Source test for calibration curve at Busan National University: in progress
- 🚧 Beam test at KEK or CERN: in progress







Quality check for each pixels **(99.5%)**

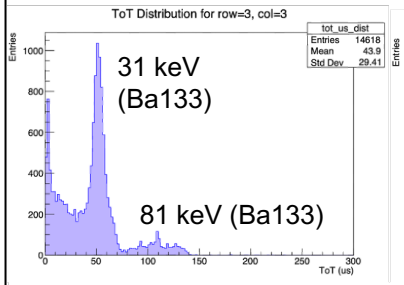


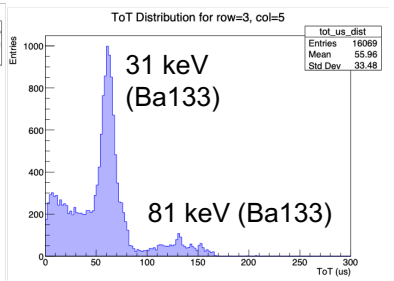
HV = -200 V, THR = 130 mV

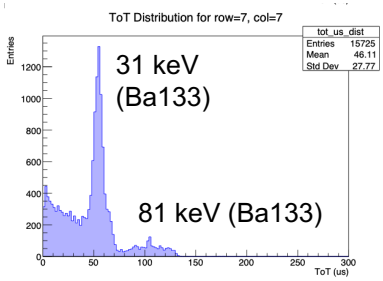
Good pixel
:mean ToT > 4 and increases with V_{inj}

Else (r0c1)
:mean ToT > 4, but not increases with V_{inj}

- Multiple injection scans on r0c1,
- but the **results varied each time**(next page)







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Summary & Plan

- Astropix v3 single and quad chip, v4 single chip testing
  - ✅ AstroPix v3 Quad chip + GECCO board: Injection test
  - ✅ AstroPix v3 Quad chip + CMOD board: Injection and Source test
  - 🚧 9 Chip PCB: HV issue
  - ✅ AstroPix v4 Single chip
- Prototype module (9 AstroPix v3 single chips) testing will be done by July 2025 for PDR.


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AstroPix and BIC Timeline

Not shown:
Early CD4 (Oct 2032)
CD4 (Oct 2034)

We are here

FY19 Q3 Q4 | FY20 Q1 Q2 Q3 Q4 | FY21 Q1 Q2 Q3 Q4 | FY22 Q1 Q2 Q3 Q4 | FY23 Q1 Q2 Q3 Q4 | FY24 Q1 Q2 Q3 Q4 | FY25 Q1 Q2 Q3 Q4 | FY26 Q1 Q2 Q3 Q4 | FY27 Q1 Q2 Q3 Q4 | FY28 Q1 Q2 Q3 Q4 | FY29 Q1 Q2 Q3

- AstroPix v1: Design & Fabr. | Test
- AstroPix v2: Design & Fabr. | Test
- AstroPix v3: Design & Fabr. | Test | Test
- AstroPix v4: Design & Fabr. | Test
- AstroPix v5: Design & Fabr. | Test
- AstroPix v6: Design & Fabr. | Test
- AstroPix v6 (production): Production Fab.

v3 has comprehensive test program: benchtop and testbeam, irradiation, quad-chip readout for NASA payload mission (A-STEP), integration with Pb/SciFi for ePIC (R&D studies and test article production)

first v5 wafers used for preproduction

Start of production driven by project fund availability (estimated ~ 1 year after CD2/3)

EIC Project Milestone
New AstroPix version

ePIC BIC Timeline

- Design and generic R&D
- Final design and EIC R&D
- BIC Preproduction
- BIC Production

CD0 | CD1 | CD3a | CD3b | CD2/3 | Start of BIC installation at BNL

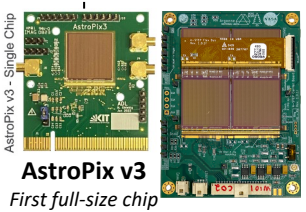
AstroPix v1

HV-CMOS MAPS based on ATLASPix3, designed for the AMEGO-X NASA mission, optimized for power dissipation and energy resolution
NIMA 1019 (2021) 165795

0.45 x 0.45 cm² chip, 175 µm pixel pitch
18 x 18 pixel matrix
Power dissipation 14 mW/cm²

AstroPix v2

1 x 1 cm² chip, 250 µm pixel pitch
35 x 35 pixel matrix
Row/column readout
Power dissipation 3.4 mW/cm²



AstroPix v3

First full-size chip

2 x 2 cm² chip, 500 µm pixel pitch
Row/column readout
Power dissipation <1 mW/cm²
2.5 MHz timestamp, 200 MHz ToT

AstroPix v4

Final design but smaller size

1 x 1 cm² chip, 500 µm pixel pitch
Individual pixel readout
3 timestamps, 3.25 ns time resolution
TuneDAC for pixel-by-pixel thresholds

AstroPix v5
pre-production chip
1.87 x 1.9575 cm² chip, 500 µm pixel pitch
Design identical to v4 (with bug fixes)

AstroPix v6
production chip
2 x 2 cm² chip, 500 µm pixel pitch
Design identical to v5 (with bug fixes)