*The ePIC Barrel Imaging Calorimeter*

# System Testing Summary


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POC

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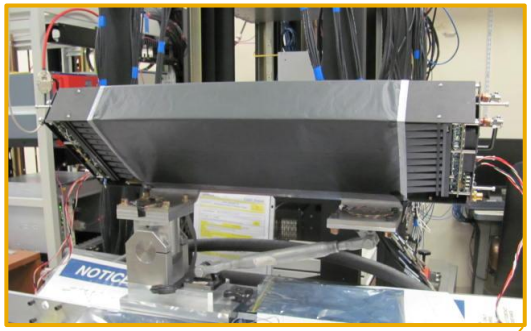
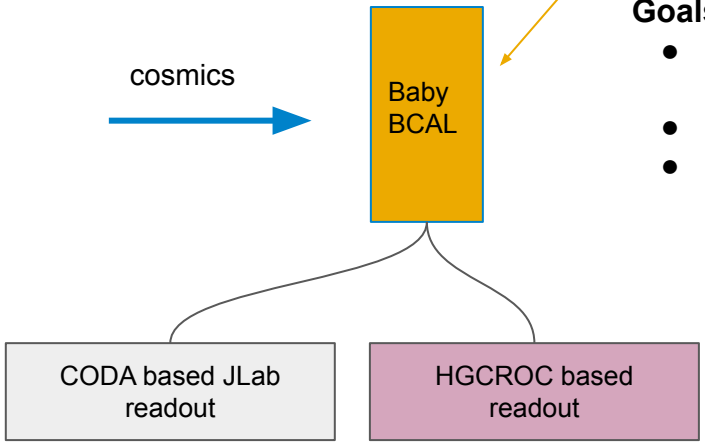
Beam Test
POC

# Test Article Evolution - PED

## What do we test and why?

GlueX Baby BCal






**Existing:**

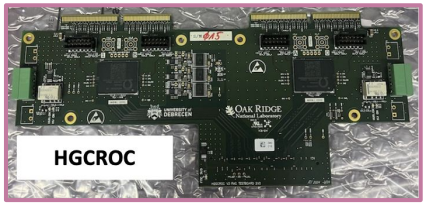
- Baby BCAL: ~60 cm long, 15.5 $X_0$ deep GlueX BCAL prototype with 40 SiPMs on each side (S12 Hamamatsu)
- CODA Based Readout: 250MHz fADCs, to TDC currently

**To be upgraded:**

- HGCROC Based readout
- New SiPM Board with BIC SiPMs (S14 Hamamatsu) and optical cookies

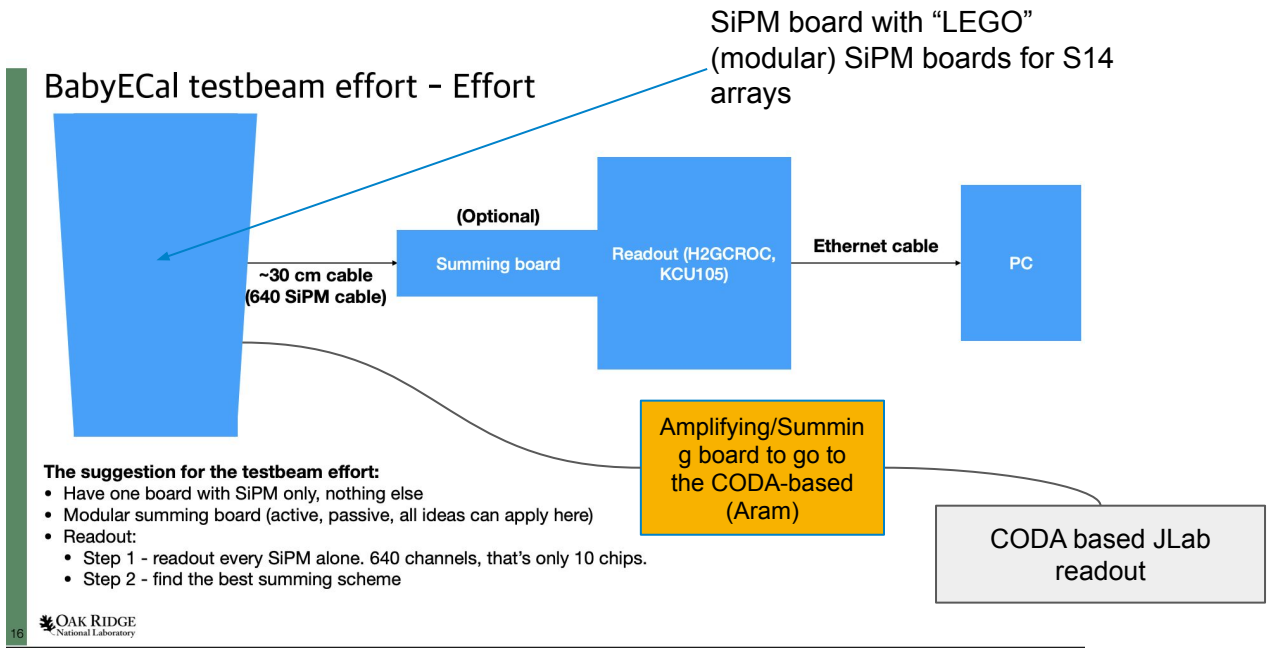
**Goals:**

- Test performance of Baby BCAL (response to muons) with new SiPMs, optical coupling (cookies) and HGCROC readout
- Benchmark against performance with previous readout (CODA based)
- Benchmark improvement in performance thanks to the new SiPMs

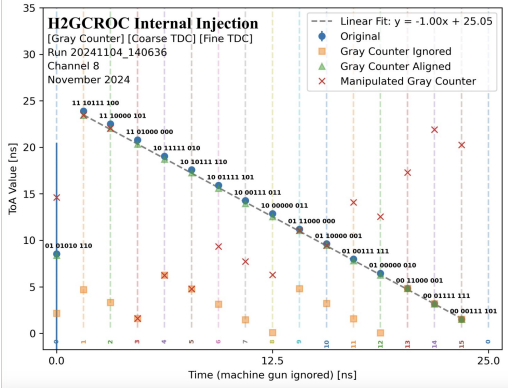


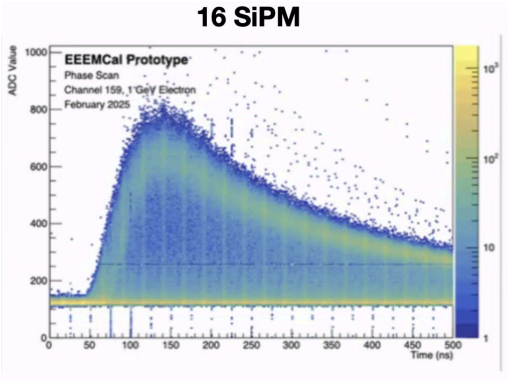

**Beam Test Opportunity:**
EM (e/ɣ) beam with range of energies up to > 10 GeV (ideally)
**Goal: linearity of response**

# Test Article Evolution - PED




Calibrated TOA




**ToA Calibration**:

- Crucial for BIC (SiFi/Pb) position resolution.
- EEEMC results suggest phase elimination is possible. PED tests should include ToA calibration efforts. Need direct tests for BIC.

**Summing Scheme**:

- Impacts signal shape and size.
- EEMCAL example shows risk of long signals—must investigate carefully.

# Test Article Evolution - PED

**Simulation Feedback**:

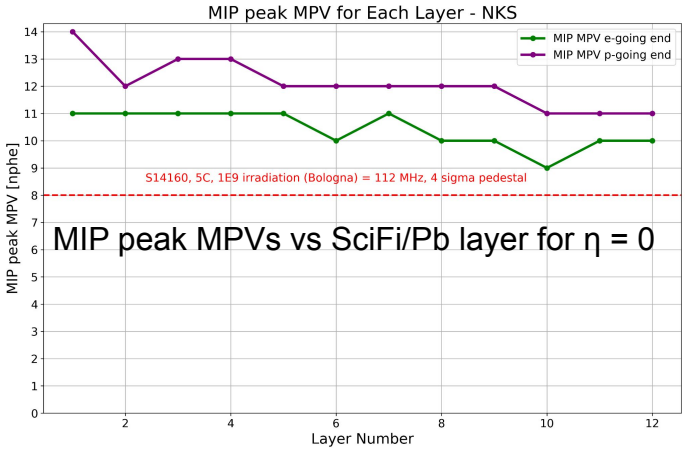
- Measurements must inform Minho's simulation.
- Align with PDR timeline—HGCROC parameters

**Pileup Studies**:

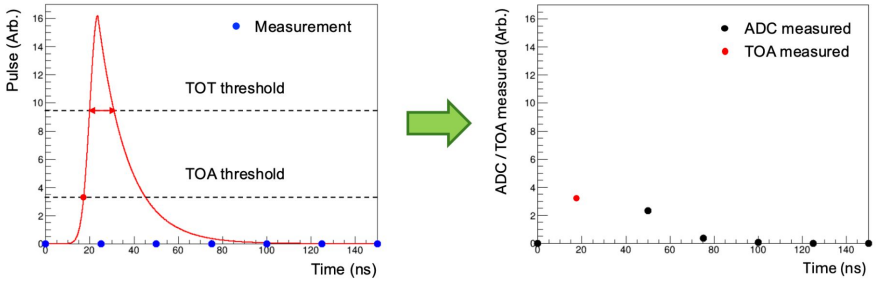
- Estimate pileup from:
  - Two physics events.
  - Background + signal.
- Revisit Jeff's background numbers.

**Photon Statistics**:

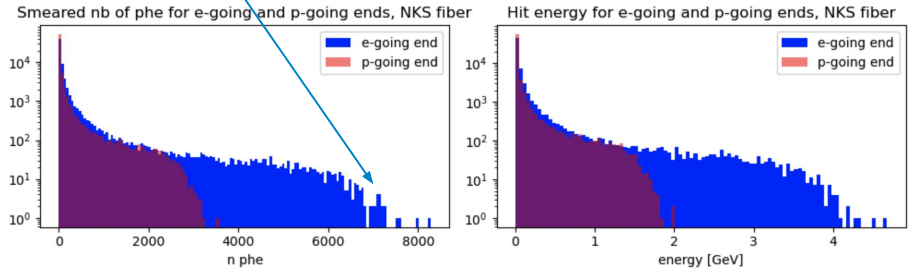
- Mean number of photoelectrons per signal




## ADC, TOA, and TOT measurements

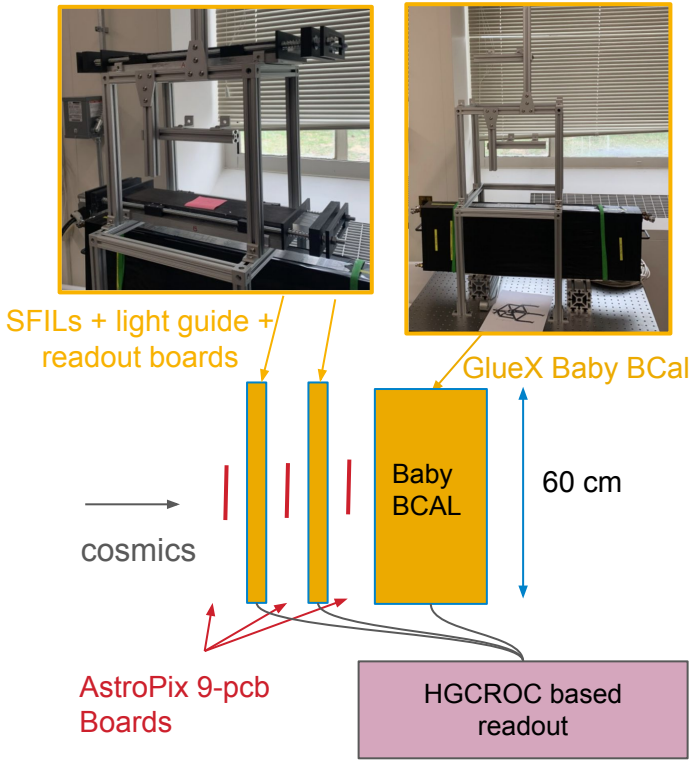


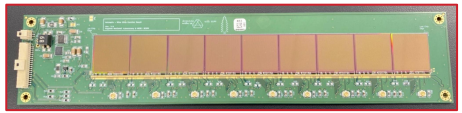

~7000 phe



# Test Article Evolution - PED

## What do we test and why?



**To be upgraded:**

- 2 SFILs (Scintillating Fiber/Pb Intermediate (thin) Layers) with S14 SiPMs (existing, but to be compatible with the HGCROC readout)
- 9-chip pcb boards (eventually 3 of them, starting from one)

**Goals:**

- Show the performance of the Integrated System of AstroPix 9-chip (daisy-chained chips) with SciFi: synchronization is needed
  - Read 3 9-chip PCB boards in sync
  - Read 9-chip PCB board and SciFi (HGCROC) in sync
    - The sync work can start with quad/single chip
- Develop basis for the cross-calibration procedure (position and energy)
- Additionally: Develop basis for the large scale AstroPix energy calibration with sources (AstroPix v4 single chip based)

**Beam Test Opportunity:**

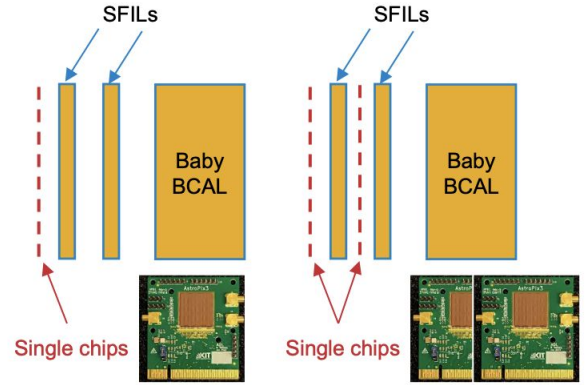
- EM (e/ɣ) beam with range of energies up to > 10 GeV (ideally), **Goal:** linearity of response
- e/π beam with range of energies up to > 10 GeV (ideally), **Goal:** e/π separation

# Test Article Evolution - PED

## System Testing Plan

### Plan for Synchronization

**Possible setup of system integration at bench test in ANL:**

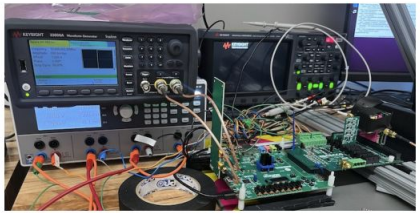





**How to synchronize?**

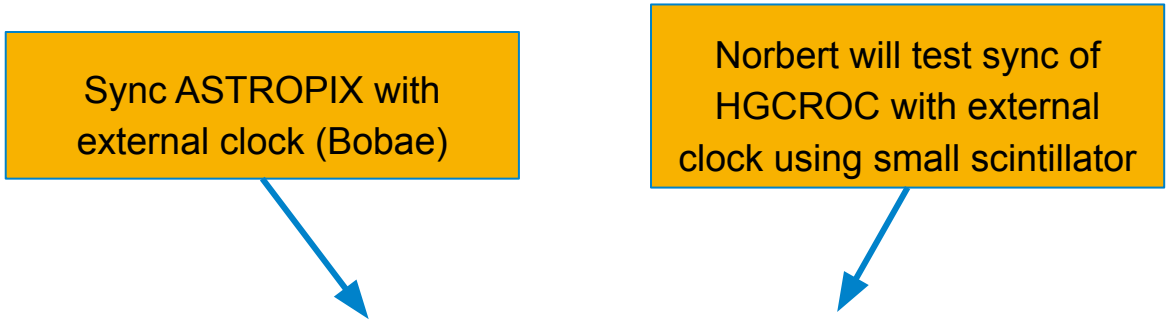
- Plan A
  - LVDS MISO0/1 signals that generated from Astropix used as trigger IN for baby bcal


- Plan B
  - Provide up to 10 MHz LVDS external clock to Astropix chip via PMOD



# Test Article Evolution - PED

**Sync of AstroPix with HGCROC** (Proof of principle)




- In the next step we will combine two together and test the AstroPix - HGCROC sync (visit ORNL in May?)
- We might also be able to read AstroPix with the FPGA that reads the HGCROC board
- **Workforce and PED planning**
    - Workforce needed for investigating the readout parameters with HGCROC to find the optimal summing configuration, to stay on track with the PED timeline
    - Tests will be also happening in Korea

# Test Article Evolution - PED

**Discussion about the QC (chip/module/tray) tests, system tests and calibration**

**Calibration of the sensors needed at scale**

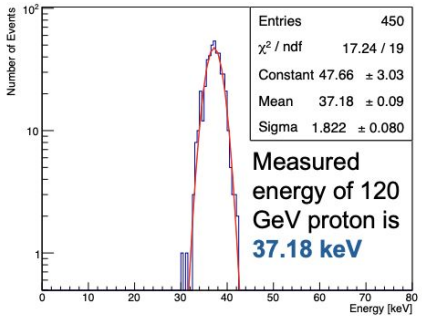
- V4 will help clarify calibration procedures, but the ultimate tests and procedure development will be possible with the new v5 chip
- Verify needs for temperature dependent relative calibration

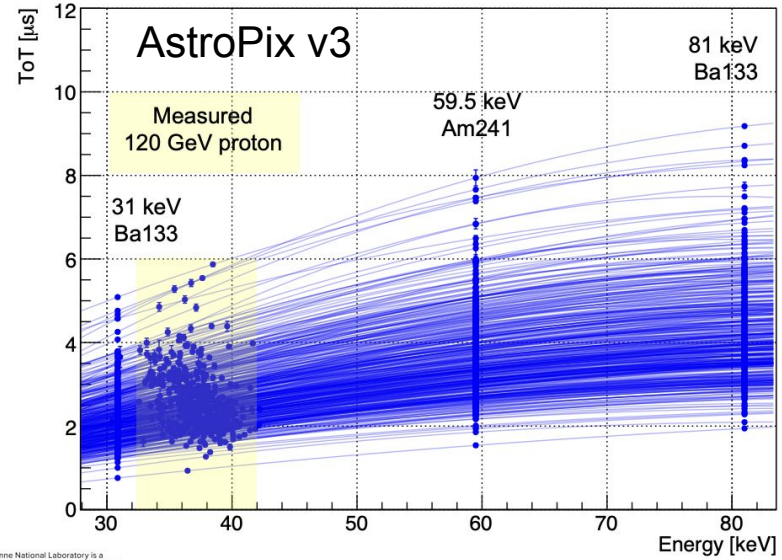
**Initial thoughts:**
**Calibration Steps**

- Threshold tuning at **module/chip QC level**
- Absolute calibration with source at **system level**
- PCB thickness on modules may complicate source-based calibration(?) (verify)

From the System Testing/Module-Wafer discussion is clear that **we need to rerun the simulation on the physics performance** (energy splitting and resolution from AstroPix) with non fully depleted chip: smaller dynami range (let's check 250 keV)

**Common meeting on Modules/Wafers/System QC in 2 weeks**



# Calibration

**Overall System Calibration**

- How **material non-uniformity impacts the EM shower calibration performance?**
  - Simulate sampling fraction vs energy for each SFIL (layer dependent), reviewers ask about the calibration procedure
  - Include both MIPs (muons) and electrons
  - We can also extract it from the beam test results from the KEK
- **AstroPix energy calibration separate** (energy calibration absolute from sources, relative later in-situ)
- **Alignment calibration** mostly from muons, with initial metrology (to be tested with first modules)
- **Cross calibration of systems possible and to be tested in PREP in full system**: we expect it will introduce improvements on top of the single-system calibration: e.g. position calibration for SciFi/Pb cross calibrated with AstroPix position