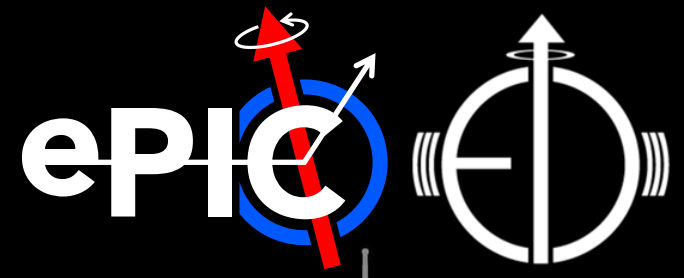




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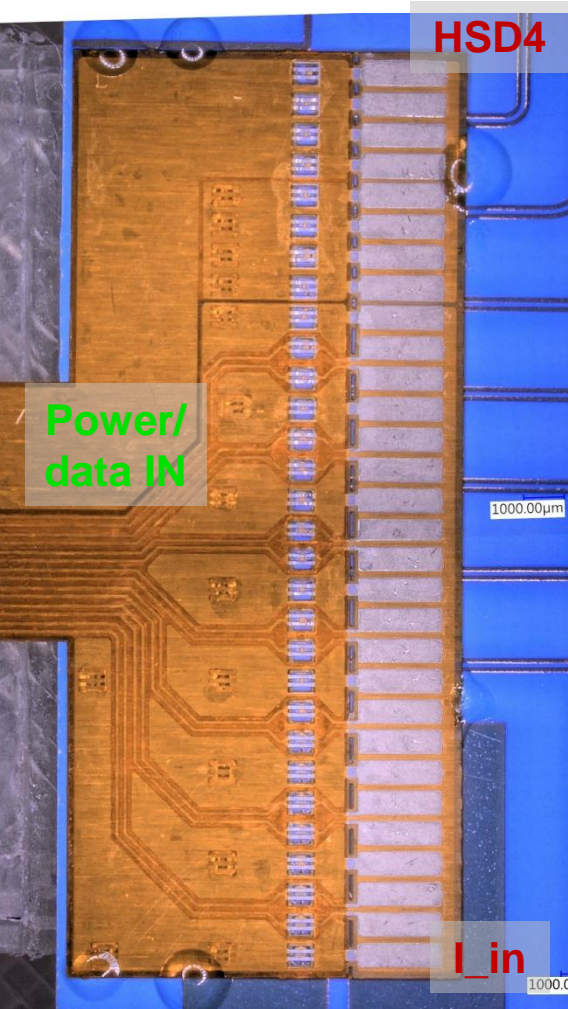
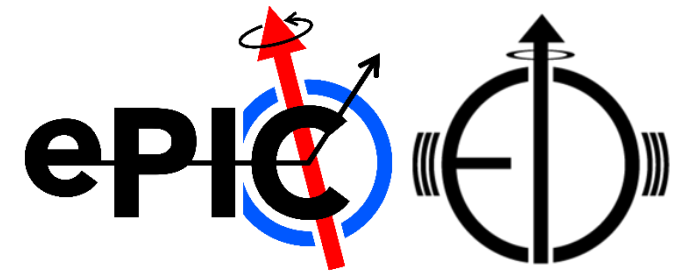
# FPC mounting & bonding (spTAB)

James Glover, Eve Tse

EIC-UK WP1 (MAPS)

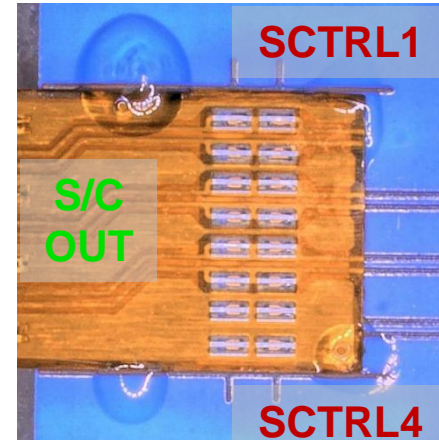
Wed, 12<sup>th</sup> February 2025

# Prototype to PCB mounting (1)

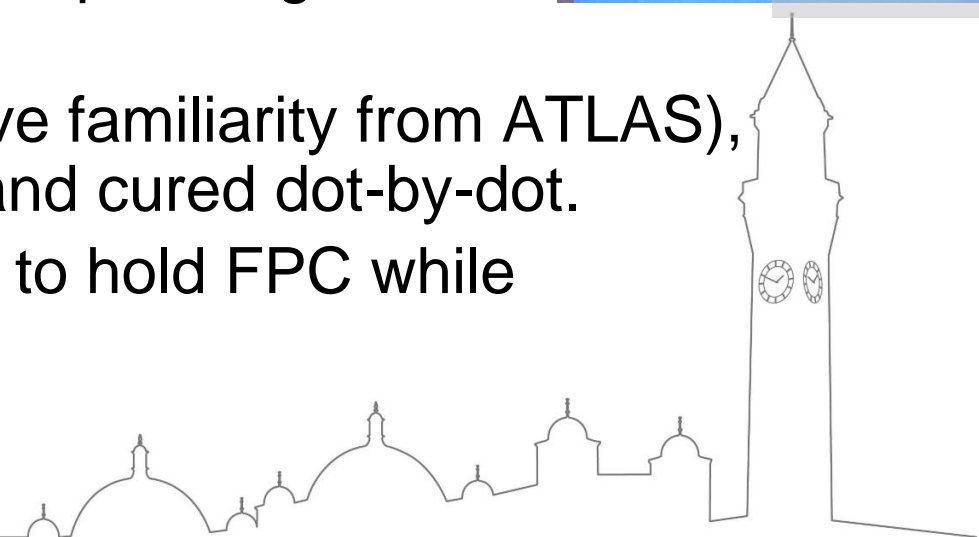
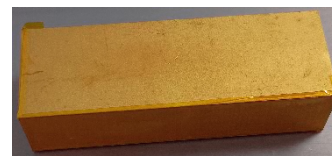


- Following on from bond trials ([reported here](#)).
- Mounting and alignment of FPC to PCB.
- Considered adhesives to help hold FPC to PCB.

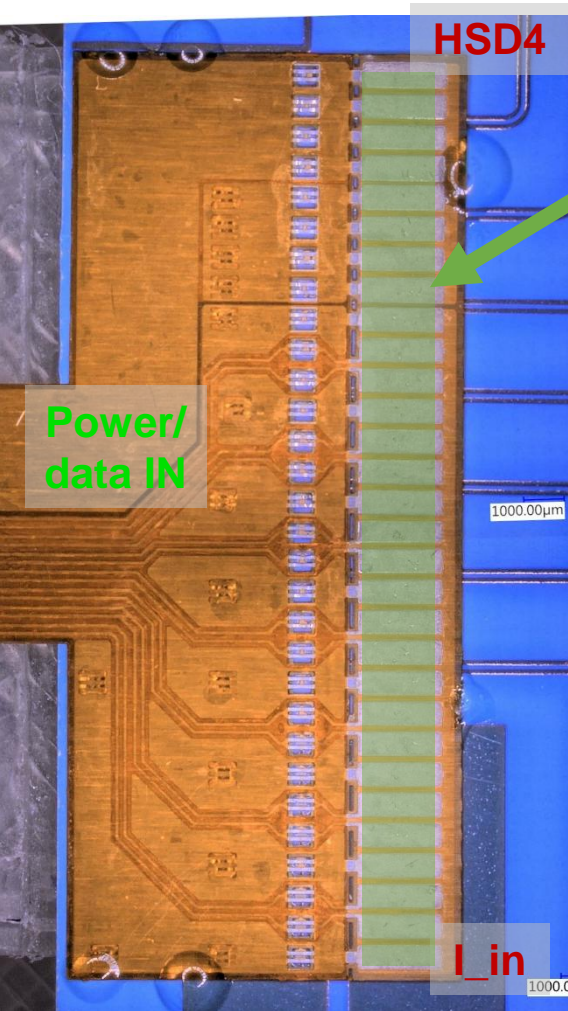
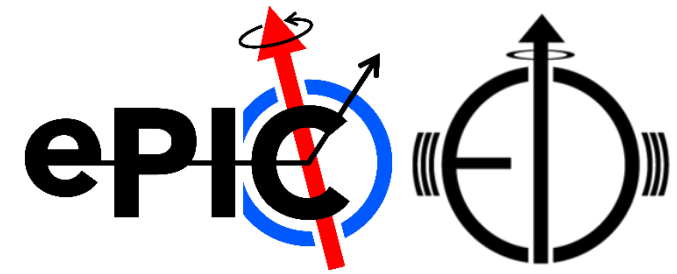
- Opted against glue under the FPC, to minimise height offset and prevent glue squeezing out to bond areas.
- Opted for a [UV-cure glue](#) (have familiarity from ATLAS), can be placed on FPC edge and cured dot-by-dot.
- Used a Kapton coated weight to hold FPC while applying glue.



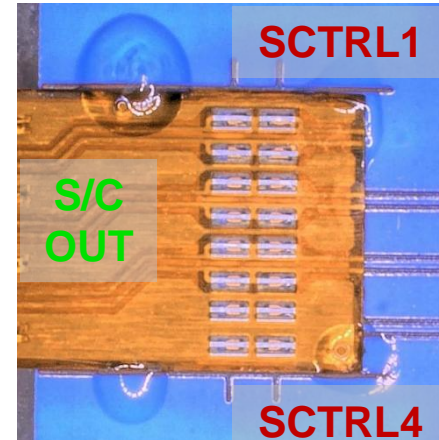
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# Prototype to PCB mounting (2)

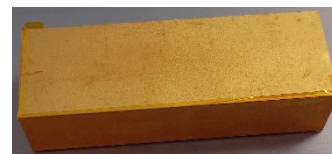


- Additional solder/probe pads on the **Power/data IN** side of the FPC made holding FPC with the weight straightforward.
- Applied the glues dots on the left before removing weight, additional dots prevent FPC from lifting at the edge (cotton swab used to ensure FPC was flat during curing).
- There was limited locations for the weight on the **S/C OUT** side of the FPC.
  - Found it harder to keep this side flat.

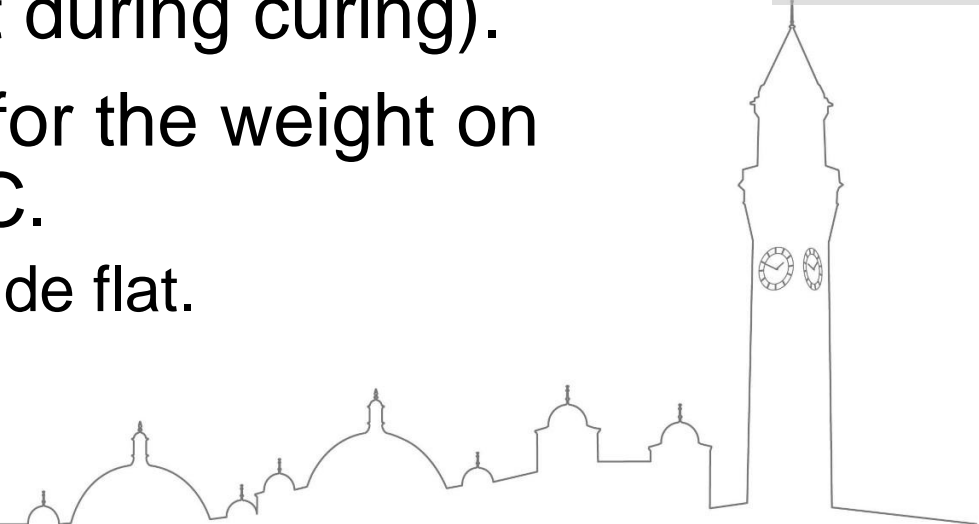


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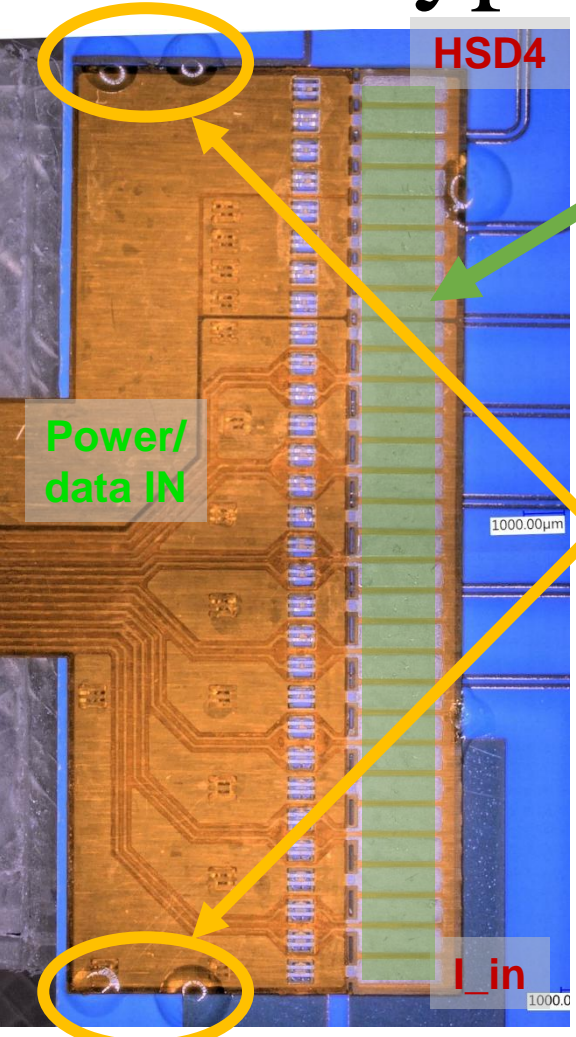
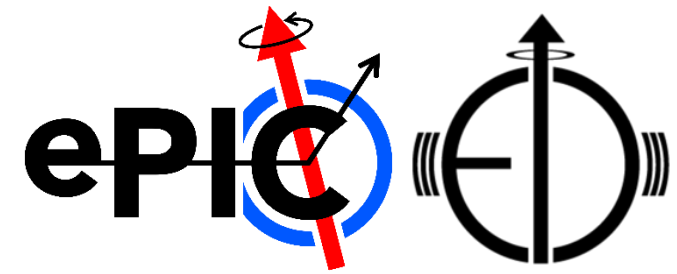
12 February 2025



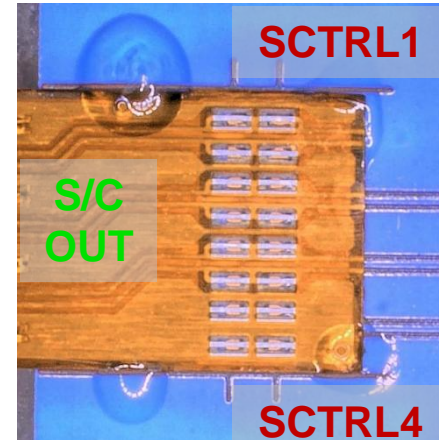
EIC-UK WP1 (MAPS)



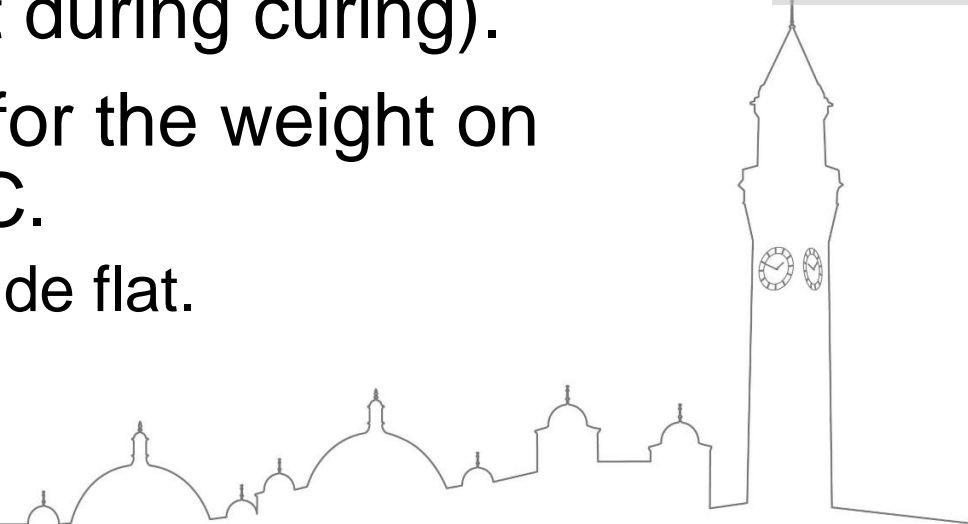
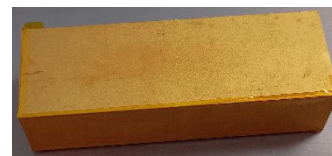
# Prototype to PCB mounting (2)



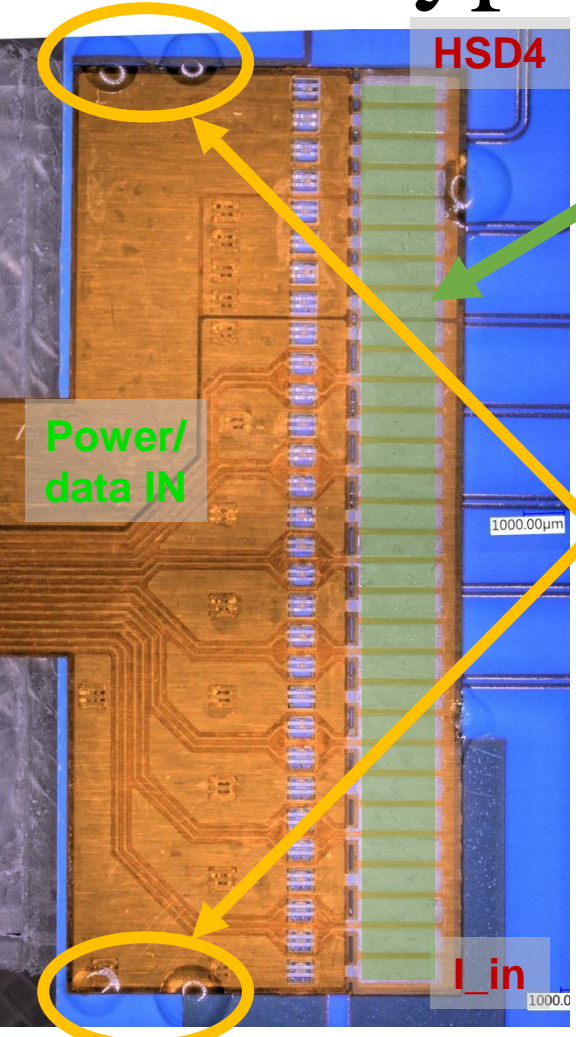
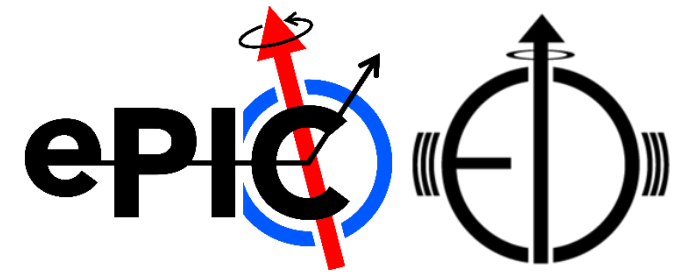
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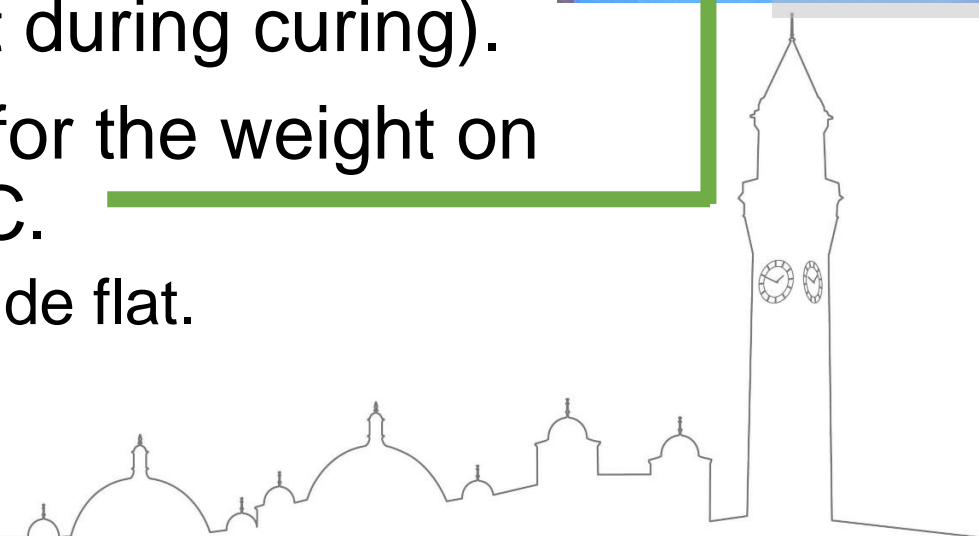
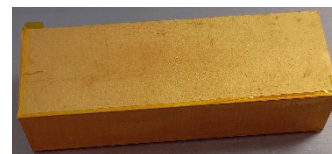
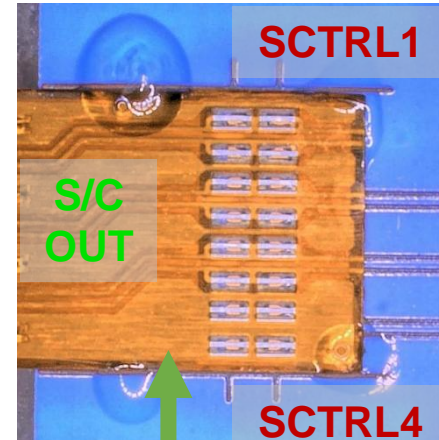
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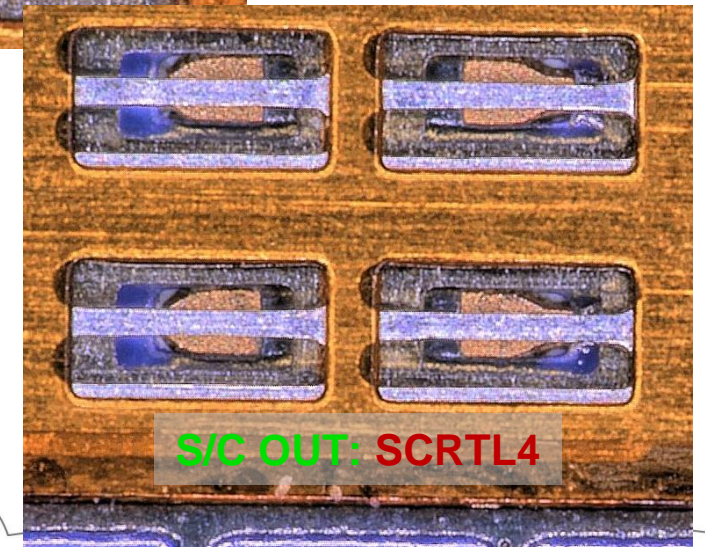
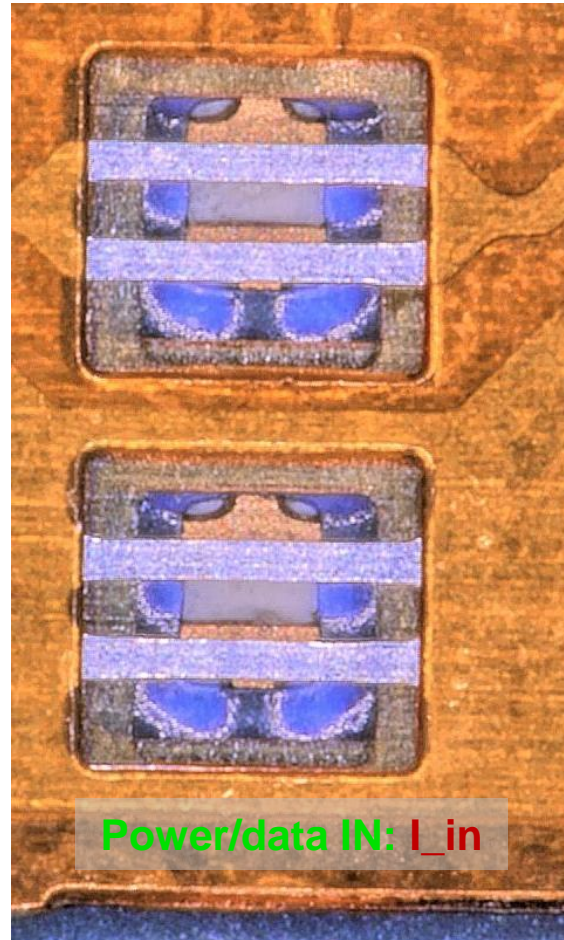
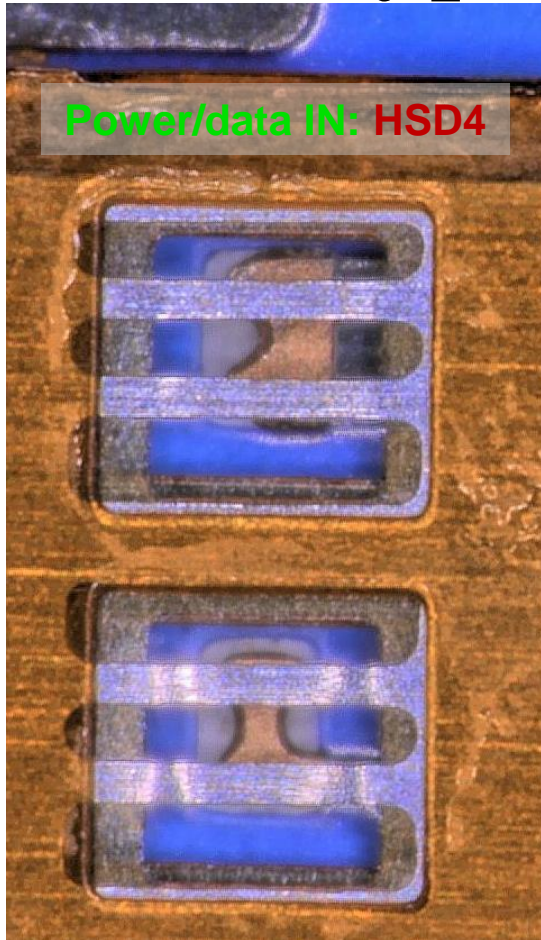
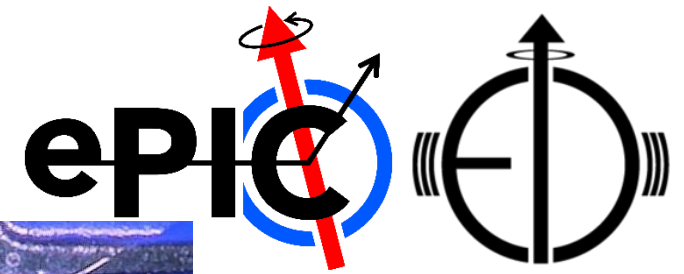
# Prototype to PCB mounting (2)



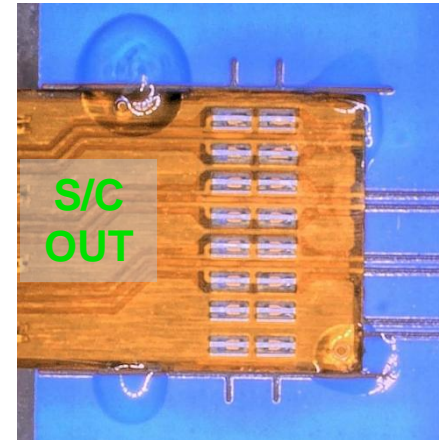
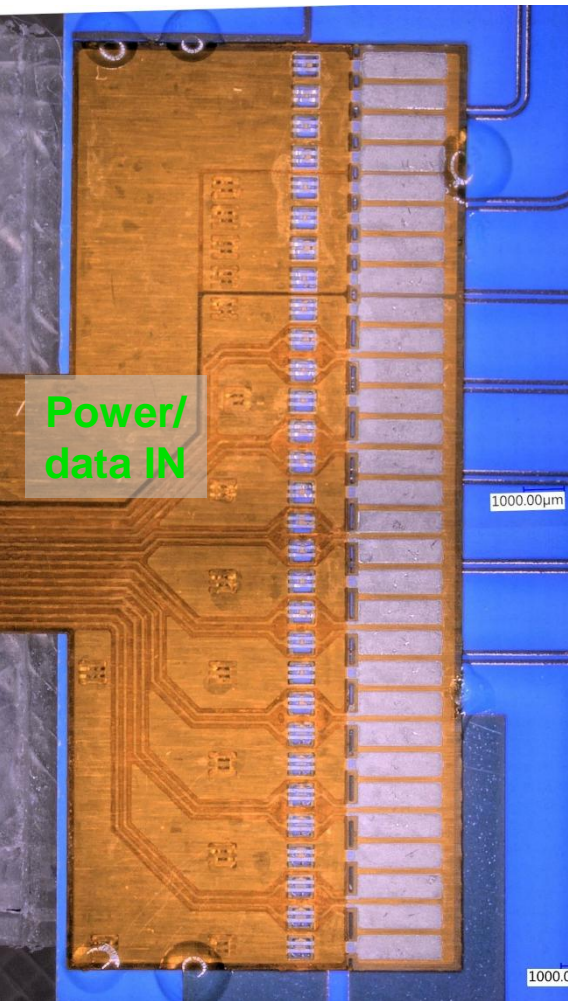
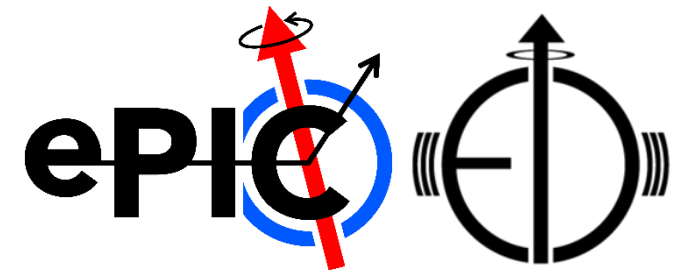
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# Prototype to PCB alignment



# For the eagle eyed!



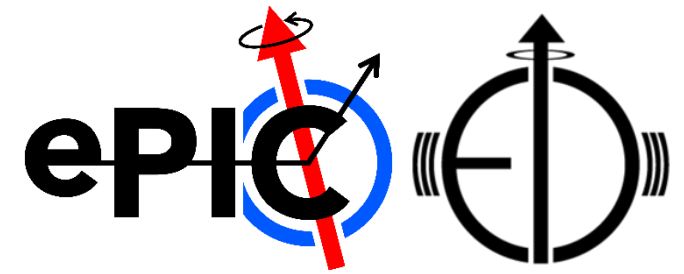
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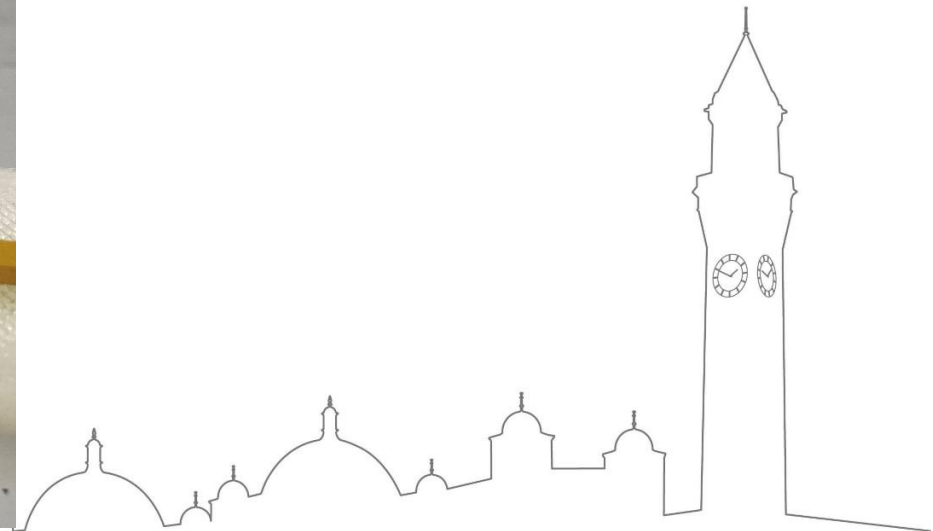
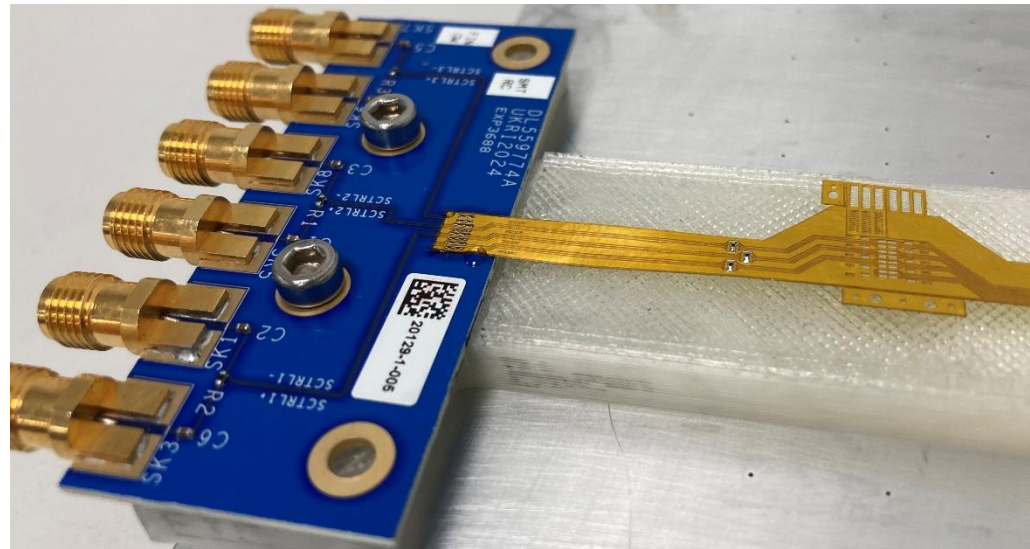
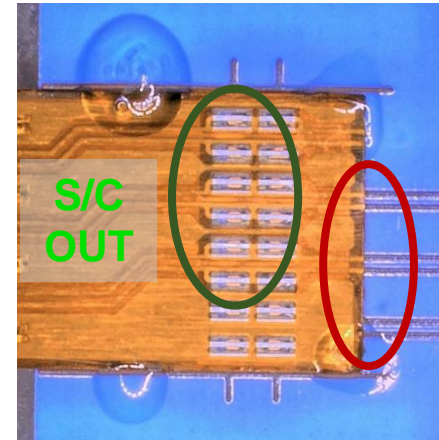
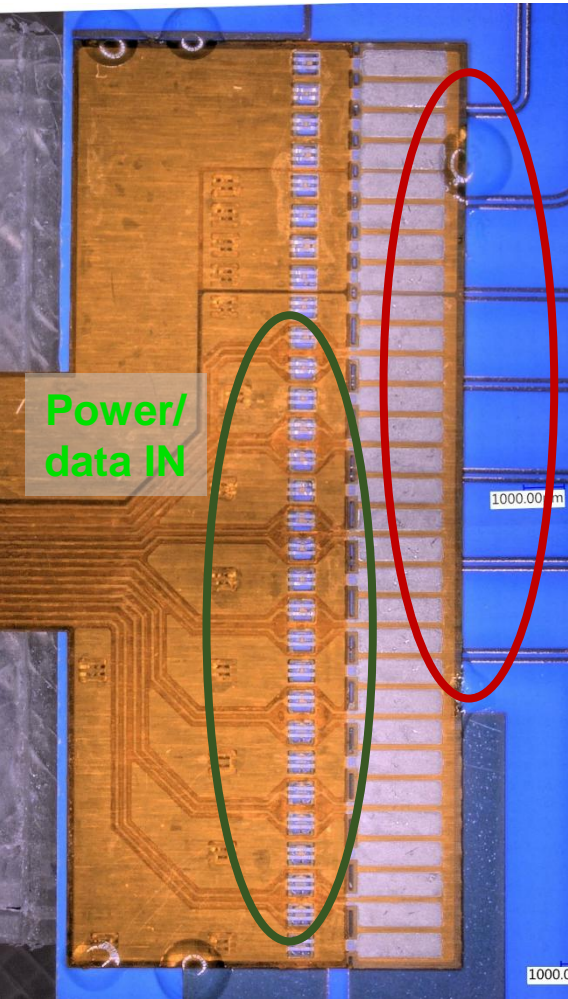


# For the eagle eyed!



- The differential lines don't line up!
- We mounted the FPC up-side-down!

PCB differential lines  
FPC differential lines

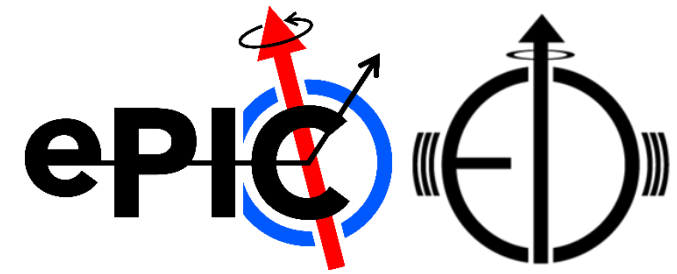


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# Actual connections

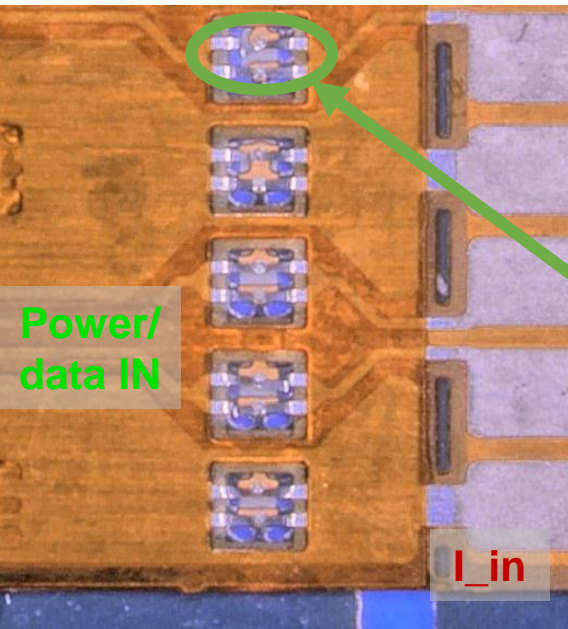
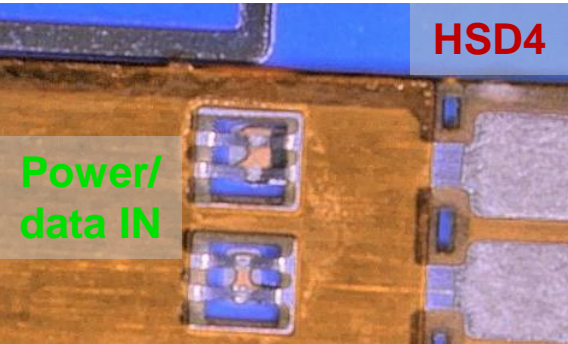
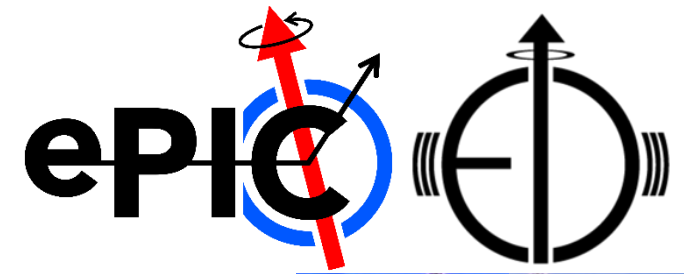


Only interested in the SCTRL1, SCTRL2, SCTRL3 (+&-) lines.  
(that run the full length of the FPC and are available on the **S/C OUT** PCB).

Power/data IN	FPC	S/C OUT
SCTRL1(+)	GND	SCTRL3(+&-)
SCTRL1(-)	HSD1(-)	Not connected
SCTRL2(+)	GND	SCTRL3(+&-)
SCTRL2(-)	SCTRL3(-)	GND
SCTRL3(+)	GND	SCTRL3(+&-)
SCTRL3(-)	SCTRL2(-)	SCTRL1(+)
GND	SCTRL2(+)	SCTRL1(-)
HSD1(-)	SCTRL1(-)	SCTRL2(+)
GND	SCTRL1(+)	SCTRL2(-)



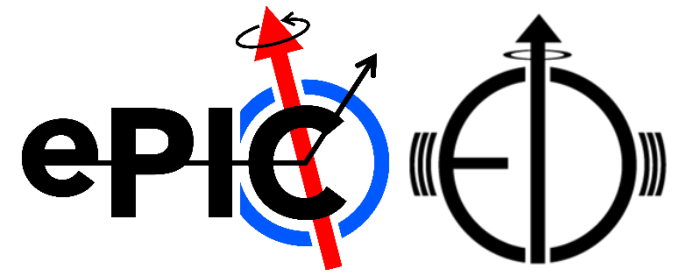
# Prototype to PCB bonding



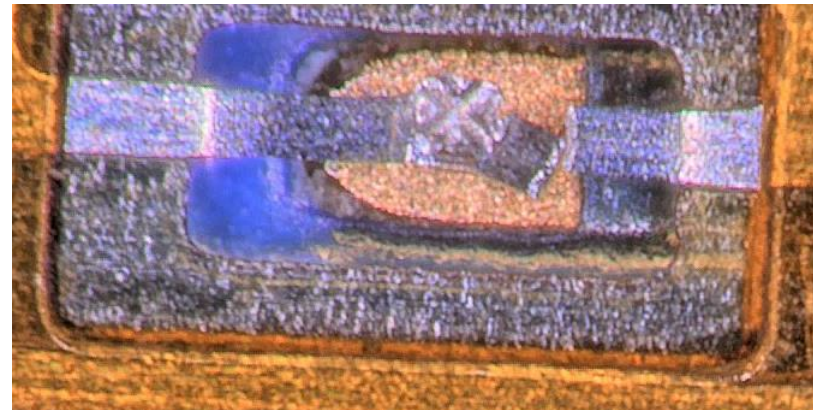
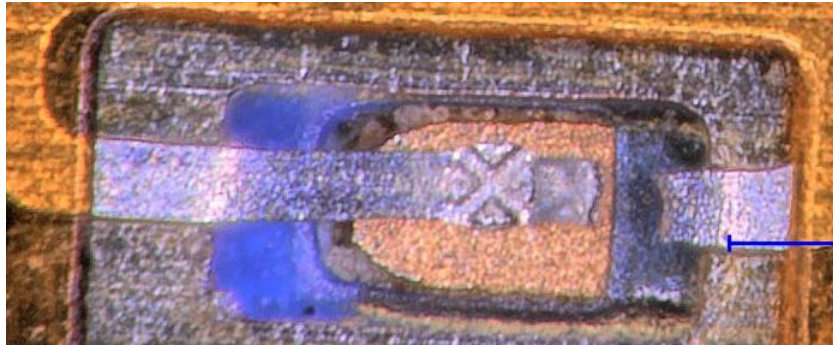
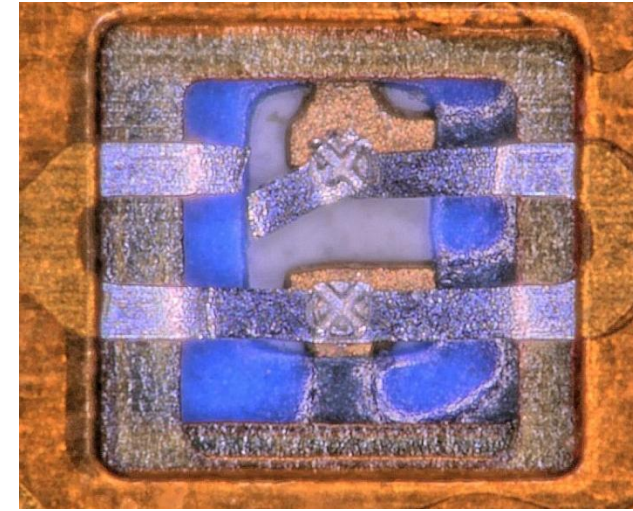
- Kept to the bond settings found to work well from [testing](#).
- Vertical offset between FPC and PCB seemed much smaller than with the (unglued) test structure.
- Observing bonds being done appeared to go very smoothly.
- A couple of foils had noticeable snapped at either end of FPC, seemed minimal.



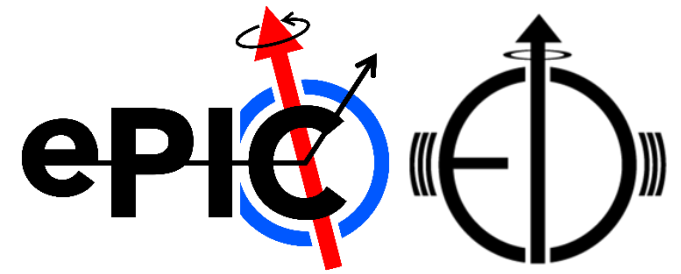
# Visual inspection (1)



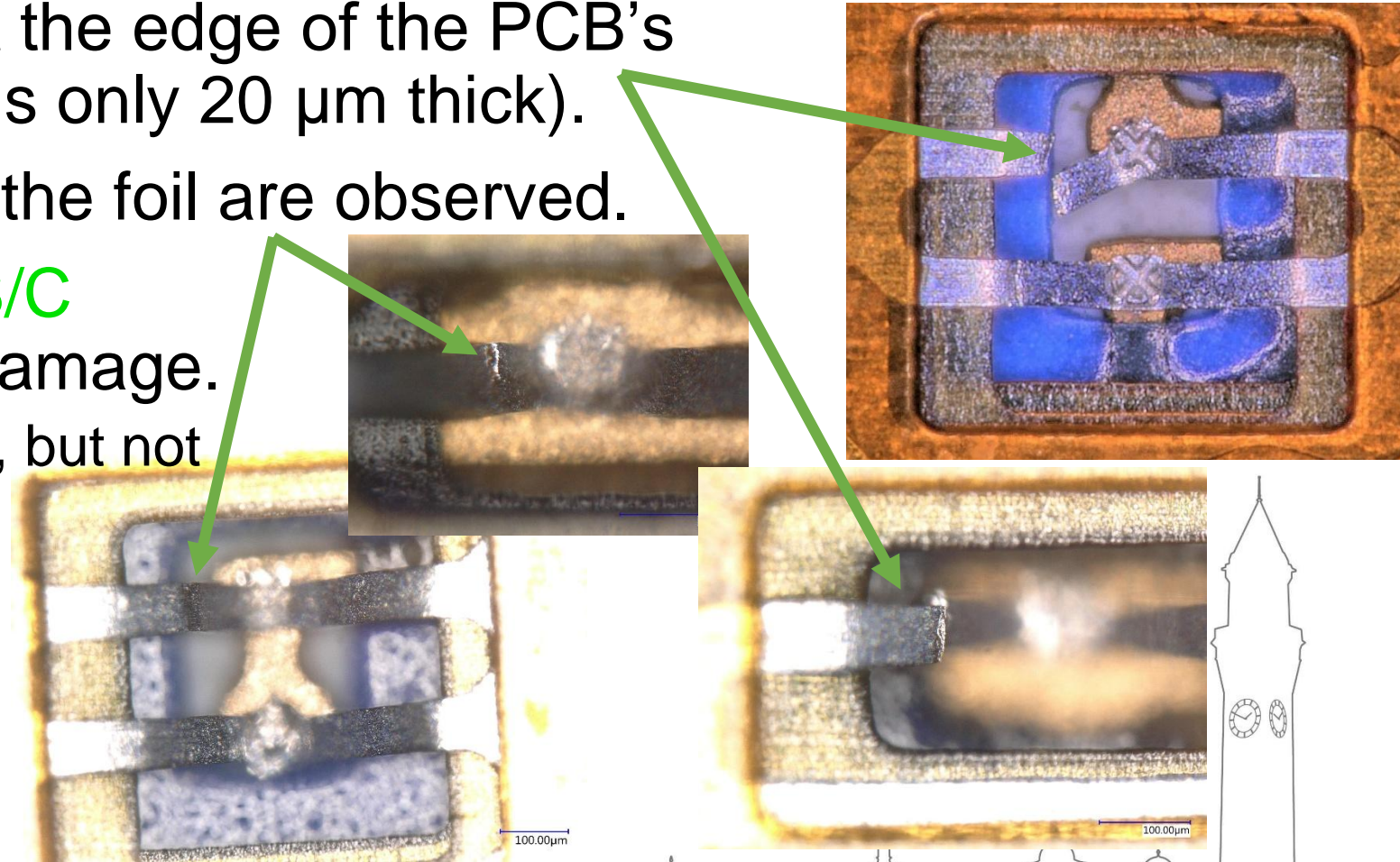
- A detailed visual inspection of the bonds (higher magnification, better lighting and observation angle control) has shown far greater damage to the FPC tracks – esp. **S/C OUT** side.
- Fully catalogued the damage into a [spreadsheet](#).



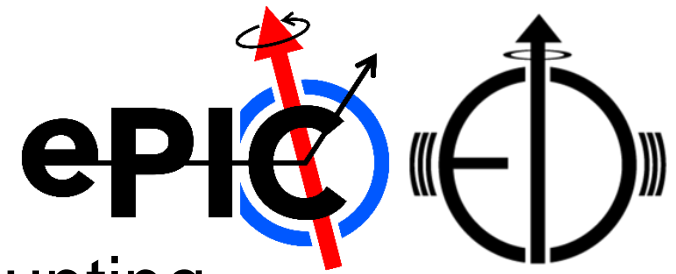
# Visual inspection (2)



- Most breaks appears at the edge of the PCB's solder mask (this layer is only 20  $\mu\text{m}$  thick).
- Some irregular kinks in the foil are observed.
- More than 60% of the **S/C OUT** side show some damage.
  - May still have continuity, but not ideal for HS data Tx.
  - Due to trouble keeping FPC flat at this end?
  - Only ~25% on the **Power/data IN** side.



# Summary

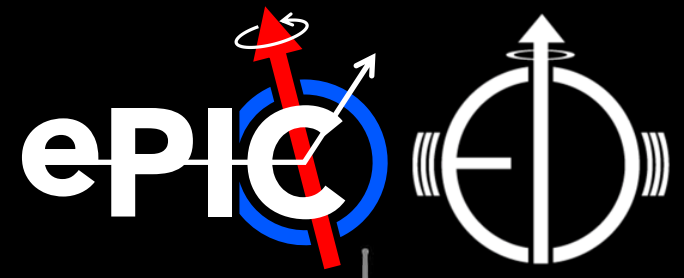


- Need to double-check FPC orientation prior to mounting.
  - Check all differential traces line-up.
  - Make sure termination resistors are removed from FPC.
  - Cut-off solder/probe pads prior to mounting.
    - Need to look at options for holding FPC without this extension.
- Bonding of FPC tracks to PCB pads seems to have good welds.
- Height difference between FPC tracks and PCB pads seems to be at a limit.
  - Keeping FPC flat to PCB surface is must!
    - Additional space on FPC (Kapton extensions) to hold down during gluing.
  - Minimising surface steps within the bond window might help.
    - PCB redesign with larger window in the solder mask is already done.



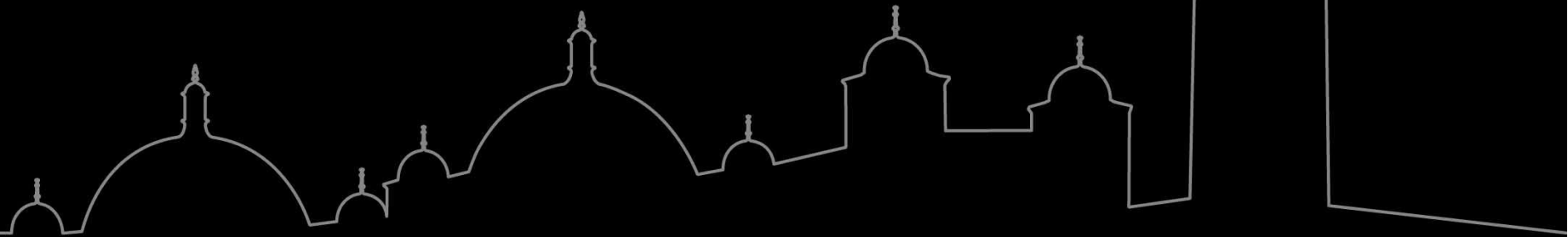


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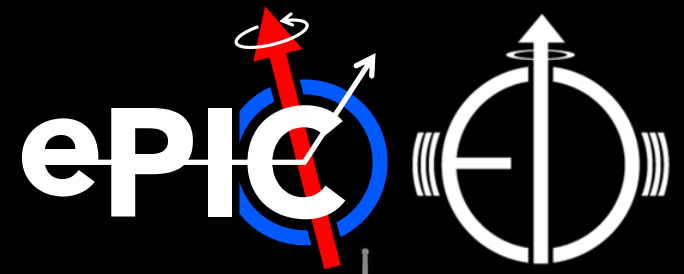
# Thank you very much!

Any questions?





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# Additional (support) slides

